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Original Article

Design and Energy Dissipation Analysis of an Interaction-Region based Single-Polarity Reconfigurable XOR/XNOR Gate for Quantum Dot Cellular Automata

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Abstract *- As Quantum Dot Cellular Automata is emerging as a promising alternative to CMOS technology for nanoscale designs, there is always a necessity for realization of compact and energy-efficient designs that perform reconfigurable logic. This paper shows a single-polarity, reconfigurable interaction-region based XOR/XNOR gate which eliminates the conventional majority-gate based structures by utilization of localized electrostatic interactions within a compact cell layout design. The proposed layout design performs dual functions, XOR or XNOR, using the same layout by varying the polarization of the control cell from -1 to +1, and thus performs dual operations without the requirement of additional hardware or structural modifications. Functional correctness of the proposed XOR/XNOR design is verified by using QCA Designer 2.0.3 under a bistable simulation engine, and energy dissipation analysis was performed using QCA Designer-E using Coherence energy vector simulation engine using both Euler's method and Runge-Kutta method. The proposed design utilizes an overall area of 0.01μm^2 with a latency of 0.5 clock cycles and 9 overall cells with output polarization of 0.965. By comparing the performance parameters of the proposed XOR/XNOR design with existing designs, it shows a reduction in cell count by 71.88% and an improvement in latency by 75%. Additionally, energy dissipation analysis was performed by using Euler's method and Runge-Kutta method, and comparative performance of energy dissipation was performed using different signals, Cos, Ramp and Gauss clock signals. The proposed design records a Total energy dissipation of 6.75×10^{-3} eV and 7.12×10^{-3} eV under Gaussian excitation with an Average energy value of 6.14×10^{-4} eV and 6.47×10^{-4} eV, and thus validates stable low-power operation. The results recorded in this work indicate that the proposed interaction-region based design architecture provides an efficient solution for the implementation of compact, programmable and energy-efficient QCA-based circuits for future nanocomputing applications.*

Keywords *- Single-Polarity, Interaction-Region based, Reconfigurable, Euler's method, Runge-Kutta method.*

1. Introduction

Quantum Dot Cellular Automata (QCA) has emerged as one of the most promising paradigms for next-generation nanoscale digital electronics as CMOS technology is approaching towards its physical and thermodynamic scaling limits. QCA-based circuits eliminate the power dissipation issues caused by leakage currents in sub-micron transistors as they replace the conventional voltage-current representation with localized cell interaction charges.

In terms of high operating frequencies, dense feature size and low power consumption, QCA-based designs show massive advantages and thus make it a suitable candidate for future ultra-dense nanocomputing platforms. For standard QCA-based logic circuit designing, a universal logic set composed of majority gates and inverters is used. This majority-logic scheme works well for designing of basic gates and small to medium-scale circuits, but for complex gates with reconfigurable features like XOR/XNOR, and thus for complex arithmetic and logic designs, this majority-gate design presents serious structural challenges. In conventional XOR/XNOR gate designing, it requires cascading of multiple majority gates and inverters, which results in high cell count, large physical layout design and propagation delays.

Thus, to overcome these issues, researchers have now focused on designing reconfigurable structures using alternative interaction-region-based strategies. Traditionally, XOR/XNOR architectures were designed using double-polarization or double-polarity configurations, which provide operational flexibility, but they drastically increase layout complexity, complicate single-layer clock routing, and result in severe leakage and cross-talk noise amid tightly packed cell arrays.

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However, for existing interaction-region-based design approaches, there is still a requirement for careful optimization for the arrangement of cells and control of polarity in order to achieve a reconfigurable XOR/XNOR gate design primitive with reduction of structural complexity. Thus, there is always a necessity for a compact architecture that is capable of providing XOR/XNOR reconfigurability by the usage of a single polarity control mechanism while maintaining a reduction in cell count and single -layer design implementation.

In order to address these limitations, this paper presents a highly compact, interaction-region based reconfigurable XOR/XNOR block by utilizing a single-polarity control scheme. The proposed design eliminates traditional majority gates-based designing and employs interaction-region-based design by using direct neighborhood coulombic repulsion forces inside a localized cell cluster. By elimination of double-polarity, the proposed design achieves a reconfigurable block that, with a change of polarity, switches the function from XOR to XNOR. When the polarity of the control cell is -1, it acts as an XOR gate and with a change in polarity to +1, it works as an XNOR gate.

The primary contributions of the proposed work involve Majority-gate free design, Single-polarity control mechanics, and physical efficiency optimization. Therefore, the novelty of the proposed design includes a localized interaction-region based structure with a single-polarity control cell in order to switch between XOR/XNOR structures, which otherwise requires designing desired multiple majority gates, cascaded logic or double-polarity control configurations.

Thus, the proposed design is capable of function as a reconfigurable block by reversing the polarity of a single control cell. Therefore, the proposed reconfigurable interaction-region based XOR/XNOR design primitive shows a reduction in structural complexity by maintaining a single-layer structure. Thus, with the majority-gate free design feature, we utilized a single-layer interaction-region based design, which performs as a reconfigurable device without cascading of majority gates and thus reduces the propagation delay.

With Single-polarity control mechanics, the given design eliminates complex wire crossovers and noise liabilities of double-polarity networks by having a single-polarity node that toggles between two operations.

The physical efficiency optimization of the proposed design is validated by bistable and coherence-vector simulations by using QCA Designer 2.0.3 and QCA Designer-E tools, which show improvement in cell reduction, area utilization and latency as compared to previous designs. The energy dissipation analysis is performed using Euler's method and the Runge-Kutta method.

2. Related Work

In QCA-based designs, the binary information is transferred by using polarization of QCA cells, and thus computation is performed by using coulombic interactions between adjacent cells. Because of ultra-low power consumption, high-device density and potential for nanoscale integration, QCA technology is well-thought-out as an attractive platform for implementation of next-generation digital systems [9, 11].

Among fundamental logic gates, the Exclusive-OR (XOR) and Exclusive-NOR (XNOR) gates play a significant role in digital circuit design. These gates are widely used in arithmetic and logic circuits like adders, comparators, parity generators, error detection units, and arithmetic logic units, etc., and thus the realization of these gates is an important research topic in QCA technology [11, 12].

There are many QCA-based designs for XOR/XNOR gates that have been implemented by researchers with the objective of reducing cell count, area, latency and power dissipation. Sheikhfaal et al. [5] and Chabi et al. [6] introduced efficient QCA-based design methodologies that provide improvement in terms of circuit performance and implementation efficiency. Ahmad et al. [7] show the significance of arithmetic circuits realization using the XOR gate, while Safoev et al. [8] designed a QCA-based XOR gate that is suitable for arithmetic and logic applications. Salih et al. [9] proposed a dual-functional XOR block that is capable of performing multiple logic functions, while Laajimi et al. [10] designed a compact XOR gate with a reduction in circuit complexity.

With all of the above advancements in QCA-based XOR/XNOR designs, there is still scope for designing a compact reconfigurable XOR/XNOR block with less complexity and reliable operation. Motivated by these observations, this paper presents a compact interaction-based reconfigurable XOR/XNOR block for QCA-based applications. The proposed QCA-based XOR/XNOR design utilizes localized cell interactions along with an appropriate clocking strategy, which realizes XOR and XNOR functionalities within a single layout without the need for any extra hardware.

3. Research Methodology

The proposed interaction-region based reconfigurable XOR/XNOR block was designed by using localized coulombic interactions between two neighboring QCA cells, in contrast to conventional majority-gate-based synthesis logic. The design methodology of projected design consists of three sequential stages, which are: interaction-based logic formulation, electrostatic interaction modelling and functional modelling. The overall design methodology for the proposed design primitive is shown in Figure 1.

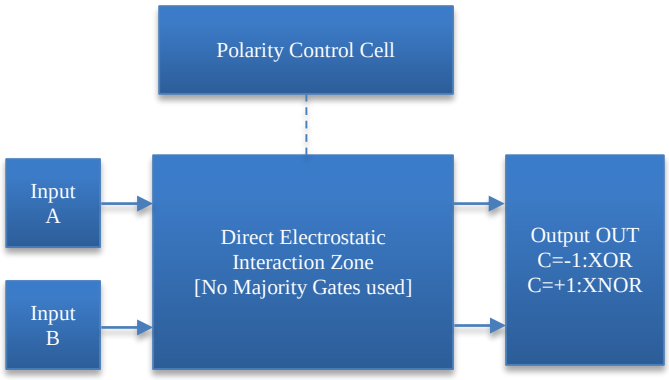


Fig. 1 Block diagram of proposed XOR/XNOR block

3.1. Interaction-based Design Methodology

The proposed design methodology utilizes localized inter-cell coulombic interactions in order to realize logic computation, unlike conventional QCA-based XOR/XNOR gates, which employ cascaded majority gates and inverter networks. The circuit is formulated by using two input cells, A and B, along with a Single Polarity Control Cell (C) as shown in Figure 1.

The control cell is capable of altering the local interaction field without altering the physical layout and thus provides a dynamic switching between XOR and XNOR operations without any need for extra hardware. Therefore, the proposed design layout reduces hardware redundancy while preserving a compact single-layer implementation.

3.2. Electrostatic Interaction Modelling

The operation of the proposed design primitive is based on electrostatic interactions between neighboring QCA cells. The polarization of each cell is dependent on the surrounding electric field generated by adjacent cells. Throughout computation, the interaction region itself converges towards the minimum-energy polarization state and therefore produces the desired logical output.

The polarization of the QCA cell is given as:

$$P = \frac{(q1+q3)-(q2+q4)}{\Sigma_{i=1}^{4}|qi|}$$

Where qi represents the charge associated with the four quantum dots of a QCA cell.

The electrostatic interaction between neighboring charges is represented by kink energy as:

$$E_k = V_{opposite} - V_{same}$$

Where $V_{opposite}$ and V_{same} represent the electrostatic interaction energies in correspondence with opposite and identical neighboring cell polarizations, the proposed design methodology utilizes this natural energy minimization mechanism for the realization of interaction-based logic computation.

3.3. Functional Logic Modelling

The proposed XOR/XNOR reconfigurable gate is mathematically represented as:

$$Y = A \oplus B, \quad C = -1$$

$$Y = A \odot B, \quad C = +1$$

Where $\oplus$ denotes the XOR operation and $\odot$ denotes the XNOR operation, Cϵ {-1, +1} represents the polarization of the control cell.

For C=-1,

Y=A$\oplus$B corresponds to the XOR operation.

For C=+1,

Y=A$\oplus$B$\oplus$1=A$\odot$B, corresponds to the XNOR operation.

4. Materials and Methods

The projected layout is designed using the QCA Designer 2.0.3 tool, and for the simulation of the design, the QCA Designer 2.0.3 tool is employed with a bistable simulation engine setup with specifications as shown in Table 1. The results validate the effectiveness of the proposed single-polarity design approach.

Table 1. QCA designer 2.0.3 setup for simulation

Design Parameter	Value	Unit
Temp (T)	1	K
Dot cell	18	Nm
QD size	5	Nm
CLK zone	4	Clock cycles
Samples	12800	-
Tolerance	0.001000	-
Radius of effect	65.000000	Nm
Relative Permittivity	12.900000	-
Clock High	9.800000e-022	J
Clock Low	3.800000e-023	J
Clock amp	2.000000	Clock cycles
Layer separation	11.500000	Nm
Iterations	100	-

In order to accomplish energy dissipation analysis for the proposed QCA-based reconfigurable XOR/XNOR design, the QCA Designer-E tool is used with the Coherence-vector energy simulation engine, as shown in Table 2, using both Euler's method and Runge-Kutta method in the specifications.

Table 2. QCA Designer-E setup (Coherence vector energy)

QCA Designer - E design setup for Euler's Method/Runge-Kutta Method (Coherence Vector Energy)		
Specification	**Value**	**Unit**
Temperature	1.000000	K
Relaxation Time	1.000000e-015	s
Clock Period	4.000000e-012	s
Input Period	4.000000e-012	s
Time Step	1.000000e-016	s
Total Simulation Time	5.000000e-011	s
Clock High	9.800000e-022	J
Clock Low	3.800000e-023	J
Clock Shift	0.000000e+000	-
Clock Slope (RAMP, GAUSS)	1.000000e-012	s
Radius of Effect	80.000000	nm
Relative Permittivity	12.900000	-
Layer Separation	11.500000	nm

5. Proposed Reconfigurable XOR/XNOR Layout Design

Figure 2 shows the layout of an anticipated interaction-based reconfigurable XOR/XNOR design, which is designed using single polarity and a compact single-layer structure. The designed layout consists of two input cells, A and B, one polarity control cell, C and an output cell, Y. In the anticipated design, there is an interaction region formed by intermediate QCA cells and an output cell, and the proposed architecture realizes the logic by localized coulombic interactions in between neighboring cells, unlike conventional QCA-based implementations for the XOR and XNOR gates that employ cascade majority gates and an inverter for the realization of logic.

In the projected layout design, the interaction region serves as the computational core in which the combined electrostatic influence of the input and control cells determines the polarization of the output cell. By maintaining the same layout design and variation of polarity of the control cell, the proposed design is capable of performing either XOR or XNOR operation without the requirement of additional hardware or structural modifications.

As shown in Figure 2, it is clear that the proposed interaction-based design reduces routing complexity while preserving single-layer implementation and performing two functions with the same layout by just variation of polarity, and thus validates it for high-density QCA circuit design.

Table 3 shows the Truth table for the given XOR/XNOR design, which shows that when the polarity of the control cell is -1, the proposed block acts as an XOR gate, and with +1 polarity of the control cell, the same circuit behaves as an XNOR gate.

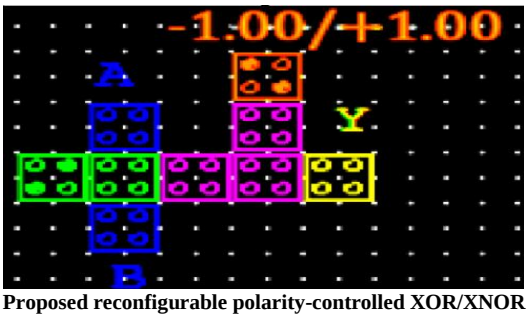


Fig. 2 Proposed reconfigurable polarity-controlled XOR/XNOR block

Table 3. Truth table of proposed XOR/XNOR block

Input A	Input B	Output Y with Polarity=-1	Output Y with Polarity=+1
0	0	0	1
0	1	1	0
1	0	1	0
1	1	0	1

The intended interaction-based XOR/XNOR gate utilizes a conventional four-phase QCA clocking mechanism in order to ensure reliable signal propagation and stable polarization transfer. The input cells A, B and the polarity control cell are assigned to the initial clock zone, which is then followed by sequential clock zones for the interaction region and the output cell. By this arrangement, the polarization generated by input cells propagates through the interaction region in a synchronized manner until the output reaches a stable logic state. Therefore, the sequential clock assignment maintains the proper flow of information and thus minimizes signal degradation and ensures reliable operation of both XOR and XNOR modes without the requirement of any additional synchronization circuitry.

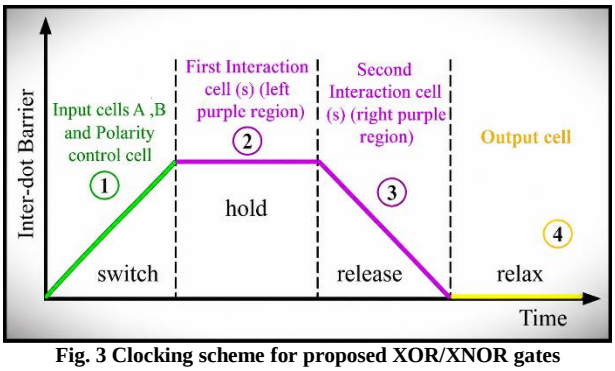
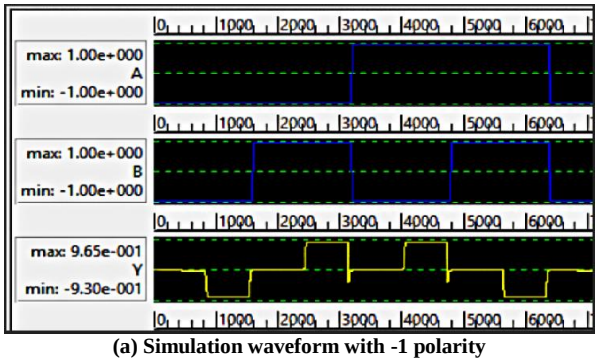


Fig. 3 Clocking scheme for proposed XOR/XNOR gates

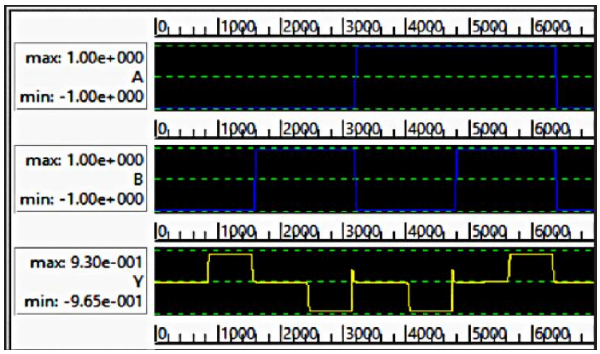
6. Results and Discussion

6.1. Functional Verification of Proposed XOR/XNOR Gate

For simulation and functional verification of the proposed design, the QCA Designer 2.0.3 tool is employed with a bistable engine simulation setup with specifications as shown in Table 1. The results validate the effectiveness of the proposed single polarity design approach by following the truth table of the designed reconfigurable block as shown in Table 3.



(a) Simulation waveform with -1 polarity



(b) Simulation waveform with +1 polarity

Fig. 4 Simulation waveform for proposed XOR/XNOR gate, (a) With-1 polarity, and (b) With +1 polarity.

Figure 4 shows the simulation waveforms attained by taking into consideration all the possible combinations of A and B while varying the polarity control cell C. When the control cell is fixed at -1 polarity as shown in Figure 4(a), the proposed design acts as an XOR gate; however, by changing the polarity of the control cell from -1 to +1, it reconfigures the same physical layout to act as an XNOR gate. Thus, the obtained output waveform completely follows the truth table of the proposed design as shown in Table 3, and consequently validates the correctness of the proposed interaction-based reconfigurable mechanism for the proposed design architecture. The results shown in Figure 4 demonstrate that the given circuit achieves dynamic logic reconfiguration through control cell polarization and clocking mechanism without the requirement of majority gates, inverter stages or any requirement for modifications to the physical layout.

6.2. Comparative Performance Analysis

Table 4 shows the performance description of the anticipated XOR/XNOR design with comparative analysis based on these performance parameters with existing designs. Our design employs a total of 9 cells for layout design with a total area consumption of 0.01 μm². The latency of the proposed design is 0.5 clock cycles, which results in an amended Area-Delay Product (ADP). Therefore, our design accomplishes a balance amid compactness and performance.

Table 4 also shows a comparison of the projected design with the present designs, considering performance constraints corresponding to overall cells, layout area and latency. By analysing Table 4, our proposed design shows improvement in terms of reduced cell count by 71.88%, less area and latency improvement by 75% as compared to existing designs.

Therefore, the proposed reconfigurable interaction-region based XOR/XNOR design is well-suited for compact and efficient implementation of arithmetic and logic circuit designs in Quantum-dot Cellular Automata.

Table 4. Comparative performance analysis of proposed XOR/XNOR gate

Author [Ref]	Cells	Area (μm²)	Latency (Clock Cycles)	Output Polariza-tion	Polarity/ Operation
Shiekhafal [5]	32	0.02	1	0.952	Dual/Single
A.M. Chabi [6]	29	0.03	0.75	0.885	Dual/Single
F. Ahmad [7]	27	0.03	0.5	0.954	Dual/Single
Nurriddinsafoev [8]	14	0.01	2	0.954	Dual/Single
A. Bassam [9]	13	0.01	2	0.950	Dual/Dual
Laajimi [10]	10	0.008	1	0.925	Dual/Single
Bandan K. Bhoi [11]	9	0.02	0.25	0.862	Dual/Single
Proposed Design	9	0.01	0.5	0.965	Single/Dual

7. Energy Dissipation Analysis

7.1. Energy Dissipation Analysis using QCA Designer-E

In order to validate thermal stability and energy efficiency of proposed reconfigurable XOR/XNOR interaction-region based design primitive energy dissipation analysis was performed with QCA Designer - E by using both Euler's method and Runge-Kutta method by consuming Coherence Vector Energy Engine Setup as shown in Table 2. The Euler's method is basically a first-order approach that estimates the next polarization state by calculating the derivative at the current time-step and thus offering fast computation. In contrast, the Runge-Kutta, also known as the RK4 method, is considered a highly accurate fourth-order technique which samples four distinct derivatives across each time-step interval in order to compute a weighted average and thus provide a precise, stable and mathematically rigorous simulation required in order to justify complex layout optimizations. The energy dissipation analysis is shown in the Table 5,6 shows distinct variations in the numerical performance and stability of the two methods. By Euler's method, total energy

dissipation is 6.75×10^{-3} eV with an average energy dissipation of 6.14×10^{-3} eV with an error margin of ± -7.11×10^{-4} eV and ± -6.46×10^{-5} eV. However, with the Runge-Kutta method, the total energy value is 7.12×10^{-3} eV, and the average energy dissipation value is 6.47×10^{-4} eV. In contrast to higher total energy values and average energy values, the Runge-Kutta method shows superior simulation accuracy and numerical stability by yielding significantly reduced error margin values of ± -3.29×10^{-4} eV, ± -2.99×10^{-5} eV, which are nearly half of Euler's method.

Table 5. Energy dissipation analysis of proposed XOR/XNOR gate using Euler's method

E_bath_total (eV)	E_clk_total (eV)	E_Error_total (eV)
2.4093e-004	6.2221e-004	-2.7789e-005
4.7143e-004	-5.6192e-004	-4.1838e-005
4.8017e-004	-5.2791e-004	-5.4888e-005
1.5858e-003	-1.2032e-004	-1.6855e-004
Total energy dissipation (Sum_Ebath) (eV) Error-margin (eV)		6.75e-003 ± -7.11e-004
Average energy dissipation per cycle (Avg_Ebath) Error-margin (eV)		6.14e-004 ± -6.46e-005

Table 6. Energy dissipation analysis of proposed XOR/XNOR gate using Runge-Kutta method

E_bath_total (eV)	E_clk_total (eV)	E_Error_total (eV)
2.5803e-004	6.1851e-004	-1.4358e-005
4.9925e-004	-5.6185e-004	-1.5275e-005
5.0829e-004	-5.2785e-004	-2.7821e-005
1.6628e-003	-1.2266e-004	-7.8330e-005
Total energy dissipation (Sum_Ebath) (eV) Error-margin (eV)		7.12e-003 ± -3.29e-004
Average energy dissipation per cycle (Avg_Ebath) Error-margin (eV)		6.47e-004 ± -2.99e-005

On comparison of two methods as shown in Figure 5, it is validated that the designed reconfigurable XOR/XNOR architecture shows precise convergence, and with tighter values of error margin of the Runge-Kutta method, it is proven that the design is free of simulation-induced fluctuations and thus stable.

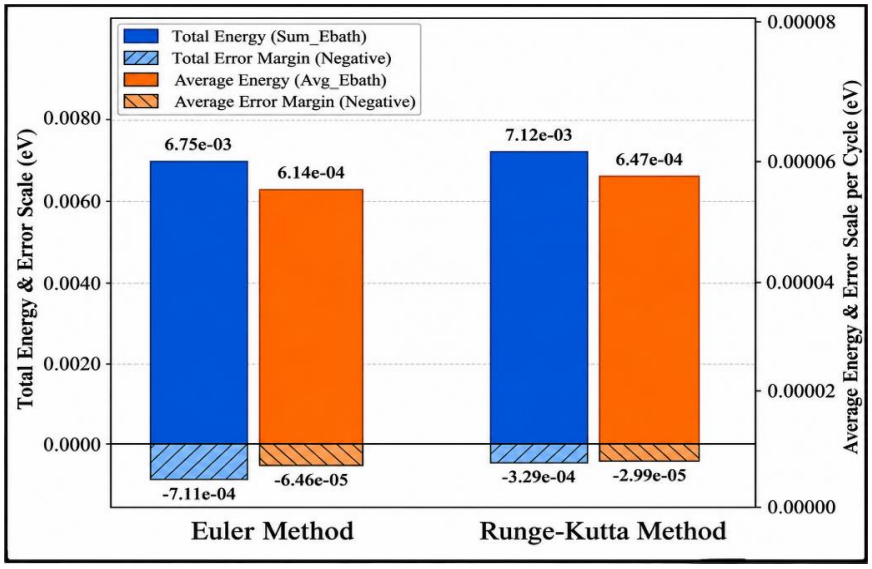


Fig. 5 Energy dissipation analysis of proposed XOR/XNOR using Euler's method and Runge-Kutta method

In order to evaluate the thermal behaviour and power efficiency of the projected interaction-based XOR/XNOR gate, the comparative analysis of Total energy and average energy dissipation across different input clock signals: Cosine, Ramp and Gauss, using QCA Designer-E under coherence energy vector as shown in Table 7.

Table 7. Energy dissipation comparative analysis at different signal types

Signal Type	Energy dissipation (eV)	Euler's Method	Runge-Kutta Method
Cos Type	Total Energy Error Margin	8.29e-003 ± -8.48e-004	8.83e-003 ± -3.83e-004
	Average Energy Error Margin	7.54e-004 ± -7.71e-005	8.03e-004 ± -3.49e-005
Ramp Type	Total Energy Error Margin	0.00e+000 ± - 0.00e+000	0.00e+000 ± - 0.00e+000
	Average Energy Error Margin	0.00e+000 ± - 0.00e+000	0.00e+000 ± - 0.00e+000
Gauss Type	Total Energy Error Margin	6.75e-003 ± -7.11e-004	7.12e-003 ± -3.29e-004
	Average Energy Error Margin	6.14e-004 ± -6.46e-005	6.47e-004 ± -2.99e-005

As shown in the Table 7, it's evident that the Runge-Kutta method exhibits slightly higher accuracy in energy dissipation values with a tighter error margin 3.83×10^{-4} eV for Cos type signal in comparison with Euler's method and is consistant with its higher order mathematical formulations. However, with Ramp type signal, the energy dissipation value is 0.00 eV. This zero-valued energy dissipation value is attributed towards the numerical precision/threshold of the coherence vector simulation engine and therefore does not imply absolute zero physical energy dissipation. Conversely, with a Gauss-type signal, total energy dissipation of 7.12×10^{-3} eV was observed using the Runge-Kutta method, and thus such a low energy value confirms that the proposed layout design fulfils ultra-low-power nanoscale design requirements. The given resultant pattern is shown in Figure 6.

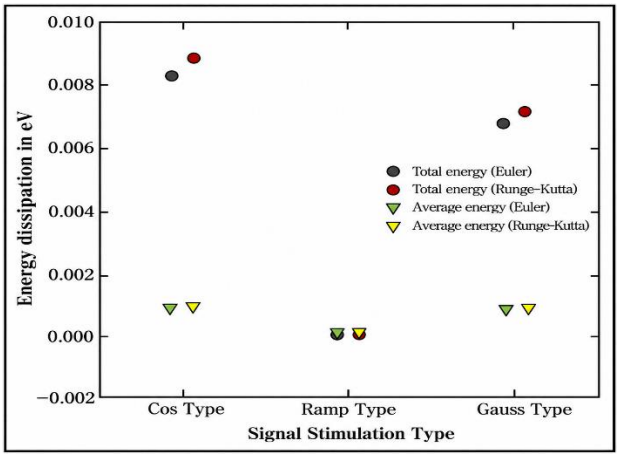


Fig. 6 Energy dissipation comparative analysis with different signal inputs

7.2. Kink Energy Analysis for Proposed XOR/XNOR Design

In QCA-based architectures, the stability of signal propagation and path selection boundaries depends directly on Kink Energy (E_k) in between interacting cells. The kink energy is represented as the difference between fully stable states, i.e. parallel polarization and faulty configuration, i.e. anti-parallel polarization. For a QCA cell having quantum dots, the total electrostatic interaction energy U between cells 'i' and cell 'j' can be calculated by summing up the Coulombic forces across all active quantum dots of each cell, and can be given as:

$$U = \sum_{a=1}^{4}\sum_{b=1}^{4}\frac{q_a q_b}{4\pi\varepsilon_0\varepsilon_r|r_{ia}-r_{jb}|}$$

Where q_a and q_b represent the localized electronic charges within dots, ε_0 is the permittivity of free space, and ε_r is the relative permittivity of the material substrate, and $|\, r_{ia}\text{-}r_{jb} \,|$ is the spatial distance between respective dots. Therefore, by evaluating the difference between mismatched, i.e. anti-parallel and matched, i.e. parallel, state energy denoted as Umismatched and Umatched, the kink energy can be given as:

$$\mathrm{Ek_{ij}} = \mathrm{U_{mismatched}} - \mathrm{U_{matched}}$$

For the proposed layout design, which is operating under standard default design values of (18nm×18nm cells arranged on a 20nm centre-to-centre grid mesh, the structural kink energy of each interaction region, depending upon cell layout, can be calculated by using an effective single-variable formulation, which evaluates the primary centre-to-centre distance (r_1) and secondary neighbor cross talk boundaries (r_2) can be given as:

$$E_k = \frac{e^2}{4\pi\varepsilon_0\varepsilon_r}\cdot\left(\frac{1}{r_1}-\frac{1}{r_2}\right)$$

By substituting the physical constant values of the substrate, we get;

$$\frac{e^2}{4\pi\varepsilon_0\varepsilon_r} \approx 1.115\times10^{-10} eVm = 0.1115 eVnm$$

Figure 7 shows the interaction region breakdown of our proposed XOR/XNOR gate, where the designed layout is divided into three main regions: the input intersection region, the control and selection core region and the output phase coupling region. So by applying the above mathematical

analysis and depending upon values of r1 and r2 from the designed layout of each region, we can calculate the Kink energy value for each specific region as shown in Table 8.

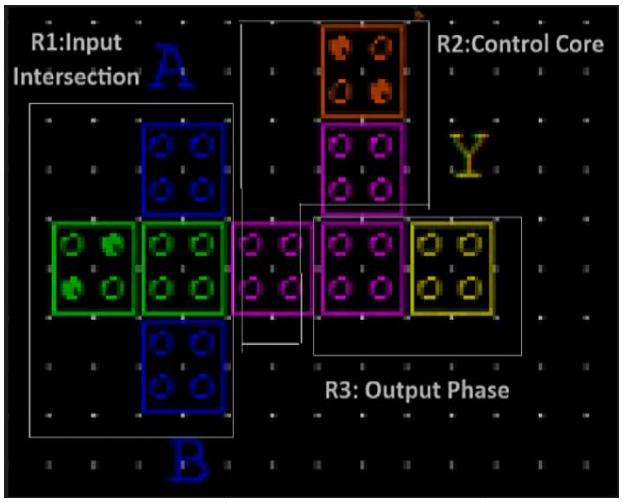


Fig. 7 Interaction region for kink energy calculations for the proposed XOR/XNOR gate

Table 8. Interaction-based kink energy calculation for proposed XOR/XNOR

Region	r1(nm)	r2(nm)	E_k (eV)
R1: Region.1 Input Intersection	20	40	2.7875×10^{-3}
R2: Region.2 Control core	18	34	2.9150×10^{-3}
R3: Region.3 Output phase	22	42	2.4134×10^{-3}

Kink energy analysis is shown in the Table 8 shows the precise electrostatic distribution across the proposed nine-cell XOR/XNOR block. Region .2 which is the control core region and decides the operation of the designed reconfigurable interaction-region based XOR/XNOR gate block, shows the highest structural energy profile. Therefore, it validates a highly stable polarization bond within the main switching area. However, the transition regions, Region 1 and Region 3, which are input and output regions, show relatively less energy values but are comparable to Region 3.

8. Conclusion

This paper shows an interaction-region based reconfigurable XOR/XNOR gate using a single-polarity control mechanism for dual-function logic implementation in Quantum Dot Cellular Automata. Unlike conventional majority-gate-based designs, the proposed design employed localized electrostatic interactions for performing logic computation while maintaining a compact single-layer layout design. The proposed design acts as a polarity control design, whereby changing the polarity of the control cell from -1 to +1, it switches its operation from XOR to XNOR without the requirement of any additional modifications and hardware requirements. Functional verification was validated using QCA Designer 2.0.3 under a bistable simulation engine, which confirmed the correctness of logical operation for the proposed designed architecture.

Comparative analysis shows that the designed architecture requires only 9 cells, by consuming an area of $0.01\mu m^2$ and an output polarization of 0.965, and thus validates the significant improvements in terms of compactness, computational efficiency and signal integrity in comparison with existing QCA-based XOR/XNOR designs. Energy dissipation analysis was performed using both Euler's method and Runge-Kutta method, which further verifies the low-power characteristics of the designed architecture. The proposed design shows a Total energy dissipation of 6.75×10^{-3} eV and 7.12×10^{-3} eV under Gaussian excitation with an Average energy value of 6.14×10^{-4} eV and 6.47×10^{-4} eV. Therefore, the interaction-region based proposed design demonstrates single-polarity programmable control and effectively realizes the compact and reconfigurable QCA-based logic while reducing hardware complexity and maintaining high output polarization. The projected architecture thus serves as an efficient building block for development of complex QCA-based arithmetic circuits, reconfigurable logic systems and future ultra-low -power nanoscale computing architectures.

Conflicts of Interest

"The author(s) declare(s) that there is no conflict of interest regarding the publication of this paper."

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