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Original Article

An Energy-Efficient 3T-1VGSOT-MTJ MRAM Cell and Array for Resource-Constrained IoT Edge Computing

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Abstract *- Spintronic devices have emerged as an attractive technology for emerging memory and logic architectures due to their non–volatility, high–speed, and CMOS compatibility. Therefore, this work demonstrates the significance of Voltage–Gated Spin-Orbit Torque Magnetic Tunnel Junction (VGSOT–MTJ) due to a lower energy barrier during switching and offers an in–plane exchange bias. This paper presents a novel 3T–1VGSOT–MTJ memory cell, which is simulated and modelled in Cadence Virtuoso at the 45nm technology node for energy-efficient IoT applications. A comprehensive analysis of switching behavior is conducted by varying free layer thickness, MTJ diameter, input voltage, and Spin Hall Effect (eta) parameters. Switching delays of 3T–1VGSOT–MTJ MRAM are characterized to evaluate reliability and performance tradeoffs at 45 nm technology. The proposed cell demonstrates a significant energy reduction of 88.20%, 55.45% and 68.23% for P–AP and 87.76%, 54.58% and 67.53% for AP–P switching compared to state–of–the–art designs. Additionally, a 1Kb MRAM array is proposed with the help of a 3T–1VGSOT–MRAM cell for low power, resource and area-constrained IoT applications. Furthermore, the 3T–1VGSOT–MTJ MRAM layout is implemented in compliance with design rules, contributing to area reduction and thereby enabling lower power consumption, cost–effective fabrication, and suitability for compact IoT applications. Simulation results confirm its energy efficiency and suitability for next–generation IoT edge platforms, offering marked improvements in switching delay and power–performance metrics over traditional MRAM structures.*

Keywords *- 3T-1VGSOT-MTJ design, Energy efficiency, Iot memory, Non-Volatile memory, Spin hall effect.*

1. Introduction

As semiconductor technology continues to push the boundaries of miniaturization, even established nodes are confronting critical challenges that limit further improvements in performance, power efficiency, and reliability [1, 2]. Traditional CMOS–based systems rely on volatile logic and memory elements, which require a continuous power supply to retain data. This leads to high static power consumption, which is a major concern in modern computing systems, especially those targeting energy–constrained environments such as mobile, IoT, and edge devices [3, 4]. Moreover, scaling limitations have introduced a host of reliability issues, including increased leakage currents, short–channel effects, and reduced device variability margins. These issues collectively degrade the energy efficiency and robustness of modern circuits, making it difficult to meet the growing demands for faster, denser, and more secure integrated systems. To address these shortcomings, there is a growing shift toward Non–Volatile Memory (NVM) technologies that can retain data without power while remaining compatible with existing CMOS infrastructure [5, 6]. In this context, spintronic–based memory technologies, especially Magnetic Tunnel Junction (MTJ)–based Magnetoresistive Random Access Memory (MRAM), offer a promising alternative due to their non–volatility, high endurance, and CMOS compatibility [7-9]. The authors of [10] introduce an energy–efficient multi–retention Spin Transfer Torque (STT)–MRAM architecture for Internet of Things (IoT) devices by classifying data based on lifetime and assigning them to memory cells with appropriate retention levels. By relaxing non–volatility for short–lived IoT data and using high–retention MRAM only, when necessary, the approach significantly cuts write energy and achieves an average 66% energy reduction compared to conventional single–retention designs, directly addressing battery–driven IoT constraints. Furthermore, [11] presents a power and area-efficient full adder based on Voltage Controlled Magnetic Anisotropy (VCMA)-STT MTJs, optimized for IoT applications, along with approximate

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magnetic full adders that exploit the error-tolerant nature of IoT workloads to achieve up to 9.5× reduction in power consumption. Using a Sobel edge-detection task as an IoT-relevant benchmark, the study demonstrates substantial power reduction with minimal accuracy degradation, making it well-suited for edge-level IoT computing. Additionally, [12] proposes an ultralow–voltage STT–MRAM solution for IoT systems by showing THAT TUNNEL FET (TFET) based Double-Barrier MTJ (DMTJ) STT–MRAM cells can reliably operate below 0.5 V, a key requirement for battery–operated and energy–harvesting IoT hardware. Compared to FinFET–based memories, the TFET–based MRAM achieves nearly 50% lower write energy and 60% faster switching for low–cost, highly constrained IoT environments. Despite the steady progress in energy–efficient IoT memory designs, all reported works rely on STT– or STT-assisted precessional VCMA–based switching mechanisms, which continue to suffer from read/write path conflicts, degraded sensing margins at ultra–low voltages, or accuracy–dependent energy gains. These limitations highlight the need for an MRAM architecture that can provide low power and energy consumption while maintaining reliable read and write operations.

Existing studies have demonstrated significant energy savings in STT–MRAM architectures and VCMA–MRAM architectures employing VCMA–STT MTJs, however, comparatively less attention has been given to energy–efficient Spin Orbit Torque (SOT)–MRAM architectures that can provide low power, energy, and delay with low area for resource–constrained applications. The use of independent read and write paths in SOT-MTJ provides an improvement in terms of reliability. However, its write operation generally requires a relatively high current to generate sufficient SOT for magnetization switching. Consequently, the associated energy overhead can become a limiting factor for low–voltage and energy–constrained systems. A research gap remains in developing compact MRAM cells that support field–free switching with low power, energy, delay, and area. Furthermore, the effects of significant device and operating parameters, including free–layer thickness (t_f), input voltage, MTJ diameter, and spin Hall effect (*eta*), on the storage of MTJ states require systematic investigation. In addition, relatively limited work has addressed the implementation of Voltage Gated Spin Orbit Torque (VGSOT)–MTJ–based MRAM at the memory–array level.

To address these identified research gaps, this work presents a compact 3T–1 VGSOT–MTJ MRAM cell and extends the design to a 1 Kb memory array. The Parallel (P) and Antiparallel (AP) storage states are evaluated by varying input voltage, MTJ diameter, t_f and *eta*, and the resulting delay characteristics are investigated. The proposed architecture combines three 45 nm CMOS transistors with a single VGSOT–MTJ device. The three–transistor configuration enables effective decoupling of the read and write paths, thereby suppressing read-induced disturbance and reducing leakage while maintaining reliable write functionality. During the write cycle, the VCMA mechanism further assists magnetic-state reversal by modulating the tunnel-barrier profile, thereby decreasing the current required for switching. The proposed architecture is analysed for switching behavior, delay characteristics, and energy efficiency under various device-level and operational parameters relevant to real-world IoT applications. This paper presents the following key contributions:

- A novel 3T–1 VGSOT–MTJ MRAM cell architecture is proposed, tailored for energy–constrained IoT applications, with low–voltage operation and reduced switching delay.
- A systematic sweep of key MTJ parameters, including free–layer thickness, input voltage, MTJ diameter, and eta, is performed to study their effects on the switching behavior of the proposed cell. The analysis focuses on identifying suitable operating conditions for low–voltage operation and reduced switching delay while maintaining reliable logic states.
- A 1 Kb MRAM array is designed using the proposed 3T–1 VGSOT–MTJ cell to demonstrate its scalability from the individual memory cell to the array level.
- Transient simulations are carried out to characterize the power and energy requirements of the proposed cell. The obtained results are used to assess its low–power operation and compare its performance with conventional MRAM approaches.
- The layout of the proposed MRAM bit cell is designed and presented to evaluate its physical area and demonstrate the compactness of the proposed architecture.

The novelty of this work lies in the proposed 3T–1 VGSOT–MTJ MRAM cell and its systematic evaluation through MTJ parameter sweeps to achieve reliable P/AP state storage at low operating voltage and reduced switching delay. The proposed cell achieves favorable performance across delay, power, energy, and area metrics, making it well suited to resource-limited IoT platforms. Its reduced energy requirement and compact implementation can help address the power and area constraints of edge devices without compromising high-speed operation.

The 1 Kb array implementation further demonstrates the scalability of the proposed cell for energy–efficient non–volatile memory systems. The result established the effectiveness of the proposed voltage–controlled spintronic memory design by demonstrating a compact, high–speed, and energy-efficient MRAM architecture with scalability toward future IoT systems.

The paper is organized as follows. Section 2 reviews existing MRAM architectures reported in the previous literature. Section 3 introduces the VGSOT–MTJ device, including its structural features and operating mechanism.

Moreover, this section demonstrates the circuit–level implementation and working of the proposed 3T–1 VGSOT–MTJ based MRAM. Furthermore, a 1Kb MRAM array based on the proposed MRAM bit–cell is presented. Section 4 presents the evaluation of the 3T–1 VGSOT–MTJ–based MRAM. Furthermore, Section 4 demonstrates the simulation results and compiles the key performance parameters in tabular form. Finally, the major findings and conclusions of the study are discussed in Section 5.

2. Literature Survey

Among the various MRAM architectures, SOT-based MRAM has attracted considerable research interest because the write mechanism is electrically decoupled from the read operations. This architecture can enable faster switching speeds and improved write reliability compared with conventional STT-based MRAM. Considering these characteristics, researchers have extensively investigated SOT–MRAM designs for their potential in low–power, high–speed, and resource-constrained IoT applications.

Previously, He et al. [13] demonstrated Spin-Orbit Torque MRAM for data processing, reporting an 8× reduction in data communication that led to an 8× improvement in energy efficiency, a key step toward exploiting SOT devices beyond conventional storage for compute-centric workloads. Afterwards, Kang et al. [14] subsequently introduced a charge-recycling technique for SOT-MRAM to avoid unnecessary write operations. By identifying and suppressing redundant switching events, the proposed scheme lowers the associated write-energy consumption and thereby improves the total power efficiency of the memory. Later, A field-free 3T2SOT-MRAM cell was reported by Wu et al. [15] for non-volatile cache-memory applications. Their evaluation of an 8 MB cache demonstrated a 38.9% improvement in read speed and a 96.1% reduction in read error rate, thereby alleviating the performance and reliability bottlenecks of SOT-based caches.

Afterwards, Nisar et al. [16] implemented a 4–bit MRAM cell based on the STT SOT mechanism. The reported evaluation showed 52.9% improvement in latency and 40% improvement in energy efficiency, respectively, demonstrating the density advantages of multi-bit SOT/STT cells. Subsequently, Hwang et al. [17] presented a field free STT assisted SOT–MRAM (SAS–MRAM) and estimated that 8–bit weight updates provide over a 20× improvement in energy delay product, primarily due to reductions in leakage energy and interconnect overhead, making the design well-suited for energy-efficient computing applications. Thereafter, Liu et al. [18] introduced a three-transistor SOT-MRAM bit cell incorporating shared diffusion regions. This configuration was developed to achieve reductions in cell area and energy consumption. The proposed layout reduces the overall cell footprint while preserving the required memory cell functionality. Recently, for neural-network computing, Wu et al. [19] developed an in-memory Booth multiplier using STT-assisted SOT-MRAM. This approach demonstrated the feasibility of performing multiplication within the memory structure, thereby expanding SOT-MRAM toward in-memory processing applications.

Taken together, these works trace the development of SOT–MRAM from basic data storage toward cache, multi-bit, and compute–in–memory applications, with successive refinements in speed, energy efficiency, density, and field-free operation.

However, conventional in-plane-field SOT-MTJ switching relies on an external magnetic field, which complicates both its design and operation. Moreover, the necessity for external fields can reduce energy efficiency and limit overall performance. Conventional SOT–MRAM also relies on high current densities for write operations, leading to increased power consumption.

These limitations motivate the investigation of alternative switching mechanisms capable of deterministic field–free operation while reducing the write energy and power requirements of SOT–based MRAM. In this context, voltage–controlled magnetic anisotropy can be combined with spin–orbit torque to develop a VGSOT–MTJ device. In addition to the SOT effect, an in–plane exchange bias is induced in the Antiferromagnetic (AFM) metal strip, generating a sufficient magnetic field to enable deterministic switching of the Free Layer (FL) magnetization [20]. The VGSOT–MTJ architecture thus presents a scalable, energy–efficient, and CMOS–compatible solution and is well suited for emerging applications such as IoT, logic–in–memory architectures, and hardware security primitives in 45 nm systems and beyond.

Table 1. VGSOT-MTJ device parameters

Parameter	Quantitative Values
Tunnel magnetoresistance (*TMR*)	150% [21, 22]
Diameter of MTJ (D)	50 nm [23]
MgO thickness (t_{ox})	1.4 nm [23]
Free layer thickness (t_f)	1.1 nm [23]
Saturation magnetization (M_S)	6.25×10^5 A/m [23]
Interfacial PMA at 0 V ($K_i(0)$)	3.2×10^{-4} J/m^2[23]
Gilbert damping factor (α)	0.05 [23]
Resistance-area product	650 Ω.μm^2 [23]
VCMA coefficient (β)	60 fJ/V.m [23]
IrMn length (L_{IrMn})	60 nm [24]
IrMn width (W_{IrMn})	50 nm [24]
IrMn thickness (T_{IrMn})	3 nm [24]
Resistivity (ρ_{IrMn})	2.78×10^{-6} Ω.m [24]
Spin Hall Angle (θ_{SH})	0.25 [24]
Exchange bias (H_{EX})	-40 Oe [24]

3. Modeling of 3T–1VGSOT–MTJ MRAM

This section highlights the key features of the VGSOT–MTJ, detailing its device structure, underlying physics, and operational mechanism. In addition, a 3T–1 VGSOT–MTJ–based MRAM architecture is proposed and evaluated by varying key device parameters to assess its suitability for energy-efficient and high–speed IoT applications.

3.1. Voltage Gated SOT- MTJ (VGSOT–MTJ)

The VGSOT–MTJ combines SOT and VCMA to enable electrical manipulation of magnetization with improved switching efficiency and reduced transition time. Its structure comprises two CoFeB ferromagnetic layers separated by an ultrathin MgO barrier, forming a magnetic tunnel junction, together with an IrMn antiferromagnetic layer that establishes the reference magnetization direction.

This configuration provides separate mechanisms for influencing magnetization dynamics and controlling the magnetic energy landscape. The principal device parameters considered in this study are listed in Table 1.

As shown in Figure 1, the MTJ consists of an FL and a Pinned Layer (PL), whose relative magnetization orientations determine the resistance of the junction. The PL provides a reference magnetic orientation, whereas the FL can switch between two stable configurations under suitable electrical and magnetic conditions. When the FL and PL magnetizations are P, electron transport experiences a lower resistance, denoted by $R_{\uparrow\uparrow}$.

Conversely, an Antiparallel (AP) configuration produces a higher resistance, $R_{\uparrow\downarrow}$. This resistance modulation enables the magnetic state to be electrically distinguished and used to encode binary information. The corresponding Tunnelling Magnetoresistance (TMR) ratio quantifies the relative resistance difference between the two configurations and is defined as [24]:

$$TMR = \frac{R_{\uparrow\downarrow} - R_{\uparrow\uparrow}}{R_{\uparrow\uparrow}} \quad (1)$$

The magnetic dynamics of the FL are governed through the modified Landau–Lifshitz–Gilbert (LLG) equation including STT and SOT terms [24].

$$\frac{\partial \vec{m}}{\partial t} = -\gamma \vec{m} \times \vec{H}_{EFF}(V_{MTJ}) + \alpha \vec{m} \times \frac{\partial \vec{m}}{\partial t} + \gamma H_{STT}^{DL} \vec{m} \times \vec{m}_P \times \vec{m} + \gamma H_{STT}^{FL} \vec{m} \times \vec{m}_P + \gamma H_{SOT}^{DL} \vec{m} \times \vec{m}_\sigma \times \vec{m} + \gamma H_{SOT}^{FL} \vec{m} \times \vec{m}_\sigma \quad (2)$$

$$H_{STT}^{DL} = \frac{\hbar P J_{STT}}{2e\mu_0 M_S t_f} \quad (3)$$

$$H_{SOT}^{DL} = \frac{\hbar \theta_{SH} J_{SOT}}{2e\mu_0 M_S t_f} \quad (4)$$

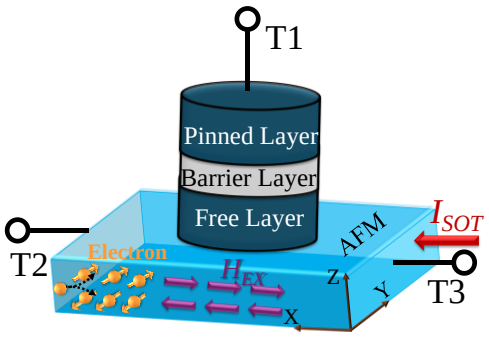


Fig. 1 Structural configuration of the proposed three-terminal VGSOT–MTJ device

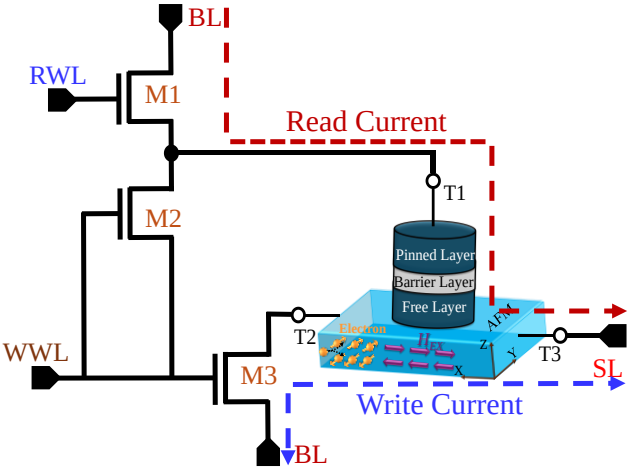


Fig. 2 Proposed 3T–1VGSOT–MTJ MRAM

$$Ratio_{STT}^{\frac{FL}{DL}} = \frac{H_{STT}^{FL}}{H_{STT}^{DL}} \quad (5)$$

$$Ratio_{SOT}^{\frac{FL}{DL}} = \frac{H_{SOT}^{FL}}{H_{SOT}^{DL}} \quad (6)$$

The symbols used in the above formulas are defined as follows: γ is the gyromagnetic ratio, $\vec{m}$is the normalized FL magnetization vector, and $\vec{H}_{EFF}(V_{MTJ})$ denotes voltage-dependent effective magnetic field. The parameter α represents the Gilbert damping constant, H_{STT}^{DL} and H_{STT}^{FL} corresponds to the Damping-Like (DL) and field-like torque of the STT, whereas H_{SOT}^{DL} and H_{SOT}^{FL} represents the respective SOT contributions.

The vectors $\vec{m}_P$ $\vec{m}_\sigma$indicate the pinned-layer magnetization and spin-polarization direction, respectively. Here, $\hbar$, P, J_{STT}, and e denote the reduced Planck constant, spin-polarization factor, STT current density, and elementary charge. In addition, μ_0, M_S, t_f, θ_{SH}, and J_{SOT} represent the vacuum permeability, saturation magnetization, FL thickness, spin Hall angle, and SOT current density, respectively. The parameters$Ratio_{STT}^{\frac{FL}{DL}}$ $Ratio_{SOT}^{\frac{FL}{DL}}$ specify the FL-to-DL torque ratios for STT and SOT, respectively.

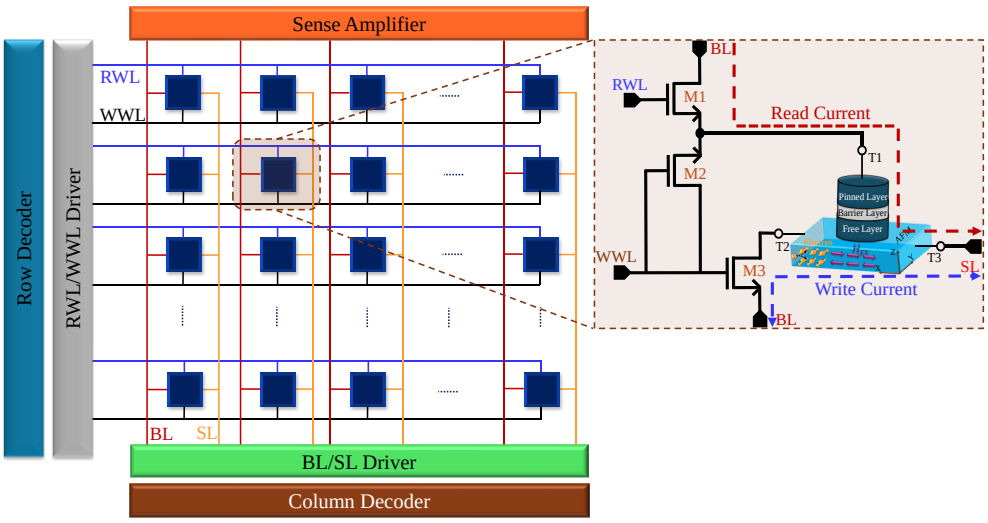


Fig. 3 1Kb MRAM array implemented using the proposed 3T-1VGSOT-MTJ bit-cell

The write operation relies on an in-plane current through the AFM layer, generating a spin current via the spin Hall effect. The resulting spin–orbit torque acts on the FL and drives magnetization reversal. Simultaneously, a positive voltage across the MTJ modifies the FL's perpendicular magnetic anisotropy through the VCMA effect, reducing the energy barrier and potentially lowering the critical switching current. The three-terminal architecture separates read and write paths, limiting read disturbance and supporting data retention. Exchange bias induced by the AFM layer can enable field-free switching under suitable device conditions. These characteristics make VGSOT–MTJs promising for energy-efficient non-volatile memory and logic-in-memory circuits.

3.2. 3T–1 VGSOT–MTJ MRAM

The operating principle and functionality of the proposed 3T–1 VGSOT–MTJ MRAM cell are described in this section. To analyse the circuit behaviour and estimate performance metrics, the complete circuit is designed and simulated in Cadence Virtuoso. Transistors are employed from the GPDK 45 nm library. The electrical behavior of the VGSOT–MTJ is represented using a Verilog–A model and integrated into the Cadence simulation environment. Further, a symbol is created for circuit–level simulation. Figure 2 depicts the circuit schematic of the proposed 3T–1 VGSOT–MTJ MRAM. Read operation is controlled by activating transistor M1 with the help of Read–Word–Line (RWL). Similarly, Write–Word–Line (WWL) activates transistors M2 and M3 for the write operation. Furthermore, SL and BL control the access to the VGSOT–MTJ. In case of read operation, only the transistor (M1) connected to the RWL is active, allowing for sensing current to flow through the VGSOT–MTJ, while the other transistors (M2 and M3) remain OFF. During the write operation, both transistors M2 and M3 are activated through WWL. Transistor M3 allows I_{SOT} to flow through the AFM metal strip to write data into VGSOT–MTJ. Additionally, transistor M2 provides the required voltage at the T1 terminal of VGSOT–MTJ to induce the VCMA effect, which helps to reduce write current. Transistor M1 remains in the OFF condition during the write operation. This selective activation is crucial for efficient memory operation.

For switching from the AP–P state, the WWL voltage of transistors M2 and M3 is maintained at 1 V to enable the VCMA effect and to enable the write path. During this operation, the SL is held at 1 V and the BL is set to 0 V, allowing a current to flow from the SL to the BL through the VGSOT–MTJ, thereby inducing the AP–P transition. In contrast, for switching from the P–AP state, the WWL is again kept at 1 V to activate the access transistor (M2 and M3). However, in this case, the SL is set to 0 V and the BL is set to 1 V. This reversal in voltage polarity causes current to flow in the opposite direction through the MTJ, facilitating the P–AP switching. These specific voltage configurations ensure controlled bidirectional switching of the FL magnetization in the VGSOT–MTJ structure, ensuring successful write operation.

In addition to the 3T–1 VGSOT–MTJ MRAM cell, we have designed a 1–Kb MRAM array using the proposed 3T–1 VGSOT–MTJ cell, as depicted in Figure 3. Since the array is implemented with the proposed MRAM cell, it offers non–volatility along with reduced power consumption due to the VCMA effect of the individual cells. Furthermore, area overhead is addressed by H_{EX}, which eliminates the requirement for an external magnetic field to ensure stable switching operation. Therefore, the MRAM array is suitable for area-constrained IoT applications. In the MRAM array, the row decoder selects the required row, and the column decoder identifies the corresponding bit–cell within that row. The RWL and WWL that are connected to the RWL/WWL drivers activate the access transistors to enable WRITE or READ operations. The BL/SL driver programs the MTJ either in AP or P state, depending on the BL and SL voltage levels for write

operation. The Sense Amplifier (SA) circuit senses the bitline response and accurately determines the stored data, ensuring reliable operation of the array.

The VGSOT–MTJ provides inherent non–volatility, which significantly lowers power consumption, and its compact structure reduces overall area occupancy. Hence, the proposed 1–Kb MRAM array is well–suited for IoT applications where low–power operation and small footprint are critical requirements.

4. Performance Metrics

The performance of the proposed 3T–1 VGSOT–MTJ-based single-bit MRAM cell is assessed in terms of its principal design metrics and benchmarked against representative state-of-the-art MRAM architectures. Furthermore, a comprehensive analysis is carried out to examine how the switching energy and delay of the VGSOT–MTJ device vary with free layer thickness, MTJ diameter, input voltage, and *eta* – each of which significantly influences the magnetization dynamics and torque efficiency. For instance, reducing the thickness of the free layer decreases switching time due to a lower energy barrier but may compromise thermal stability. Increasing the MTJ diameter enhances reliability through improved spin current injection but results in higher energy consumption. Additionally, tuning the eta enables control over the torque exerted on the free layer, directly influencing switching latency and energy performance. The switching delay is measured by systematically varying the free layer thickness across a practical range, revealing the tradeoffs between speed and switching performance. The MTJ diameter is also swept, with observations showing a nonlinear relationship between device size and switching delay. Furthermore, input voltage scaling experiments demonstrate how lower voltages favour energy efficiency but may degrade switching–a crucial concern for low–voltage IoT devices.

The transient magnetization behavior of the FL for AP–P and P–AP state transitions is presented in Figure 4. The proposed 3T–1 VGSOT–MTJ cell is investigated under multiple input-voltage conditions to characterize the resulting variation in its switching dynamics. Notably, the cell demonstrates successful switching at a lower input voltage of 0.4 V for the AP–P transition, while the P–AP transition requires a minimum input voltage of 0.6 V.

The corresponding switching delays are also reduced as depicted in Figure 8(a), measured at 3.43 ns and 3.31 ns for AP–P and P–AP transitions, respectively. This is due to the three–terminal configuration, which isolates the read and write operations, ensuring efficient torque transfer and enabling mz switching at reduced input voltages.

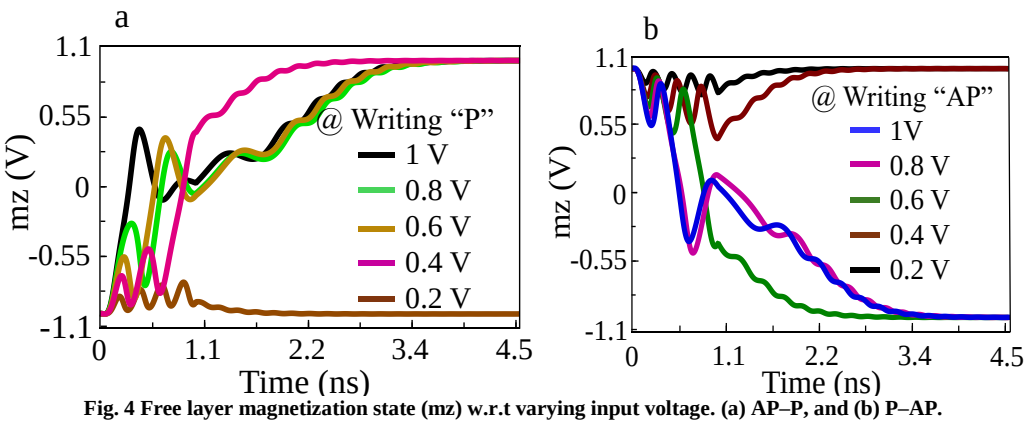


Fig. 4 Free layer magnetization state (mz) w.r.t varying input voltage. (a) AP–P, and (b) P–AP.

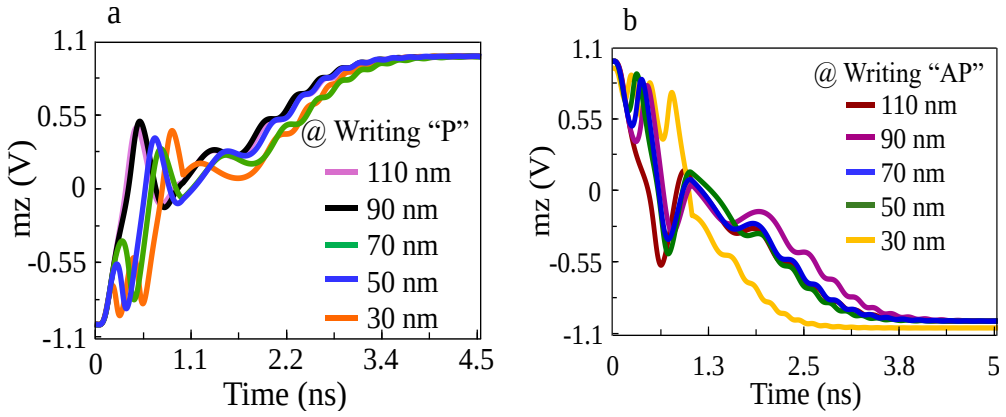


Fig. 5 Free layer magnetization state (mz) w.r.t varying MTJ diameter. (a) AP–P, and (b) P–AP.

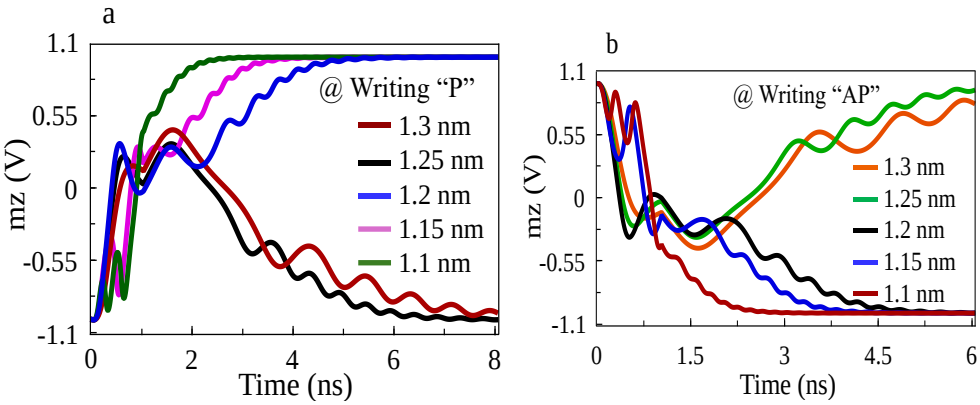


Fig. 6 Free layer magnetization state (mz) w.r.t varying FL thickness. (a) AP–P and (b) P–AP.

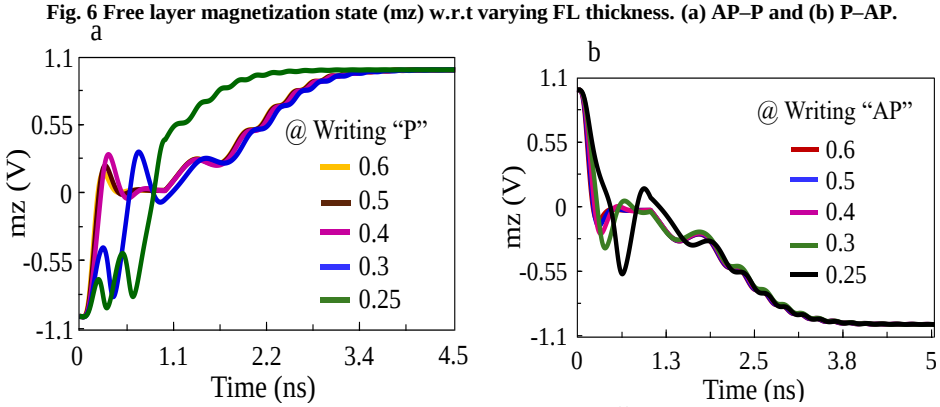
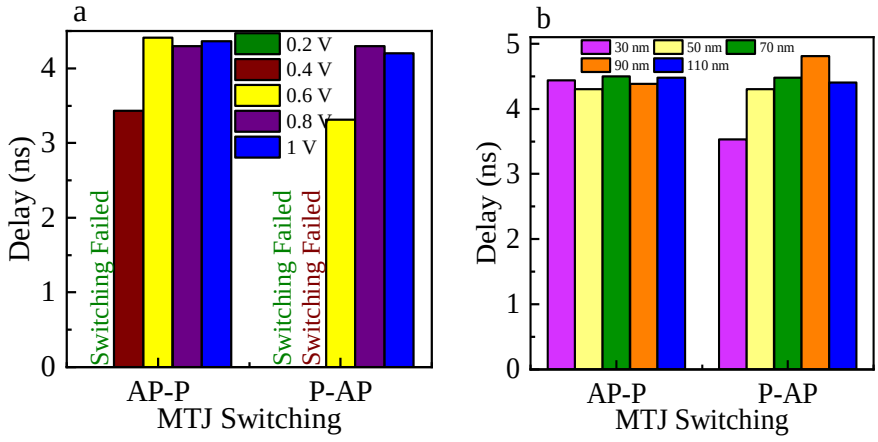


Fig. 7 Free layer magnetization state (mz) w.r.t varying spin hall effect (*eta*). (a) AP–P and (b) P–AP.

Moreover, the diameter of the VGSOT–MTJ is varied to evaluate AP–P and P–AP switching behavior in the MRAM cell. As illustrated in Figure 5, the VGSOT–MTJ successfully achieves switching across different diameters for AP–P and P–AP configurations. In addition to that, in the 3T–1 VGSOT–MTJ cell, AP–P switching shows a non–uniform delay trend with diameter scaling due to variations in current density, edge effects, and thermal instability. Delay decreases initially, rises at intermediate sizes, and fluctuates due to non–linear magnetization dynamics. In contrast, P–AP switching shows a smooth, gradual reduction in delay from 90 nm to 30 nm, as depicted in Figure 8(b). This consistent behavior suggests greater stability and efficiency in P–AP transitions under diameter scaling.

Additionally, the FL thickness of the VGSOT–MTJ is varied to evaluate its impact on switching behavior for AP–P and P–AP transitions, as shown in Figure 6. Notably, at a lower FL thickness of 1.1 nm as depicted in Figure 8(c), successful switching is achieved with delays of 3.27 ns and 3.31 ns, respectively. Beyond this, at 1.25 nm, switching fails altogether, suggesting that increased FL thickness hinders the torque effectiveness required for reliable state transitions. Furthermore, the Spin Hall Effect parameter of the VGSOT–MTJ is varied to analyze its influence on the switching dynamics of the proposed MRAM cell. As shown in Figure 7, variations in *eta* do not result in a significant change in the switching delay, as illustrated in Figure 8(d).



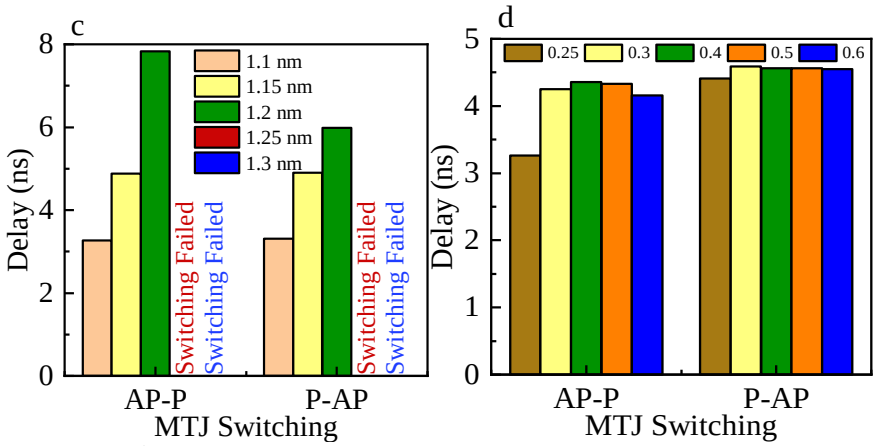


Fig. 8 Switching delay for variation in (a) Input voltage, (b) MTJ Diameter, (c) Free layer thickness, and (d) *eta*.

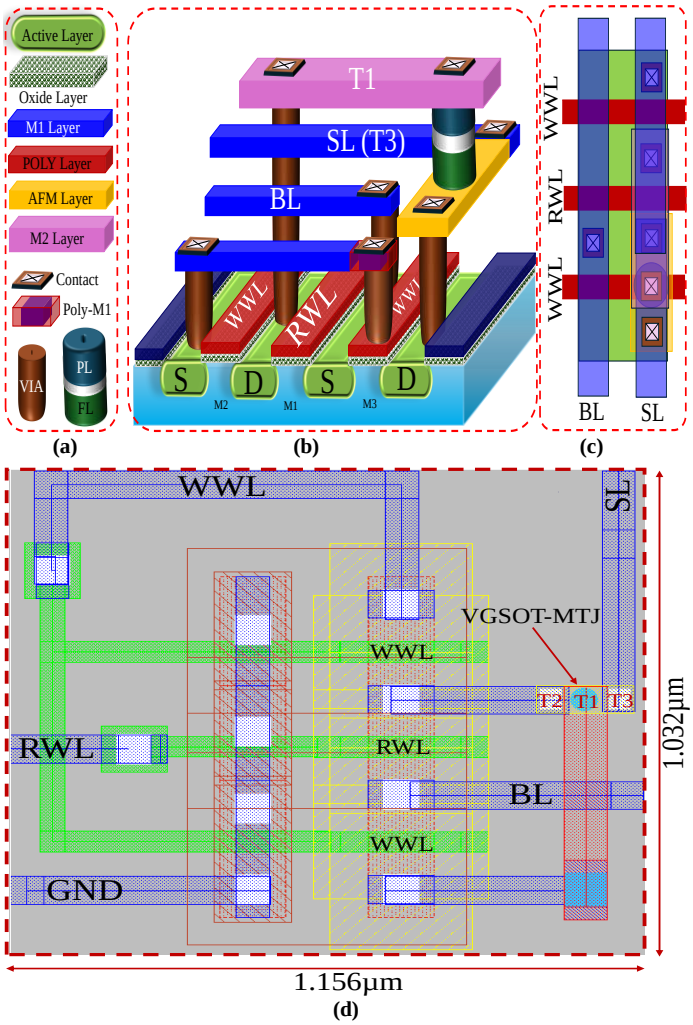


Fig. 9 A 3T–1VGSOT–MTJ based MRAM (a) Layers detail, (b) 3D view, (c) Top view, and (d) Layout view with an area of 1.193µm^2.

This behavior can be explained by the fact that, for the applied write current, the spin–orbit torque generated via the *eta* is already sufficient to ensure reliable magnetization switching [27]. As a result, further increases in *eta* yield only marginal improvement in switching speed, and the switching delay becomes weakly dependent on *eta* since torque is no longer the limiting factor. Instead, the switching delay is predominantly governed by intrinsic magnetic parameters such as the damping constant, effective magnetic anisotropy, and thermal effects.

Table 2. Comparison of MTJ–based single MRAM bit–cell performance metrics

			Liu et al. [18]	Sarkar et al. [25] (Redesigned)	Wu et al. [26] (Redesigned)	Proposed work
Switching direction	AP-P	Power (µW)	-	26.19	30.45	18.1
		Delay (ns)	-	3.5	4.21	2.3
		Energy (fJ)	340	91.66	128.2	41.63
	P-AP	Power (µW)	-	24.61	21.55	15.5
		Delay (ns)	-	3.11	4.98	2.2
		Energy (fJ)	289	76.54	107.32	34.1
Count			3T-1SOT-MTJ	4T-1VGSOT-MTJ	2T-1SOT-MTJ	3T-1VGSOT-MTJ

Table 2 presents the performance metrics of the proposed 3T–1 VGSOT–MTJ MRAM cell. The performance metrics, including delay, power, and energy, are evaluated using transient analysis of the proposed MRAM cell in Cadence Virtuoso at the 45 nm technology node. The write delay for storing AP–P and P–AP in the MRAM cell is determined by the time taken by the z–component of the magnetization (*mz*) to settle at a stable logic '1' or logic '0'. This approach enables an accurate estimation of write latency for both switching directions based on the actual magnetization dynamics of the device. The write power is obtained by multiplying the applied input voltage by the total current drawn by the circuit during the write operation. Finally, the write energy is calculated as the product of the measured power and the corresponding switching delay.

Notably, the design demonstrates a significant reduction in energy consumption during switching operations. For AP–P switching, the proposed cell achieves an 87.76%, 54.58% and 67.53% reduction in energy consumption at BL = 0 V and SL = 1 V when compared to [18, 25, 26]. Likewise, for P–AP switching at BL = 1 V and SL = 0 V, an 88.20%, 55.45% and 68.23% reduction in energy consumption is observed relative to [18, 25, 26]. These results highlight the superior energy efficiency of the proposed architecture under standard write conditions. The improved energy efficiency can be attributed to the voltage–assisted switching characteristics of the VGSOT–MTJ device and the optimization of key device parameters. The VGSOT–MTJ enables efficient magnetization switching through voltage–assisted control, where the voltage at the T1 terminal modulates the interfacial magnetic anisotropy via the voltage–controlled magnetic anisotropy effect, thereby lowering the SOT write current required for switching. In addition, tuning the input voltage, MTJ diameter, free–layer thickness, and *eta* helps achieve low–power operation with reduced switching delay, making the proposed architecture suitable for compact and high–speed IoT applications.

In addition to analyzing the switching behavior, the layout of the proposed 3T–1VGSOT–MTJ cell is designed as shown in Figure 9 using λ–design rules. Representation of diffusion layers, MTJ layers, contacts, metal layers, and vias is presented in Figure 9 (a), respectively. Furthermore, Figure 9 (b) represents the 3D view that shows the vertical integration of the VGSOT–MTJ above the underlying CMOS transistors, along with the routing of the SL and BL. Figure 9 (c) shows a top view representing the planar arrangement of the three transistors with a shared diffusion region, along with the placement of the read and write word–lines and the vertical routing of the bit–line and source–line that establish the required current paths for operation. The final layout is shown in Figure 9 (d), which occupies an area of 1.193 μm^2. This rule–aware implementation supports compatibility with conventional fabrication processes, improves electrical reliability, and enables integration with existing CMOS back–end flows. Nevertheless, the compact layout is optimized for area efficiency, making it well–suited for dense, low–power IoT applications. Compared to conventional STT and SOT–MRAM designs, the VGSOT–MTJ–based MRAM cell achieves notable reductions in both power and energy consumption with minimal area overhead.

5. Conclusion

The proposed work presents a 3T–1 VGSOT–MTJ–based MRAM bit–cell and a 1 Kb MRAM array architecture, targeting energy-efficient and high–speed memory operations. A comprehensive analysis was performed by varying key device parameters, including the nanopillar diameter of the VGSOT–MTJ, FL thickness, *eta*, and input voltage. These variations allowed for a detailed understanding of the impact of physical and electrical parameters on the overall device performance. Among the different configurations analyzed, the proposed structure achieved a minimum write delay of 2.2 ns for an input voltage of 0.8 V and *eta* = 0.25, demonstrating improved switching speed under optimized conditions. Additionally, the 3T–1VGSOT–MTJ design showed significant energy efficiency when compared with the existing MRAM architecture. Specifically, 34.29% and 45.37% reduction in delay observed for AP–P switching. Similarly, for P–AP, the delay is reduced by 29.26% and 55.82%, respectively. For AP–P switching, the proposed cell achieves 87.76%, 54.58%, and 67.53% reduction in energy consumption compared with existing designs. Similarly, for

P–AP switching, energy consumption is reduced by 88.20%, 55.45%, and 68.23% compared with the corresponding existing designs, respectively. These improvements highlight the suitability of the proposed MRAM design for low–power embedded memory systems and energy–constrained applications. These results establish the 3T–1 VGSOT–MTJ MRAM as a highly efficient and high–speed alternative, making the proposed architecture suitable for future non–volatile memory systems.

Conflicts of Interest

The authors declare that there is no conflict of interest regarding the publication of this paper.

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