SSRG International Journal of Electronics and Communication Engineering
ISSN: 2348-8549/ https://doi.org/10.14445/23488549/IJECE-V13I11P125

Volume 13 Issue 11, 398-407, November 2026
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Original Article

Design of 9T Read-Decoupled SRAM Cell with a Controllable Footer Transistor (CFT) for Machine Learning based PDP Optimization

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Received: 11 September 2026 Revised: 05 November 2026 Accepted: 17 November 2026 Published: 27 November 2026

Abstract *- In this paper, the CF-9T SRAM has been simulated in 180 nm CMOS technology. SPICE simulations were carried out by varying V_{DD}, V_{FG}, temperature and transistor sizes to generate a total of 600 dataset. Here, a Controllable-Footer 9T (CF-9T) SRAM cell is proposed by adding a footer NMOS transistor to an 8T SRAM cell. The proposed footer adds a new control parameter, V_{FG}, to enhance the power-delay characteristics of the SRAM cell. The standard ML models like Stacking Ensemble, Random Forest, SVR-RBF, and XG Boost has been created to predict write and read PDP from nine circuit-level input variables. The proposed cell has got a read and write delay of 0.0049 ns and 0.1184 ns. The comparable PDP value of read and write was 1.05 X 10^{-20} J and 2.06 X 10^{-16} J correspondingly. The evaluation of the ML models was made by R^2, RMSE and MAE. The prediction results demonstrate good agreement between simulated and predicted PDP values. The proposed CF-9T SRAM attains a 69.92% mitigation in read PDP and a 32.90% mitigation in write PDP compared with the existing 9T SRAM cell. The combination of CF-9T cell and ML-based prediction suggested in this work provides an effective way to analyze and optimize SRAM power-delay performance under wide range of operating situations.*

Keywords *- SRAM, PDP, Machine Learning, Circuit simulation, Power.*

1. Introduction

Static Random-Access Memory (SRAM) is a basic building element of recent System-on-Chip (SoC) designs and is widely utilized in cache memories, embedded processors and Internet of Things (IoT) devices. With the increasing use of memory in modern integrated circuits, the power consumption and performance of SRAM cells are becoming key aspects in the overall energy efficacy and speed of a system [1]. SRAM cells are required to operate with less power consumption and maintain acceptable read/write speed, data stability and reliable operation. Therefore, simultaneous power and delay optimization is still a big issue for SRAM design. Recent SRAM research explores other transistor topologies, power gating schemes, read decoupling techniques, and low voltage operation to get a better tradeoff between power, delay, stability, and energy efficiency [2]. Therefore, an SRAM architecture that enhances the read operation robustness and at the same time allows an efficient optimization of the PDP is desirable for energy-constrained computing applications.

The 6T-SRAM cell is an implementation of two cross-coupled CMOS inverters with two access transistors. However, the same access path is typically used for both read and write, resulting in a basic tradeoff between read and write capabilities. During a read operation, the bit-line access path may disturb the internal storage node. During a write operation, the cell must resist the feedback of the cross-coupled inverter. These limits become more important as the supply voltage is scaled because it can impact both stability and performance. To solve these problems, numerous multi-transistor SRAM cells have been developed, such as 7T, 8T, 9T and SRAM cells with more transistors [3, 4]. The read decoupled 8T architectures can enhance read, and additional transistors can be employed for write assistance, power gating, and leakage control. However, adding more transistors can also add size, capacitance, and control complexity, so the extra devices need to deliver a significant performance boost.

Another effective method to manage the current route of an SRAM cell is to use power-gating and virtual-ground techniques [5, 6]. A transistor can be put between the cell and ground supply in such configurations to make a virtual-ground node. The discharge ability of the cell and hence the leakage current, dynamic power and switching delay depend

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on the state of this transistor. Virtual ground and power gating techniques have previously been shown to be effective for increasing the energy efficacy and the operational characteristics of SRAM cells. However, the performance of a footer-controlled SRAM is very sensitive to the electrical state of the footer device. Therefore, the control voltage of the footer transistor is another design element that can be used to trade off the conflicting requirements of power and performance.

A CF-9T SRAM cell where an extra NMOS transistor (M_9) is added to the ground path of an 8T SRAM core has been presented. M_9 source is connected to ground, and its drain is connected to the Virtual Ground Node of the SRAM core (V_{GND}). The gate of M_9 is driven by a special Footer-Control Voltage (V_{FG}). The suggested architecture thus gives an extra degree of control over the current path between the SRAM core and ground. By changing (V_{FG}), the conduction strength of the footer transistor may be tuned, which provides a trade-off between power consumption and operating delay [7].

The joint effect of supply voltage, transistor sizing, and footer-control voltage on the PDP of the CF-9T SRAM cell is unexplored. ML based methods have been used to forecast the performance of SRAM. Finding the proper operating points that result in a good power-delay trade-off is still a challenge. The present work analyzes the feasibility of multiple machine learning regression models in forecasting the PDP and finding a proper operating region of the CF-9T SRAM cell.

Circuit-level simulation is a useful way to evaluate SRAM performance. The performance of SRAM is affected by various interrelated elements such as supply voltage, transistor size, footer-control voltage and operating conditions. The ensuing relationship between these parameters and performance indicators, such as power and latency, is significantly non-linear [8]. Khorrami and Nabavi used deep learning models to estimate the effect of process variation and device aging on the performance parameters of a standard 6T SRAM cell [9]. Sharma and Chandel, in their previous work, used variation-aware modeling to optimize speed and yield of 6T SRAM designs under multiple process and operating variations [14]. The results of these investigations show the ability of predictive modeling to analyze SRAM performance.

Conventional parameter sweeping can only find an optimum inside the chosen simulation grid, and may need a significant number of simulations. Thus, a data-driven surrogate modeling is an interesting way to reduce computing cost of recurrent circuit simulations. Recently, the viability of SRAM characteristics prediction under process, voltage and temperature using machine learning algorithms has been shown. In this work, the link between the key parameters of the proposed CF-9T SRAM cell and its Power-Delay Product (PDP) is studied with Ensemble Stacking Regression (ESR), Random Forest Regression (RFR), Extreme Gradient Boosting (XGBoost) and Support Vector Regression (SVR) Radial Basis Function (RBF) kernel models. The ML models are trained on a dataset generated from circuit-level simulations, and their prediction accuracy is evaluated using pertinent statistical measures like Coefficient of Determination (R^2), Mean Absolute Error (MAE) and Root Mean Square Error (RMSE) [10]. The best one is then used to find an operational region that minimizes the PDP. The paper is organized as: In Section 2, the architecture of the proposed CF-9T cell with its functions are described. In section 3 comprises details of the simulation process and how metrics such as power, delay and PDP have been extracted. Section 4 elaborates on the machine learning technique and discusses the dataset generation, preprocessing, model building, and performance of the Ensemble, Random Forest and XGBoost models. Simulation and ML-based optimization findings are shown in Section 5. The suggested cell is compared with existing SRAM. Lastly, Section 6 ends the work and advises possible paths for future research.

2. Proposed 9T SRAM Cell

The proposed cell is a 9T SRAM design, which consists of an 8T SRAM core and an extra adjustable footer transistor M_9. The 8T core consists of the cross-coupled inverter pair of PMOS transistors M_1 and M_2 and NMOS transistors M_3 and M_4. M_1-M_4 supply the regenerative storage mechanism and are used to hold complementary data at the internal nodes Q and Q_B. Transistors M_5-M_8 are used for write-access and read-interface functions between the storage core and the bit-line circuitry [11]. The extra transistor M_9 is an NMOS footer transistor linked between the virtual ground node V_{GND} and the real ground wire. The gate of M_9 is controlled by the dedicated voltage V_{FG} for the footer control. M_9 therefore offers an electrically controlled channel to ground for the core current of the SRAM. The controlled V_{GND} route provides an additional degree of freedom to trade off power consumption and circuit delay. Figure 1 represents the proposed 9T-SRAM.

The size of the transistors of the proposed CF-9T SRAM cell is chosen as follows. The pull-up transistors PU1 (M_1) and PU2 (M_2) are PMOS with a W/L ratio of 2.104. The pull-down transistors PD1 (M_3) and PD2 (M_4) are NMOS transistors with W/L ratio of 2.0. The access transistors AX1 (M_5) and AX2 (M_6) are NMOS transistors with a W/L ratio of 1.333. The read-access transistor M_7 is an NMOS device with W/L = 1.0, whereas the read pull-down transistor M_8 has width 0.270 µm and channel length 0.18 µm. An extra NMOS Footer Transistor (MFG) for Adaptive Virtual-Ground (VGND) control is employed with a width of 0.360 µm and a channel length of 0.18 µm, resulting in a W/L ratio of 2.00. All nine transistors possess a channel length of 0.18

µm, and their widths are chosen according to their circuit roles. The TSMC 180 µm library is used for simulation. During hold operation, the WL and RWL are disabled, and the M_1-M_4 is able to hold the recorded data. The M_5-M_8 are still in their respective idle states to insulate the storage nodes from undesirable bit-line interruptions. V_{FG} sets the status of M_9, which sets the strength of the virtual-ground connection. For a write, WL is enabled to allow the access transistors to be turned on and the bit-line-to-cell current path to be established. In a Write-0 operation, the selected bit line is driven low while the corresponding bit line is driven high. The access transistors transmit write state to Q and Q_B correspondingly. The low state at the specified storage node is set by the pull-down NMOS transistor of the inverter pair. M_9 supplies the return path from V_{GND} to ground and also impacts the strength of the cell discharge current. Therefore, V_{FG} can influence the write current and the time required to accomplish the Write-0 transition. In a Write-1 operation, the complementary bit-line condition flips the voltage state of Q and Q_B.

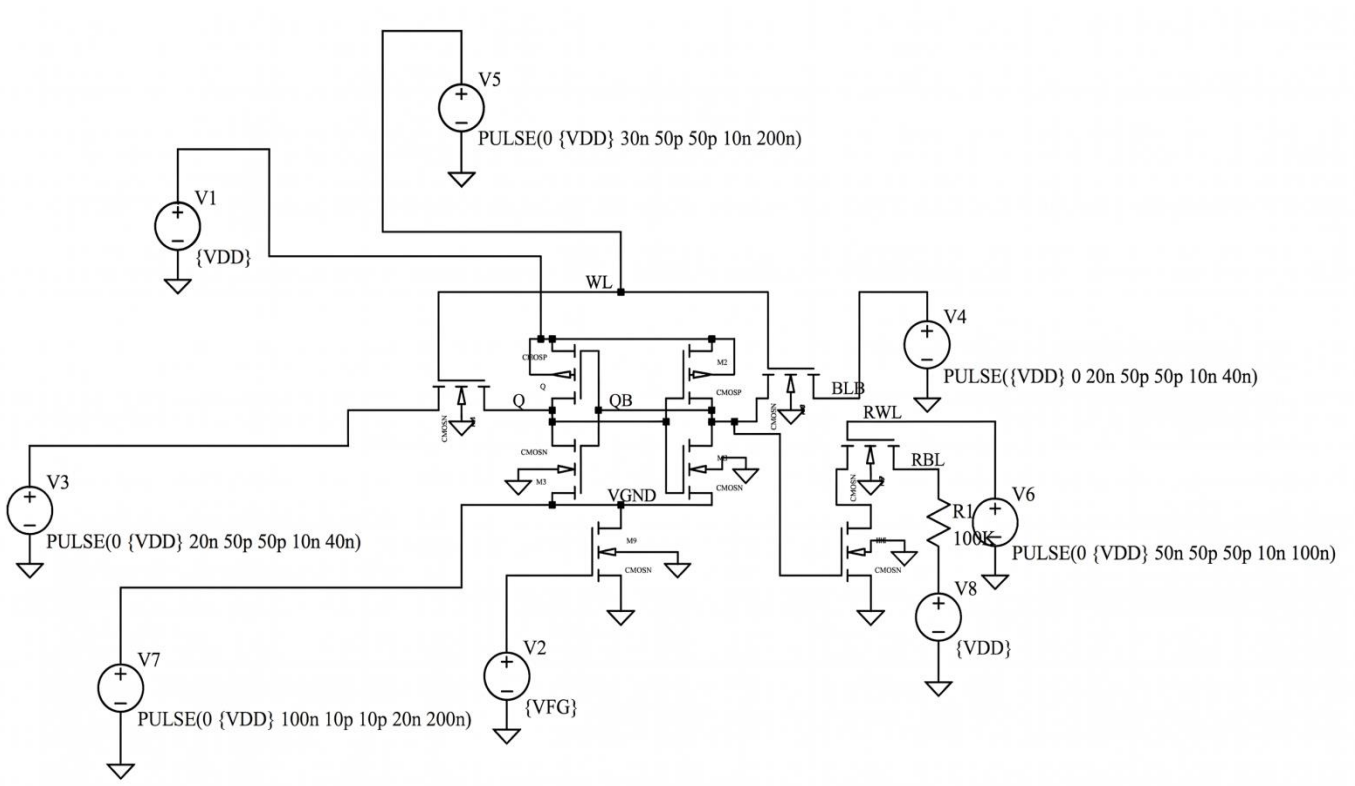

Fig. 1 Schematic of proposed 9T-SRAM

The access transistors enable the externally applied data to overcome the regenerative feedback of the cross-coupled inverters. The footer transistor M_9 is used to manage the effective ground path during this switching process and so is an influence on write latency and power.

For read operation, RWL is asserted to enable the specialized read path provided by respective read transistors of the 8T core. The stored data in internal node governs the read stack and dictates the discharge behavior of RBL. The read path is decoupled from the feedback path of the main storage so that the read operation can relieve direct disturbance of Q and Q_B. In the proposed topology, M_6 and M_8 are involved in the read-stack process, M_5 and M_7 offer the respective access functionalities [12]. Figure 2 depicts the output waveform.

Thus, stored data, transistor sizing, supply voltage and footer state effect the read current and read delay. M_9 also changes the effective current path through V_{GND}, and hence influences both the dynamic power and the delay of memory operation. Therefore, the footer-control voltage V_{FG} in the proposed CF-9T cell is regarded as a key design element. Varying V_{FG} allows obtain varied power–delay operating points without modifying the core 8T storage structure. The proposed architecture is characterized by SPICE simulations for hold, read, Write-0 and Write-1 operations. The calculated power and delay data are utilized to create the power–delay product and construct the dataset for Ensemble, Random Forest, SVR-RBF and XGBoost models. Then, the ML models are applied to search for a good V_{FG} and circuit-parameter combination so that PDP is minimized with the SRAM operating properly [13, 14].

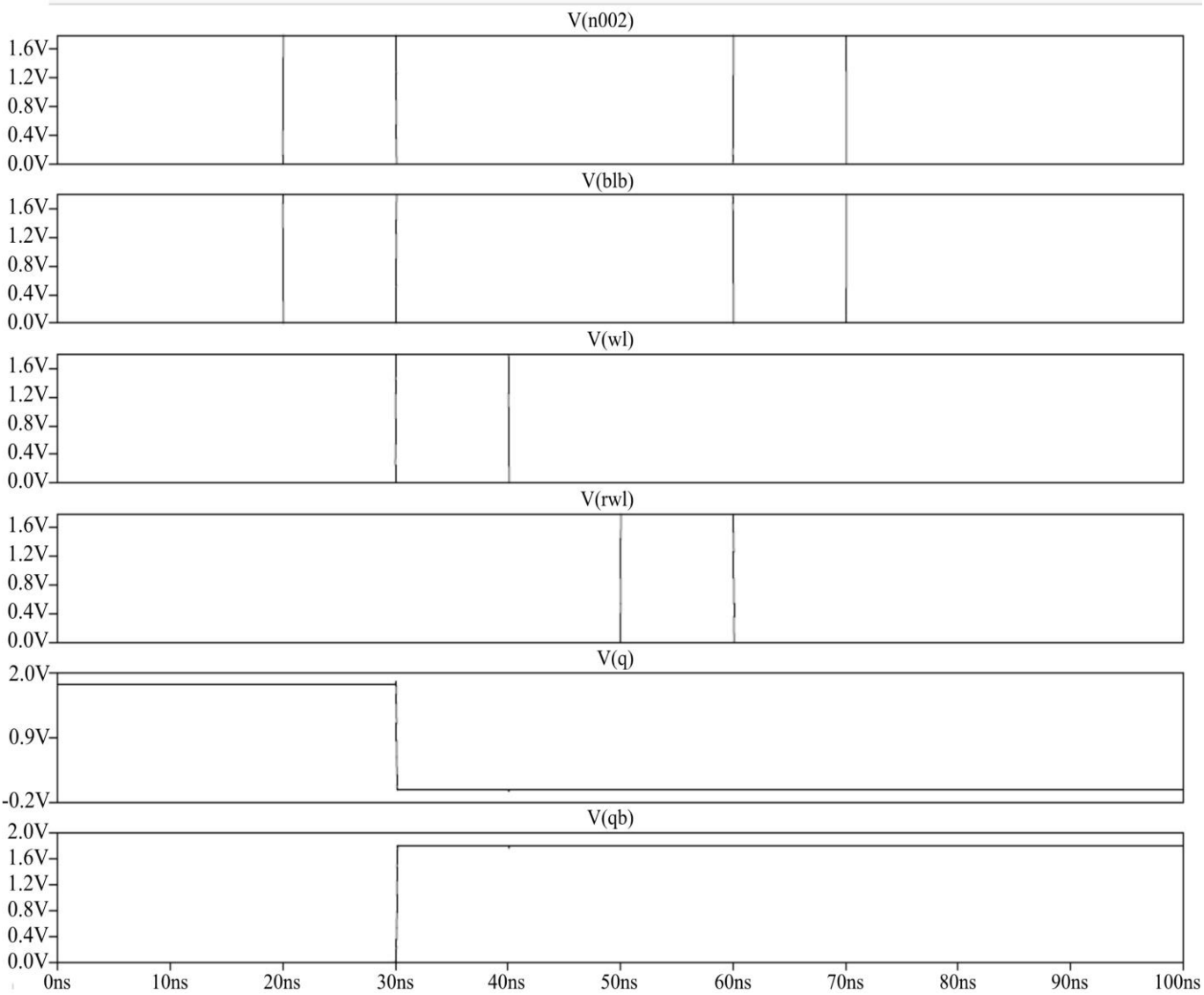

Fig. 2 Output of 9T-SRAM

3. Simulation Methodology

The PDP of the proposed CF-9T cell are characterized using circuit-level transient simulations. The proposed design shows the implementation of the circuit using CMOS transistor models in the SPICE simulation environment. The 9T cell consists of the regular 8T SRAM core plus the extra NMOS footer transistor M_9 controlled by the Voltage (V_{FG}). Transient simulations are done for the four basic working situations of the SRAM: hold, Write-0, Write-1 and read. WL, RWL, BL and BLB are excited using proper pulse sources to implement the desired memory operations.

The storage node is initialized before each transient operation so that it can obtain reproducible simulation results. The write procedure consists of applying complementary data signals to BL and BLB. The WL is activated for the desired write interval. For the read operation, RWL is enabled, and the read discharge path is determined by the data stored. The footer-control signal (V_{FG}) is applied to the gate of M_9 separately to control the virtual-ground connection of the SRAM core.

The V_{FG} is a crucial factor to regulate the functioning of the proposed CF-9T SRAM cell. The footer transistor is connected between the V_{GND} and the actual ground terminal. The gate overdrive voltage of the footer transistor is increased, which results in stronger conduction and lessening the voltage difference between V_{GND} and ground. Therefore, the virtual-ground voltage approaches zero, allowing the SRAM cell to operate closer to its usual ground-referenced condition. It may improve the discharge ability of the internal nodes and decrease the read delay. During a write operation, increased footer conduction can impact the voltage levels at the storage nodes and the write margin.

Conversely, a reduction in V_{FG} reduces the conduction of the footer transistor, and so V_{GND} rises due to the voltage drop across the footer device. This may decrease the effective voltage across the SRAM cell and mitigate leakage current. However, too much reduction in V_{FG} may increase read/write latency and degrade cell stability. Thus, choosing a suitable footer-control voltage is important for balancing leakage reduction, read/write performance, and SRAM stability.

A parametric simulation is carried out by altering V_{DD}, V_{FG} and selected transistor sizes within stated design ranges. For each set of parameters, the transient response of the SRAM cell is captured and examined. Similarly, read latency is dictated by the propagation of the stored data to the read bit line. The delay measurements are done by finding the 50% (V_{DD}) crossover points of the associated input and output waveforms. Read PDP and Write PDP are examined respectively to distinguish the performance of the two major memory operations. To find the effect of M_9 on the power–delay tradeoff, the simulations are run for different (V_{FG}) values. The generated simulation data is collected in a structured dataset comprising the circuit parameters and the relevant metrics for performance. Each dataset sample is comprised of the selected input parameters and the power, delay, and PDP values obtained from SPICE. The resulting dataset is split into training and testing subsets for later machine-learning analysis. The nonlinear association between circuit parameters and PDP is established based on the training data. Then the resulting simulation data is used to train the models of ESR, RFR, SVR-RBF and XGBoost Regression. The performance of the model is measured with statistical metrics, namely R^2, MAE and RMSE. The highest-performing model is then used to predict PDP over the explored design space and to indicate promising operating circumstances [15].

Finally, another SPICE simulation is performed to validate the ML-predicted optimum, which confirms the prediction accuracy and the functional functioning of the CF-9T SRAM cell. Figure 3 depicts the overall framework of 9T-SRAM using machine learning.

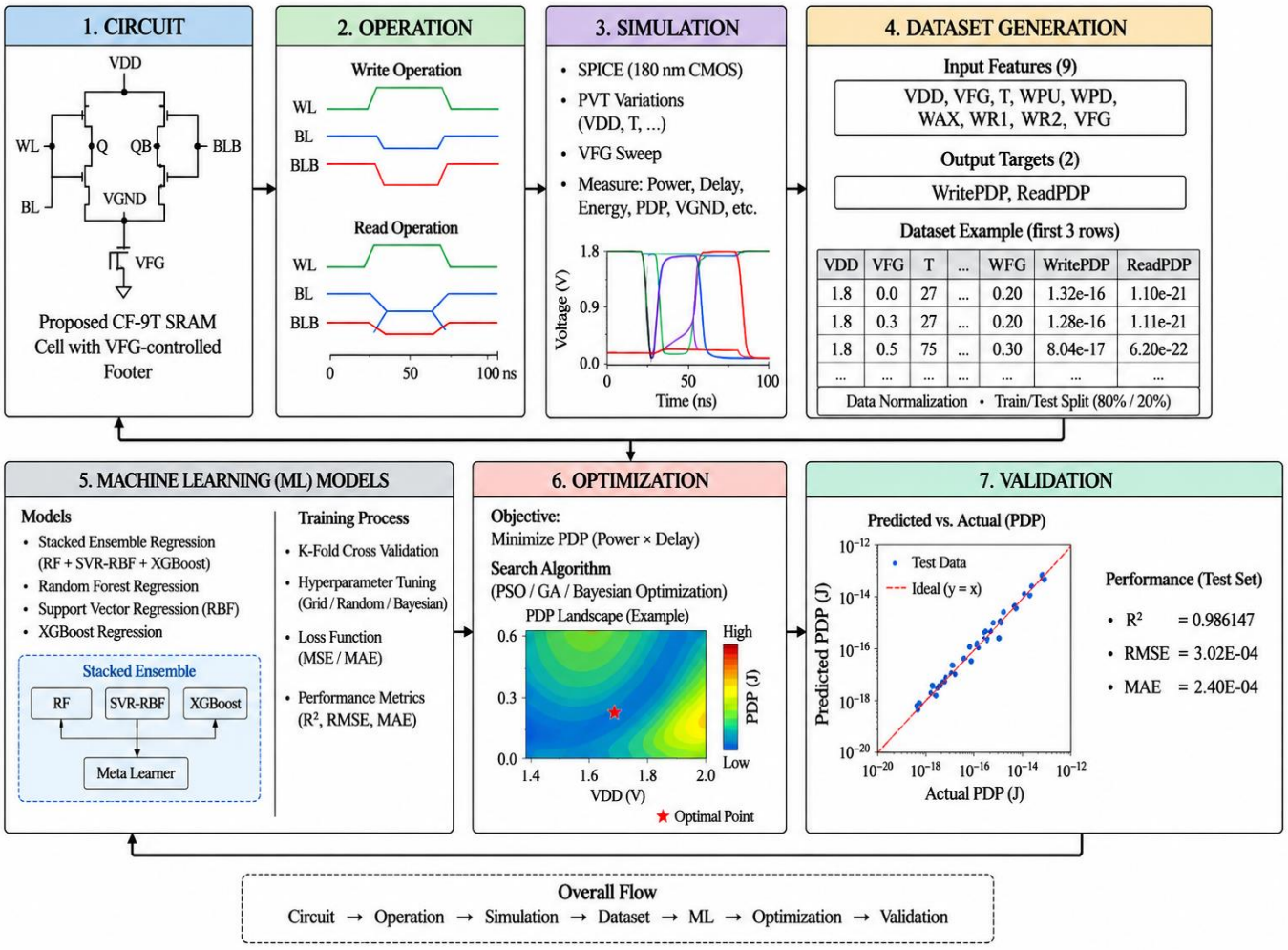

Fig. 3 Machine learning framework of proposed 9T- SRAM

4. Dataset Generation

The machine learning dataset is built from the SPICE simulations of the proposed CF-9T cell at the transistor level. The primary aim of dataset generation is to create a relationship between the design parameters of the SRAM and its Power–Delay Product (PDP). The input parameters used are the Supply Voltage (V_{DD}), Footer-Control Voltage (V_{FG}), temperature and the size of the transistors. For each combination of input parameters, a transient SPICE simulation for the needed SRAM operations is performed. The average power and propagation delay are obtained from the simulated waveforms. The generated dataset contains one row for each unique simulation condition and the related performance response.

The simulation dataset is obtained via systematic variation of the supply voltage, footer-gate voltage, the temperature and transistor sizing of the proposed CF-9T cell. Five configurations of transistor sizing were studied. V_{DD} changed from 1.62 V to 1.98 V in five steps, V_{FG} varied from 0 V to 0.7 V in 0.1V increments, and temperature was evaluated at −40°C, 27°C and 85°C. The transistor widths varied in the following ranges: W_{PU} from 0.27 to 0.48 µm, W_{PD} from 0.27 to 0.45 µm, W_{AX} from 0.18 to 0.30 µm, W_{R1} from 0.18 to 0.30 µm, W_{R2} from 0.27 to 0.45 µm, and W_{FG} from 0.18 to 0.54 µm. For each combination of transistor-sizing configuration, supply voltage, footer-gate voltage, and temperature, transient SPICE simulations were performed. Thus, 600 simulation samples in total were created. The general dataset structure is ([V_{DD}, V_{FG}, T, W_{PU}, W_{PD}, W_{AX}, W_{R1}, W_{R2}, W_{FG}] as input features and [write PDP, read PDP]) as output features.

The generated data are checked for missing values, faulty simulation points and unexpected findings before training. Simulation samples that describe unsuccessful SRAM operations are removed from the regression data set as constraint violations during optimization. The valid data set is then separated into training and testing to assess the capabilities of ML algorithms. The ML framework includes four regression methods, namely ERS, RFR, SVR-RBF and XGBoost Regression.

The circuit and operational parameters collected from the SPICE simulation are fed to the input layer of the framework. The simulated PDP is used as target variable, power and delay can be treated as independent target variables. The Ensemble model integrates the predictions of numerous learners to improve the robustness of prediction and reduce the dependency on individual models. The RFR model creates numerous decision tree models by using random samples and features and then averages their predictions for regression. The XGBoost model uses gradient boosting to build decision tree models sequentially to minimize prediction errors. The training dataset is utilized for each model to learn the nonlinear association between the input parameters and PDP. The performance of the trained models is assessed by R^2, MAE and RMSE [10]. The model with highest predictive accuracy and lowest error is selected as surrogate model for PDP optimization. Then, feature significance analysis can be performed to assess the relative influence of V_{FG} and transistor size on PDP. Thus, the predicted response is used to execute an optimization search to find the parameter combination with smallest PDP. The ML prediction is then verified using an independent SPICE simulation of the predicted optimum. To validate the accuracy of the proposed ML learning system, the simulated and ML-predicted PDP values are compared. This SPICE-ML-SPICE methodology provides an effective computational way to optimize the controlled footer voltage and other design parameters of the proposed CF-9T SRAM cell.

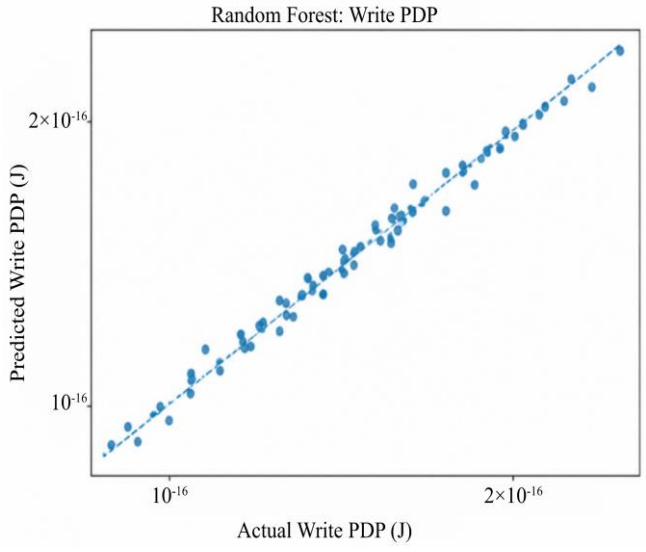

Fig. 4 (a) Actual vs. predicted PDP in case of RFR

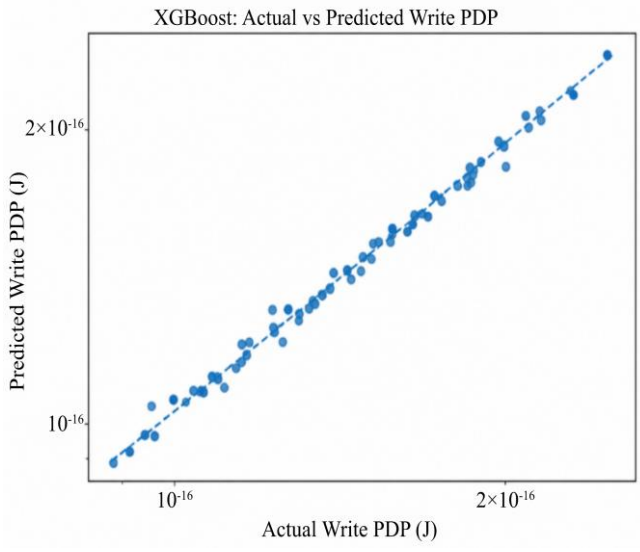

Fig. 4 (b) Actual vs. predicted PDP in case of XGBoost

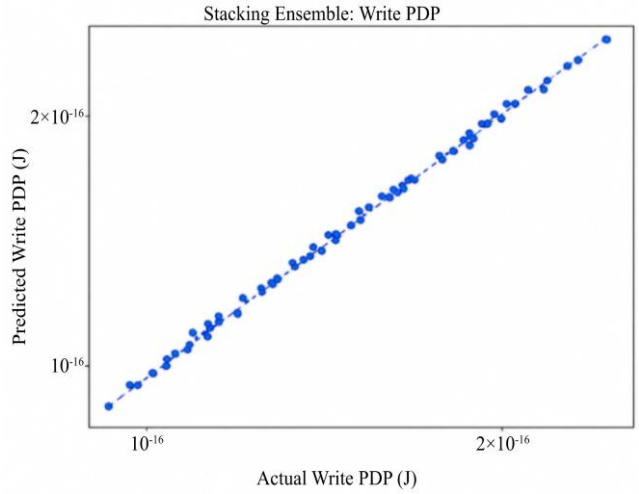

Fig. 4 (c) Actual vs. predicted PDP in case of ESR

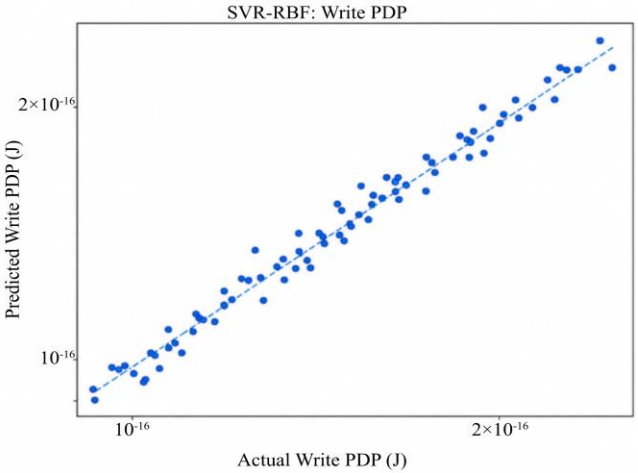

Fig. 4 (d) Actual vs. predicted PDP in case of SVR-RBF

5. Machine Learning Models

Four supervised regression models are used to estimate the PDP of the presented CF-9T SRAM cell, including RFR, XGBoost, ERS and SVR-RBF. These models are selected since they can capture the nonlinear relationship between the circuit characteristics like V_{DD}, V_{FG}, transistor size and the resultant SRAM performance. RFR is a regression method based on several decision tree models as an ensemble learning method. The final prediction is the average of the predictions from the various trees. The proposed SRAM optimization employs the RFR to model the nonlinear link between the circuit input parameters and the PDP produced from SPICE. The model is somewhat resilient to nonlinear parameter interactions and can also provide feature importance information, which helps to find the parameters with the greatest impact. Regression using XGBoost is a decision-tree-based gradient boosting algorithm. It builds trees iteratively to reduce the prediction error of the previous learners. This allows XGBoost to learn complex nonlinear interactions between V_{DD}, V_{FG}, transistor sizes and PDP. The ML algorithms were implemented in Python with the Scikit-learn module. Min-Max Scaler was utilized for feature scaling. The XGBoost model was set with 300 estimators (trees) and a learning rate of 0.05 for stable and gradual boosting. The maximum tree depth of 6 was used. A subsampling ratio of 0.8 and random state of 42 was used. The SPICE-produced dataset is used to train the model, and with proper hyperparameter optimization, the model is taught to predict the PDP accurately. ERS uses a higher-level meta-regressor to integrate the predictions from many base regression models. In the proposed framework, RF, XGBoost and SVR-RBF are used as the base learners, while an appropriate regression model is considered as the meta-learner. The base learners capture the varied nature of the nonlinear interaction between the SRAM design parameters and the PDP. The meta-learner then aggregates these predictions to get the final estimate of PDP. This method can improve generalization by utilizing the complementary characteristics of individual learning algorithms. The SRAM dataset is modelled using SVR-RBF to model the nonlinear interactions. The RBF kernel maps the input parameters into a higher-dimensional feature space, allowing complicated interactions between the circuit variables and PDP to be represented without the need to explicitly define a nonlinear mathematical equation. The SVR-RBF model has parameters including regularization Coefficient (C), Kernel Width (Gamma) and Insensitive Loss Parameter (Epsilon). Therefore, hyperparameters are tuned properly to get accurate PDP prediction and to prevent overfitting. All four models are trained on the dataset supplied by SPICE, where the circuit and operational parameters are employed as input features, and PDP is the regression objective. The dataset is split into training (80%) and testing (20%) data, and the test data are maintained separate from model training to offer an unbiased evaluation of prediction performance. The models are evaluated in terms of R^2, MAE and RMSE. Higher R^2 and lower MAE and RMSE values indicate superior prediction accuracy. The input features were normalized using Min-Max Scaler before training the machine learning algorithms. The prediction errors were evaluated on the original physical scale of actual and predicted Power-Delay Product (PDP) values. Thus, the RMSE and MAE are represented in Joules (J). The surrogate model for the optimization of PDP is then chosen as the model with the optimal trade-off between prediction accuracy and generalization capabilities. Finally, an independent SPICE simulation is carried out to verify the optimum operating point predicted by the selected ML model. Figure 4(a)-4(d) depicts the actual versus predicted PDP of ML.

The predicted write PDP values are quite close to the ideal trend, and most points are spread close to the reference line. This shows good agreement of the simulated and predicted write PDP, with moderate prediction variations. Data points are well clustered around the optimum trend line for the whole PDP range. This indicates high predictive

power and accurate modeling of the write PDP. The predictions are quite close to the ideal trend line, suggesting good agreement between the actual and expected write PDP values. The model can be used to describe the dependency of circuit parameters and write PDP properly.

The predicted values reflect the overall growing trend of actual write PDP, however more scatter is observed compared to the other models. It has a fair prediction accuracy but considerably larger prediction error.

Table 1. Performance analysis of various ML algorithms

Algorithm	Target	R^2±S.D.	RMSE± S.D.	MAE± S.D.
RFR	Write PDP	0.969228 ± 0.004	2.79E-03 ± 0.0012	2.19E-03 ± 0.0010
XGBoost		0.978924 ± 0.002	3.20E-04 ± 0.0008	2.62E-04 ± 0.0006
ESR		0.986147 ± 0.001	3.02E-04 ± 0.0005	2.40E-04 ± 0.0004
SVR-RBF		0.962993 ± 0.0005	2.28E-03 ± 0.0002	1.77E-03 ± 0.0008
RFR	Read PDP	0.970109 ± 0.001	9.83E-04 ± 0.0006	7.34E-04 ± 0.0006
XGBoost		0.97679 ± 0.003	6.91E-04 ± 0.0004	2.65E-04 ± 0.0011
ESR		0.98413 ± 0.002	4.39E-04 ± 0.0002	1.55E-04 ± 0.0008
SVR-RBF		0.95412 ± 0.0005	1.18E-03 ± 0.0005	7.46E-04 ± 0.0004

The performance of four ML models for write and read PDP prediction of the proposed CF-9T SRAM cell is shown in Table 1. Results show that all models predict with high accuracy, with R^2 greater than 0.95 for both operations. The RFR model for write PDP has R^2 value of 0.969228 and an RMSE of $2.79x10^{-3}$. XGBoost improves the prediction accuracy with R^2 of 0.978924 and RMSE of $3.20x10^{-4}$. maximum write-PDP accuracy is achieved by the ESR with an R^2 value of 0.986147, an RMSE of $3.02x10^{-4}$, and an MAE of $2.40x10^{-4}$. SVR-RBF achieves the worst write-PDP performance compared to the other models. It has R^2=0.962993 and MAE of $1.77X10^{-3}$. For read PDP, RFR gets R^2=0.970109, and XGBoost gets it up to 0.976790. Again, the ESR is the best overall read-PDP prediction with R^2=0.984130. It also achieves the smallest MAE of $1.55x10^{-4}$, which demonstrates a minimal mean prediction error. The SVR-RBF model has the lowest R^2 for read PDP at 0.954120, but still shows a high correlation with the simulated results. The greater R^2 achieved by ESR demonstrates its capacity of it to adequately capture the non-linear characteristics. The decreased error values of the ESR also indicate that the prediction accuracy is enhanced compared to the individual RF, XGBoost and SVR-RBF models. These results suggest that the combination of several learning procedures can result in more robust PDP estimation than the use of a single regression algorithm. Hence, ESR is selected as the best-suited surrogate model for the further PDP optimization of the proposed memory cell. Finally, the optimum found by ML should be tested by independent SPICE simulations to check the practical accuracy of the optimization result.

6. Results & Discussion

The comparative results show that the proposed memory cell provides substantial enhancement in speed and power-delay performance in contrast to the orthodox 6T, 8T and 9T SRAM architectures. The proposed cell utilizes nine transistors, as in the present 9T architecture, but provides much lower read and write delay. The proposed CF-9T has just a 0.0049 ns read latency, whereas the 6T, 8T, and present 9T SRAM have delays of 0.671 ns, 0.517 ns, and 0.388 ns, respectively. The write delay is also decreased to 0.1184 ns, which is less than that of the 6T and 8T cells and gives competitive performance in comparison to 9T cell. The proposed cell also exhibits the lowest read PDP of $1.05x10^{-20}$ J and write PDP of $2.06x10^{-16}$ J as compared to the other architectures.

This shows the improvement in energy efficiency in read and write operations. Although the power consumption of the proposed CF-9T is 2.14 µW, which is slightly higher than the existing 9T SRAM 1.70 µW, the huge reduction in delay leads in a far lower PDP. Table 2 shows that the CF-9T design provides an effective compromise between transistor count, power consumption, operating speed and energy efficiency. The proposed CF-9T is a promising design for high-speed and low-power SRAM applications since it uses the same transistor count of nine as the present 9T cell, but with a much-reduced latency and PDP. The proposed CF-9T SRAM attains a 69.92% mitigation in read PDP and a 32.90% mitigation in write PDP in comparison to 9T cell [15], which signifies the enhancement in energy efficiency with same number of transistors.

Table 2. Performance comparison of various SRAM cells

Parameter	6T SRAM	8T SRAM	Existing 9T SRAM [15]	Proposed CF-9T
Technology (nm)	180	180	180	180
V_{DD} (V)	1.8	1.8	1.8	1.8
Transistors	6	8	9	9
Power (µW)	1.69	1.82	1.70	2.14
Read Delay (ns)	0.671	0.517	0.388	0.0049
Write Delay (ns)	0.267	0.392	0.181	0.1184
Read PDP (J)	8.12E-20	5.83E-20	3.49E-20	1.05E-20
Write PDP (J)	4.51E-16	7.13 E-16	3.07E-16	2.06E-16

7. Conclusion

The 8T SRAM core was extended with an additional NMOS footer transistor coupled to the virtual-ground path, and a Controllable-Footer 9T (CF-9T) SRAM cell was proposed. The proposed structure adds an extra control parameter $V_{FG,}$ which provides flexibility to manage the footer operation and the trade-off between power and delay. SPICE simulations were performed using 180-nm CMOS technology at V_{DD}=1.8 V. The proposed CF-9T has obtained the lowest read delay of 0.0049 ns, write delay of 0.1184 ns, read PDP of $1.05x10^{-20}$ J and write PDP of $2.06x10^{-16}$ J in comparison to the traditional 6T, 8T and current 9T SRAM cells, indicating better power-delay performance. Then, the simulation dataset was built using circuit parameters such as V_{DD}, V_{FG} and transistor dimension parameters, with write PDP and read PDP as goal outputs. To forecast the SRAM PDP features, regression-based ML models such as ESR, RFR, SVR-RBF and XGBoost were used. The models were evaluated using R^2, MAE, and RMSE, and the best model exhibited a strong correlation between simulated and predicted PDP values. The ML framework observed a predicted low-PDP operating state, which was validated with SPICE simulation, illustrating the effectiveness of ML as a design space exploration and optimization technique for the proposed CF-9T SRAM. Thus, the ML framework serves as complementary tool to the circuit-level simulation for efficient prediction of SRAM performance and data-driven identification of acceptable operating conditions and optimization of the proposed CF-9T SRAM design. SRAM stability and reliability are important design considerations, the presented investigation does not provide a complete evaluation of Read Static Noise Margin (RSNM), Write Static Noise Margin (WSNM) and Monte Carlo reliability. These characteristics will be considered in future work to provide a more complete evaluation of the stability and reliability of the proposed SRAM cell.

Conflicts of Interest

The authors declare that there is no conflict of interest regarding the content of this article

Funding Statement

No funding was received for conducting this study.

Acknowledgments

The idea of the research was conceptualized by Neetu Rathi and Neeraj Gupta. Anil Kumar and Neeraj Gupta carried out the simulation of proposed device. The formal analysis and resources for the research were arranged by Sanjay Kumar Singh.

Neeraj Gupta, Anil Kumar and Neetu Rathi also prepared the original draft of the paper. Sanjay Kumar Singh, Anil Kumar and Neetu Rathi did the review, proofreading and necessary editing in the article.

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