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Original Article

Frequency Response-Based Design of PI and PID Controllers for a Quadratic Boost Converter

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Abstract *- Quadratic Boost Converters (QBCs) may produce high voltage gains without excessive duty cycles, making them ideal for high step-up DC-DC conversion. However, QBCs' multistage construction and high-order dynamics make voltage regulation difficult, especially under input voltage and load changes. A systematic, frequency-response-based design and comparison of PI and PID controllers for a QBC is presented in this work. The work starts with QBC hardware parameter design, then state-space modeling, and small-signal duty-to-output transfer function formulation. PI and PID controllers are tuned using Bode-plot analysis to establish a target phase margin, gain crossover frequency, and predicted transient response. With a 33 kHz switching frequency, the converter steps up 40 V to 400 V at 400 W. MATLAB simulates open-loop, closed-loop, and PI and PID controller operations. The analysis covers rise time, settling time, overshoot, steady-state error, gain/phase margins, and input voltage step variations. Both PI and PID controllers stabilize the QBC and meet transient-response criteria. The PID controller has a shorter rising time (0.456 s compared to 0.7509 s), faster settling (0.808 s versus 1.293 s), and reduced steady-state error (0.007% versus 0.08%) than the PI controller, with almost no overshoot for a 400 V reference. PID controllers dampen and recover faster from input-voltage perturbations. These findings demonstrate that frequency-response-based PID design can regulate high-order QBCs efficiently.*

Keywords *- QBC, PI and PID Controller, Frequency Response, Bode Plot, DC-DC Conversion.*

1. Introduction

DC-DC converters are key building blocks in modern power-electronic systems, particularly in renewable-energy applications such as photovoltaic (PV) power generation. A single PV module typically produces a relatively low and fluctuating DC voltage on the order of 18-40V while grid-connected systems (e.g., micro inverters) require a much higher DC bus voltage before conversion to AC grid levels (220-230 V) [1-7]. A key component is the step-up converter, which must be both efficient and well-regulated to successfully adapt the PV source's output for the grid-interface converter. The literature presents a range of step-up converter topologies designed to meet this specification. These encompass fundamental designs like the conventional boost converter, as well as more advanced configurations such as interleaved, cascaded, and high-gain architectures, notably the QBC [8]. Furthermore, an isolated high-boost DC-DC flyback converter has also been developed, which consists of an active clamp circuit and a boost converter with an isolated transformer [9].

The QBC is particularly appealing because it provides a quadratic relationship between output voltage and duty cycle. Compared with a conventional boost converter, a QBC can achieve a higher voltage gain at a moderate duty cycle, while maintaining acceptable voltage stress on semiconductor devices [10-12]. This feature makes QBCs suitable for low-voltage renewable-energy sources and micro inverter front-end stages.

Research on QBCs has progressed in at least two directions. The first focuses on new topologies and modifications to improve voltage gain, efficiency, and component utilization, for example, interleaved, coupled-inductor, switched-capacitor, and switched-inductor variants [13, 14]. The second part focuses on control methods to stabilize the output voltage and improve dynamic response. For QBCs, a wide range of control schemes has been explored, including PI/PID control, sliding-mode control, fuzzy logic, and other robust or nonlinear regulators [15-22]. Despite this extensive literature, many studies either concentrate on sophisticated nonlinear techniques or apply classical

controllers tuned mainly with time-domain trial-and-error. For engineers who need transparent design rules and easy implementation, a systematic frequency-domain approach to tuning PI and PID controllers remains attractive. Frequency-response methods, based on Bode plots, gain crossover frequency, and phase margin, offer a clear way to shape stability margins and transient response for high-order systems such as QBCs [23].

In parallel, optimization-based PID tuning using meta-heuristic algorithms such as Genetic Algorithms, Particle Swarm Optimization, Artificial Bee Colony, and other hybrid methods has been widely investigated, particularly for complex or uncertain plants [24-27]. Fractional-order and filtered PID variants have also been proposed to further enhance robustness and disturbance rejection [28-32]. These advanced approaches can provide excellent performance but often at the cost of higher implementation complexity and reduced transparency for practicing engineers.

In contrast, this work deliberately focuses on a classical yet rigorous frequency-response design of PI and PID controllers for a QBC, with the following main contributions: A complete workflow from QBC component design, state-space modelling, and small-signal transfer-function derivation to frequency-response-based controller tuning is presented in a unified manner.

To bridge this specific research gap, the novelty of this work deliberately introduces a rigorous, systematic frequency-response-based design framework for PI and PID controllers tailored for a high-order QBC. By utilizing Bode-plot analysis under explicit phase-margin (ϕ_m) specifications, this approach establishes a direct, mathematical bridge between frequency-domain design targets and exact time-domain performance metrics (rise time, overshoot, and settling time) without relying on complex nonlinear algorithms or empirical trial-and-error.

The remainder of the paper is organized as follows. Section 2 describes the QBC topology, operating principles, and averaged state-space model. Section 3 summarizes the design of passive components and introduces the frequency-response-based design of PI and PID controllers. Section 4 explains the simulation methodology. The results are laid out and discussed in Section 5, where we take a close look at how the system handles step changes and rejects disturbances. Finally, in Section 6, we wrap up the paper by summarizing our key findings and pointing toward promising directions for future research.

2. Quadratic Boost Converter

The Quadratic Boost Converter (QBC) is an extended form of the conventional boost converter, designed to achieve a higher voltage gain without requiring an extreme duty cycle [33-36]. The schematic diagram of the QBC is illustrated in Figure 1.

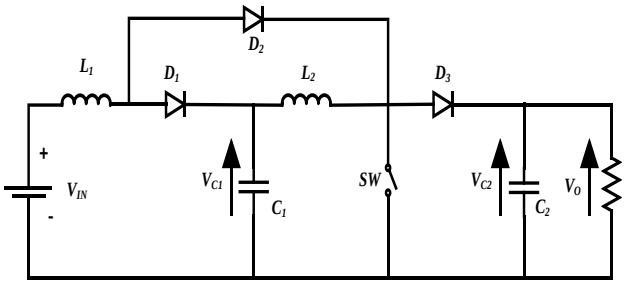

Fig. 1 Circuit diagram for the quadratic boost converter

2.1. Analysis of QBC

This converter employs two voltage-boosting stages that produce a quadratic gain. The QBC consists of two inductors (L_1 and L_2), two capacitors (C_1 and C_2), three diodes (D_1, D_2, and D_3), and a single power switch, typically a MOSFET.

There are two sub-intervals for the steady-state operation of the QBC in Continuous Conduction Mode (CCM). Figure 2 shows the first sub-interval, which is when the switch is turned ON. Diode D_2 is forward-biased during this time, and diodes D_1 and D_3 are reverse-biased. The input voltage (V_{in}) sends energy to inductor L_1, and capacitor C_1 sends energy to inductor L_2. Capacitor C_2, on the other hand, gives up its energy to power the resistive load. Because of this, the currents in both inductors, i_{L1} and i_{L2}, start to go up.

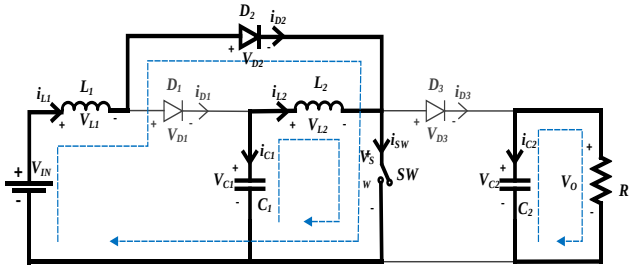

Fig. 2 Model SW ON

The corresponding state equations are given by

$$\frac{di_{L1}}{dt} = \frac{V_{in}}{L_1} \quad (1)$$

$$\frac{di_{L2}}{dt} = \frac{V_1}{L_2} \quad (2)$$

$$\frac{dv_{C1}}{dt} = \frac{-I_{L2}}{C_1} \quad (3)$$

$$\frac{dv_{C2}}{dt} = -\frac{V_o}{RC_2} \quad (4)$$

These state equations can be expressed in matrix form. $\dot{x} = A_{on}\,x + B_{on}\,u,$ where $x = [i_{L1}\ i_{L2}\ v_{C1}\ v_{C2}]^T$. The state-

space matrices for Mode 1 (SW=ON), A_{on} , and B_{on} are given in (5) and (6).

$$A_{\text{on}} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{L_2} & 0 \\ 0 & -\frac{1}{C_1} & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{RC_2} \end{bmatrix} \quad (5)$$

$$B_{\text{on}} = \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad (6)$$

During the second sub-interval, when the switch SW is turned OFF (as shown in Figure 3), diodes D_1 and D_3 become forward-biased, while diode $_2$ is reverse-biased. The stored energy in inductors L_1 and L_2 is transferred to charge capacitors C_1 and C_2. In this interval, the inductor currents i_{L1} and i_{L2} begin to decrease.

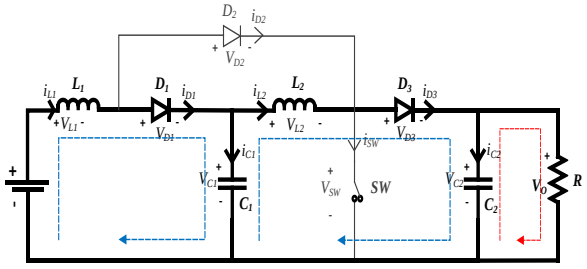

Fig. 3 Model SW OFF

The relationship between the input voltage and the output voltage of the QBC can be expressed as:

$$\frac{di_{L1}}{dt} = \frac{V_{in}-V_1}{L_1} \quad (7)$$

$$\frac{di_{L2}}{dt} = \frac{V_1-V_o}{L_2} \quad (8)$$

$$\frac{dv_{C1}}{dt} = \frac{i_{L1}-i_{L2}}{C_1} \quad (9)$$

$$\frac{dv_{C2}}{dt} = \frac{i_{L2}}{C_2} - \frac{V_o}{RC_2} \quad (10)$$

In the state-space representation for Mode 2 (SW = OFF), the matrices are given by:

$$A_{\text{off}} = \begin{bmatrix} 0 & 0 & -\frac{1}{L_1} & 0 \\ 0 & 0 & \frac{1}{L_2} & -\frac{1}{L_2} \\ \frac{1}{C_1} & -\frac{1}{C_1} & 0 & 0 \\ 0 & \frac{1}{C_2} & 0 & -\frac{1}{RC_2} \end{bmatrix} \quad (11)$$

$$B_{\text{off}} = \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad (12)$$

By applying the state-space averaging method, the dynamic behavior of the QBC is obtained by weighting the two switching intervals using the duty ratio D and its complement (1-D), yielding.

$$A(D) = DA_{\text{on}} + (1-D)A_{\text{off}}. \quad (13)$$

$$B(D) = DB_{\text{on}} + (1-D)B_{\text{off}}. \quad (14)$$

Here, $A(D)$ and $B(D)$ represent the averaged state matrix and averaged input matrix, respectively, formed from the contribution of the ON and OFF intervals. Thus, the averaged system dynamics can be written as

$$\begin{aligned} \dot{x} &= A(D)x + B(D)u \\ y &= Cx \end{aligned} \quad (15)$$

Where

$$A(D) = \begin{bmatrix} 0 & 0 & -\frac{1-D}{L_1} & 0 \\ 0 & 0 & \frac{1}{L_2} & -\frac{1-D}{L_2} \\ \frac{1-D}{C_1} & 0 & 0 & 0 \\ 0 & \frac{1-D}{C_2} & 0 & -\frac{1}{RC_2} \end{bmatrix} \quad (16)$$

$$B(D) = \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad (17)$$

In the state-space representation of the QBC, the output vector is typically chosen as the output voltage, leading to the following output equation:

$$y = [V_{C0}] = [0 \quad 0 \quad 0 \quad 1]x \quad (18)$$

The transfer function that relates the output voltage to the duty ratio is obtained and presented in the following equation:

$$G(s) = \frac{\hat{V}_o(s)}{\hat{d}(s)} = \frac{g_3 s^3 + g_2 s^2 + g_1 s + g_0}{s^4 + a_3 s^3 + a_2 s^2 + a_1 s + a_0} \quad (19)$$

where,

$$g_3 = \frac{V_{in}}{(1-D)^3 C_2 R} \quad (20)$$

$$g_2 = \frac{-V_{in}}{(1-D)L_2 C_2} \quad (21)$$

$$g_1 = V_{in}\left[\frac{2L_1 + L_2(1-D)^2}{(1-D)^3 C_1 C_2 L_1 L_2 R}\right] \quad (22)$$

$$g_0 = \frac{-2V_{in}(1-D)}{L_1L_2C_1C_2} \quad (23)$$

$$a_3 = \frac{1}{C_2R} \quad (24)$$

$$a_2 = \frac{1}{L_2C_1} + \frac{(1-D)^2}{L_2C_2} + \frac{(1-D)^2}{L_1C_1} \quad (25)$$

$$a_1 = \frac{1}{L_2C_1C_2R} + \frac{(1-D)^2}{L_1C_2C_1R} \quad (26)$$

$$a_0 = \frac{(1-D)^4}{L_1L_2C_2C_1R} \quad (27)$$

2.2. Design of QBC

The components' design of the QBC can be executed depending on the desired standards. The parameters can be the input voltage (V_{in}), output voltage (V_o), load power (P_o), switching frequency (f_s), and the allowable current and voltage ripple limits [37]. The ideal voltage conversion ratio of a QBC is given as [38]:

$$V_o = \frac{V_{in}}{(1-D)^2} \quad (28)$$

Thus, the required duty cycle can be calculated using.

$$D = 1 - \sqrt{\frac{V_{in}}{V_o}} \quad (29)$$

For a certain duty cycle, the output and input currents are given by

$$I_o = \frac{P_o}{V_o} \quad (30)$$

$$I_{in} = \frac{P_o}{\eta V_{in}} \quad (31)$$

The average currents of the first and second inductors can then be approximated as

$$I_{L1} \approx I_{in}, \qquad I_{L2} \approx \frac{P_o}{V_1} \quad (32)$$

The voltage at the intermediate stage is given by $V_1 = V_{in}/(1-D)$. A common design rule for limiting the inductor current ripple (r_L) is to keep it between 20% and 40% of the inductor's average current:

$$\Delta I_{Lk} = r_L \,.\, I_{Lk}, \qquad 0.2 \le r_L \le 0.4 \quad (33)$$

Where Ilk is the average current of the k-th inductor (i_{L1} for the first inductor and i_{L2} for the second inductor). This leads to the following inductor sizing equations:

$$L_1 \gg \frac{V_{in} \cdot D}{\Delta I_{L1} \cdot f_s} \quad (34)$$

$$L_2 \gg \frac{V_{C1} \cdot D}{\Delta I_{L2} \cdot f_s} \quad (35)$$

The voltage ripple that is allowed for the energy-storage capacitors is usually limited to 1-3% of the average capacitor voltage:

$$\Delta V_x = r_V \,.\, V_x, \qquad 0.01 \le r_V \le 0.03 \quad (36)$$

In this case, r_V stands for the capacitor voltage ripple factor, which is the percentage of the ripple compared to the average capacitor voltage. V_x is the average voltage across a certain circuit node or capacitor.

From this guideline, the minimum capacitance required for the intermediate and output capacitors is obtained as

$$C_1 \ge \frac{I_{out} \cdot D}{f_s \cdot \Delta V_{C1}} \quad (37)$$

$$C_2 \ge \frac{I_{out} \cdot D}{f_s \cdot \Delta V_{C2}} \quad (38)$$

The semiconductor devices (MOSFETs, IGBTs, and diodes) are chosen with voltage ratings at least 1.5-2 times higher than the maximum voltage stress and RMS current ratings greater than the current in the corresponding branch. The converter efficiency is then calculated by considering conduction losses, switching losses, and losses due to Equivalent Series Resistance (ESR):

$$\eta \approx \frac{P_o}{P_o + \sum P_{\text{loss}}} \quad (39)$$

3. Frequency Response-Based Design

In a frequency-response perspective, the behaviour of the plant is examined by looking at how it responds to sinusoidal inputs over a range of frequencies, through the magnitude and phase of its transfer function $G(j\omega)$ [39, 40].

From the resulting Bode plot, two quantities are particularly important: the gain crossover frequency ωc, at which the loop gain magnitude becomes unity (0 dB), and the Phase Margin (PM), defined as the difference between the system phase at ωc and -1800, which effectively measures how far the system is from the verge of instability.

A controller is generally considered well-tuned when it provides a sufficiently large phase margin, typically in the range of 450-600, together with a reasonable crossover frequency, since this balance reflects a practical trade-off between robust stability and fast dynamic response [23, 41-44]. In this work, the PI and PID controllers are both designed to achieve a phase margin of around 550, which, under a second-order approximation, corresponds to a damping ratio $\zeta \approx 0.55$ and an overshoot of about 10-13%.

3.1. PI Controller Design

To maintain a constant output voltage, the QBC is equipped with a feedback control loop [44]. In this configuration, the converter output voltage is compared with a reference voltage, and the resulting error signal is processed to adjust the duty ratio such that the output voltage remains regulated despite disturbances or load variations [45, 46].

Let *e(t)* denote the input to the PI controller and *u(t)* its output. The time-domain expression of the PI controller is given by [47, 48]:

$$u(t) = K_P e(t) + K_I \int_0^t e(t)dt \tag{40}$$

Transforming (40) into the frequency domain yields,

$$\frac{U(s)}{E(s)} = K_P \left(1 + \frac{1}{T_I s}\right) \tag{41}$$

Thus, the controller transfer function can be written as

$$G_C(s) = \frac{K_P s + K_I}{s} \tag{42}$$

Design procedures of the PI controller are as follows [49]:

1. Determine the frequency ω_1 at which the phase of the open-loop plant satisfies $\angle G(j\omega_w) = (-180^\circ + \phi_m{}^\circ + 5^\circ)$, where ϕ_m is the desired phase margin.

2. Compute the proportional gain.
$$K_P = \frac{1}{|G(j\omega_1)\, H(j\omega_1)|} \tag{43}$$

3. Define a low frequency
$$\omega_0 = 0.1 \cdot \omega_1 \tag{44}$$

4. Calculate the integral gain.
$$K_I = \omega_0 \cdot K_P \tag{45}$$

5. Substitute (44) and (45) into (43) to finalize the controller parameters.

It is noted that the integral component may introduce sluggish or oscillatory closed-loop dynamics, where the output exhibits slowly decaying or even growing oscillations if not properly tuned.

3.2. PID Controller Design

A PID controller is a linear control strategy composed of proportional, integral, and derivative elements [50, 51]. The combined action of these three components provides a versatile and robust approach for process regulation. Structurally, a PID controller can be viewed as a PI controller augmented with a derivative term [52-54]. The derivative component is particularly important for improving transient performance by reducing overshoot and suppressing oscillations in the plant response. PID controllers are the most widely used control scheme in industrial applications due to their simplicity, effectiveness, and broad applicability.

They offer desirable dynamic characteristics, including fast rise time, zero steady-state error, improved stability margins, and reduced oscillatory behaviour. Their flexibility and robustness make PID controllers indispensable in systems such as temperature regulation, pressure control, and flow management, contributing to higher process efficiency, operational safety, and product quality.

In a PID control loop, the error signal, defined as the difference between the reference value and the actual output, is processed by the proportional, integral, and derivative components [55]. By adjusting the control input accordingly, the controller aims to minimize this error continuously. The block diagram of a PID controller integrated with the plant is illustrated in Figure 3. The PID controller equation is expressed as:

$$u(t) = K_P \left(e(t) + \frac{1}{T_I}\int_0^t e(t)dt + T_D \frac{de(t)}{dt}\right) \tag{46}$$

Accordingly, the PID controller transfer function becomes,

$$\frac{U(s)}{E(s)} = G_C(s) = K_P + \frac{K_I}{s} + K_D s \tag{47}$$

Where K_P is the proportional gain, T_I is the integral time constant, T_D is the derivative time constant, K_I is the integral gain, and K_D is the derivative gain

The procedure for designing the PID operator is as follows [56]:

1. Determine the frequency ω_1 at which the angle $\angle G(j\omega_w) = -180^\circ + \phi_m{}^\circ - \angle(G(j\omega_1)\, H(j\omega_1))$, where ϕ_m is the desired phase margin.

2. Calculate the proportional gain.
$$K_P = \frac{\cos\theta}{|G(j\omega_1)\, H(j\omega_1)|} \tag{48}$$

3. Determine the derivative gain.
$$K_D = \left[\frac{\sin\theta}{\omega_1 |G(j\omega_1)\, H(j\omega_1)|}\right] + \frac{K_I}{\omega_1^2} \tag{49}$$

4. Substitute (48) and (49) into (47) to obtain the complete controller parameters.

The performance of a PID controller is shaped by the combined contributions of its three components. Increasing the proportional gain $|K_P$ accelerates the system response but

may introduce oscillations and reduce stability. The integral gain K_I eliminates steady-state error more rapidly but can lead to overshoot. The derivative gain K_D suppresses overshoot and improves damping, although excessive derivative action can slow the transient response and, in some cases, introduce instability. Therefore, the controller parameters must be selected carefully based on the dynamic characteristics of the plant.

4. Methodology

The QBC's performance under multiple control systems is tested using MATLAB/Simulink time-domain simulations. Implementing the plant model using the QBC's small-signal transfer function and setting passive component values and operating parameters according to the prior design starts the analysis.

To characterize the system in open-loop, the step response and Bode diagram are examined to determine its natural dynamics, stability margins, and prominent resonant modes. Simulate a unity-feedback system without a controller to see the simplest effect of feedback. After that, frequency-response analysis-based PI and PID controllers are developed, and their closed-loop step responses to a 400 V reference and Bode graphs are obtained.

To determine robustness, disturbance rejection is examined by altering the input voltage in multiple steps every 2 seconds to compare PI- and PID-controlled output-voltage deviations and recovery behavior. The following performance goals were specified for the controllers: the system should respond quickly (with a short rise time), have the least amount of overshoot to keep the process stable, and have no steady-state error to make sure the reference voltage is tracked accurately. The goal design criteria had a damping ratio of $\zeta = 0.55$. This indicates that the overshoot is less than or equal to 12.6% and the phase margin ϕ_m is 55°. Important performance information, such as rise time, settling time, steady-state error, gain margin, phase margin, and % overrun, can be obtained from these simulations.

5. Results and Discussion

The converter was designed to produce an output voltage of 400 V from a 40 V input source, delivering 400 W of output power at a switching frequency of 33kHz. The QBC specifications and circuit parameters employed in this study are summarized in Table 1.

To meet the desired performance requirements, the system specifications were defined as follows: a damping ratio of $\zeta = 0{,}55$, an overshoot of $\leq 10\%$, and a phase margin of $\phi_m = 55°$. Under these conditions, the system is expected to achieve a fast rise time, zero steady-state error, and a short settling time.

Table 1. Circuit parameter

Parameter	Specifications
Capacitor C_1	56μF
Capacitor C_2	100μF
Inductor L_1	250μH
Inductor L_2	800μH
Load Resistance R	400Ω

Figure 4 shows the open-loop response of the system to a step reference signal. The waveform exhibits an enormous initial overshoot, approaching 800 V, followed by ringing down to a smaller magnitude and then hovering close to the steady-state amplitude of 400 V; thus demonstrating that the system is under-damped with a low damping ratio leading to fairly large oscillatory phenomena at *t=0*. While the steady-state value attained by the system after a time approaches a value with no significant steady-state error, as can be observed, however, from Figure 4, this open-loop arrangement is characterized by its excessive damping and long settling time, such that stability of the system in any closed-loop application is inadequate to permit for practical operation without further control. This highlights the necessity of implementing a controller (such as PI or PID) to improve the dynamic characteristics, reduce overshoot, and accelerate the settling process. The Bode diagram in Figure 5 reveals the marginal stability of the open-loop system even more clearly.

The diagram indicates a gain margin of -8.45 dB and a phase margin of just 0.198°, which means that the system is operating extremely close to the instability boundary. The magnitude curve shows two significant resonance peaks, which are the two dominant oscillatory modes with a low damping ratio. At the same time, the phase curve steeply decreases and crosses 180°, thus confirming that the system acts as a high-order, underdamped plant. These features imply the possibility of the converter producing uncontrollable dynamic responses if it is operated directly in open-loop mode.

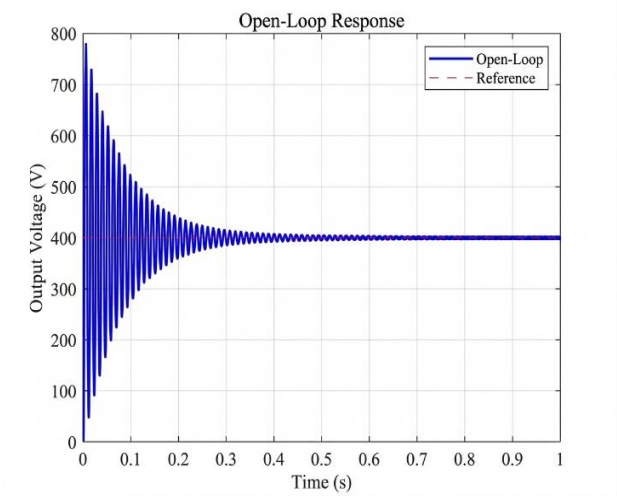

Fig. 4 Output of the open-loop system

While the system manages to reach a steady state eventually without making a large steady-state error, the big overshoot and long settling time are signs that the open-loop system has poor stability and is not suitable for practical operation without additional control. It emphasizes the necessity of a controller (e.g., PI or PID) to enhance the system's dynamic behaviour, lower the overshoot, and decrease the time needed to reach steady state. Furthermore, the use of controllers can also increase system resilience to external disturbances and parameter variations. This results in more reliable and consistent system performance under various operating conditions.

The Bode plot in Figure 5 shows that the open-loop frequency response is marginally stable. The system has a gain margin of -8.45 dB and a phase margin of only 0.198°, placing it very close to the instability boundary. The magnitude plot shows two very significant resonance peaks, which is an indication of the existence of two dominant low-damping modes. The phase plot also goes down steeply and crosses 180°, implying that the system is a high-order underdamped one. The presence of such features means that the system is capable of having uncontrolled dynamic responses if operated directly in open-loop mode.

The almost zero phase margin and negative gain margin very strongly suggest that the system is practically unstable. In such a situation, even a minor change in gain or a slight external disturbance may cause the system to oscillate continuously or diverge. The presence of two resonance peaks also indicates the complex interaction between frequency modes, which, in turn, can lead to overshoot increasing and the damping process becoming slower. Hence, the open-loop system is evidently in a condition where it needs to be compensated, or the use of a controller (e.g., PI, PID, or lead-lag) should be employed so as to increase stability margins, make the frequency response less rugged, and improve stability as well as the dynamic performance.

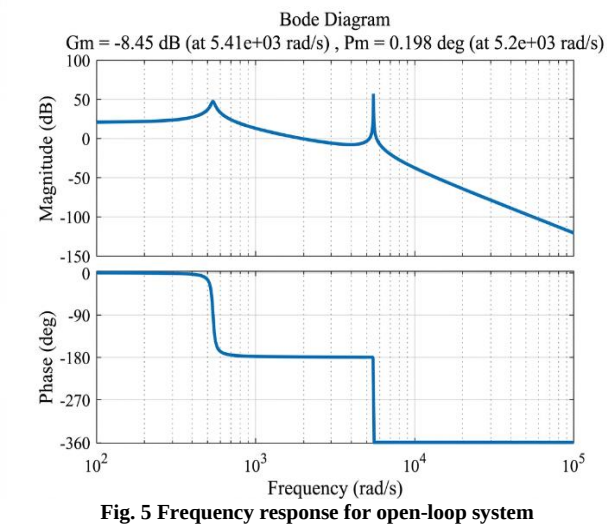

Fig. 5 Frequency response for open-loop system

Figure 6 provides information about the step input response of a closed-loop system without a controller. A response of large oscillations with the highest initial amplitudes and very slow decays over time characterizes this system. Because the system reaches a considerable overshoot and has very low damping to achieve stability at the observation time, it returns such a pattern of response. Thus, these features prove that the system is on the verge of stability, or it is practically unstable even though the system is in a closed-loop mode without a controller. The closed-loop frequency response without a controller, shown in Figure 7, indicates an infinite gain margin (Gm = ∞), whereas the phase margin is extremely small at 0.542° around 4.72×10^3 rad/s. The magnitude plot displays two resonance peaks at mid-range frequencies, indicating a high-order system with low damping.

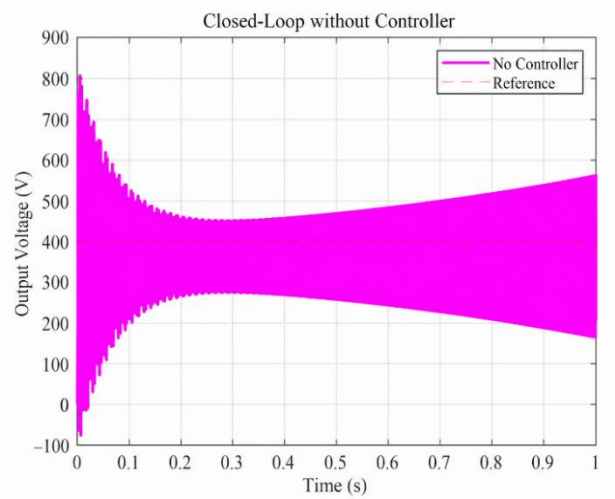

Fig. 6 Output of the closed-loop system without control

Meanwhile, the phase plot drops well beyond -360°, implying the presence of additional dynamic components that produce significant phase shifts.

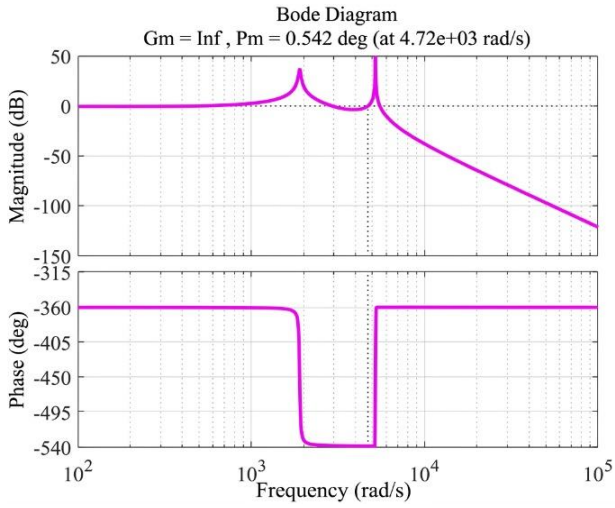

Fig. 7 Frequency response without control

The very small phase margin confirms that the system is extremely close to the instability boundary despite the infinite gain margin. This condition clearly shows that the closed-loop system without a controller exhibits weak stability, is highly prone to oscillation, and requires compensation or a controller to increase stability margins and improve its frequency response. The performance of QBC on open-loop conditions and closed-loop without a controller can be seen in Table 2. Table 2 shows how the QBC behaves when no proper controller is applied. In the open-loop condition, the converter responds relatively slowly, with a rise time of 1.90 ms, but it eventually settles with a settling time of 365.73 ms and a very small steady-state error of 0.28%. When the loop is closed without a carefully designed controller, the response becomes much faster, the rise time drops sharply to 0.42 ms, but this comes at a clear cost. The percent overshoot increases from 95.02% to 101.74%, the output does not reach a well-defined steady state (indicated by the NaN settling time), and the steady-state error grows significantly to 38.80%. In the frequency domain, the gain margin changes from -8.45 dB in open loop to an infinite value in closed loop, while the phase margin increases from 0.1980 to 0.5420. Overall, these results suggest that simply closing the loop, without proper controller design, can make the system faster but also much less accurate in steady state.

Table 2. The performance of QBC without a controller

Plant conditions	Open loop	Closed loop
Rise Time	1.90 ms	0.42 ms
Percent Overshoot	95.02	101.74
Settling time	365.73 ms	NaN ms
Steady state error	0.28 %	38.80%
Gain Margin	-8.45 dB	inf
Phase margin	0.198˚	0.542˚

5.1. The Designed PI Controller

The design specification for the PI controller is a phase margin of $\phi_m = 55^\circ$. Following the standard PI design procedure, the required phase condition is obtained as $\angle G(j\omega_w)$ = (-180°+55°+5°) = -120°. From the open-loop frequency response at -120°, the resulting frequency is ω_1=547.481 rad/s with $|G(j\omega_1)H(j\omega_1)|$= 202.40. The controller parameters are then computed using (43) and (45). The proportional gain is K_P = 0.00524, and the integral gain is K_i = 0.28812. Thus, the PI controller transfer function derived from (42) is:

$$G_c(s) = \frac{0.00524s+0.28812}{s} \quad (50)$$

The closed-loop system response with a PI controller for a 400 V step reference is depicted in Figure 8. The green curve indicates the output voltage, which moves exponentially towards the set point with almost no overshoot (OS = 0.04%). The rise time is T_r=0.7509 s and the settling time is T_s =1.2929 s; thus, the response can be considered as both fast and stable. The steady-state error is negligible, only 0.304 V (0.008%), which is a result of the integral action that is capable of completely removing the steady-state offset. The transient response is smooth and well-damped, which is a further confirmation that the PI gains are properly tuned, as the system is stabilized with excellent voltage regulation.

Figure 9 depicts the Bode diagram of the system after the PI controller application. The gain margin is extended to 23.4 dB at 724 rad/s, and the phase margin is elevated to 54.9° at 549 rad/s, very close to the design target of 55°, thus showing a dramatic change towards the controlled system.

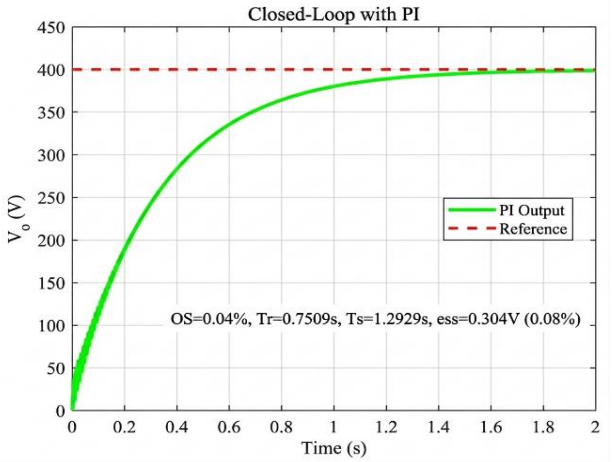

Fig. 8 Speed response of the output plant with a PI controller

The magnitude plot exhibits a clear crossover and a better-controlled mid-frequency behaviour, whereas the phase plot indicates enough phase lift to give some extra damping. These gain and phase margins are indications that the system attains solid stability with a good measure of safety margins. Actually, the frequency-domain features signal the power of the PI controller to stabilize the system and yield a system that is more responsive and well-regulated.

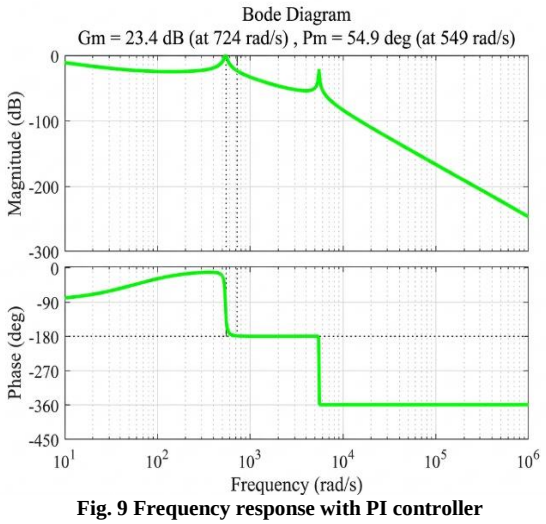

Fig. 9 Frequency response with PI controller

5.2. The Designed PID Controller

Following the PID controller design procedure, the desired phase margin is selected as ϕ_m = 55°. The required phase condition is $\angle G(j\omega_1).H(j\omega_1) = \angle -180° + 55° = -125°$. From the open-loop frequency response, the system phase of ∠-125° occurs at ω = 551.749 rad/s. Therefore, ω_1 must be chosen greater than this value while satisfying $|\angle G(j\omega_1).H(j\omega_1)|\angle 1$. The PID controller parameters K_P, K_I , and K_D are obtained from (23) and (24), yielding: $K_I = 0.505$, $K_P = 0.00492$ and $K_D = 8.99897 \times 10^{-7}$. Thus, the PID controller transfer function is:

$$G_c(s) = 0.00492 + \frac{0.505s}{s} + 8.99 \times 10^{-07}\, s \qquad (51)$$

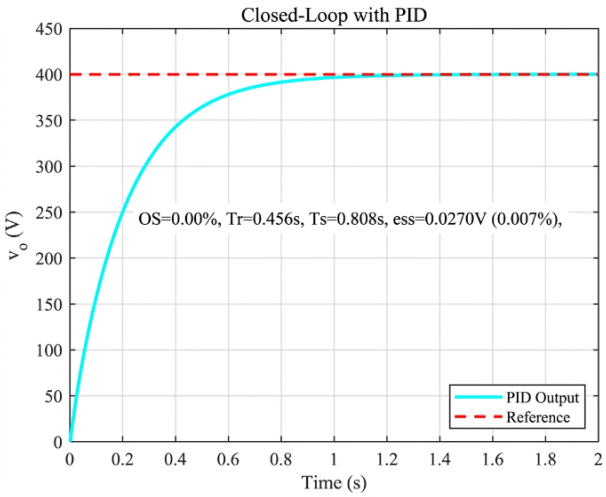

Fig. 10 Output voltage response with PID controller

Figure 10 illustrates the closed-loop transient response of the system using a PID controller for a step input of 400 V. The output (blue curve) quickly approaches the reference (red dashed line), with the rise time being 0.456 s and the settling time 0.808 s, thus, the response can be characterized as both stable and fast. The overshoot is 0% (no ringing), which is indicative of a system that is well-damped and without excessive transient deviation. At steady state, the system has a very small steady-state error of 0.0272 V (approximately 0.007% of the reference), thus, the integral action is quite effective.

Based on the Bode plot in Figure 11, the QBC system with the designed PID controller exhibits excellent and stable performance. The system achieves a very large stability margin, with a phase margin of 55˚ at $\omega_c \approx 1.8$ kHz and an infinite gain margin, indicating a fast yet secure response without excessive oscillation. Throughout the frequency range from low to high, the system keeps a small steady-state error of noise that is effectively attenuated. In general, the PID design is perfect for QBC purposes, giving a quick dynamic response and stable behavior of great trustworthiness. The quantified step response performance parameters of the QBC performance with a PI and a PID-controlled system are given in detail in Table 3.

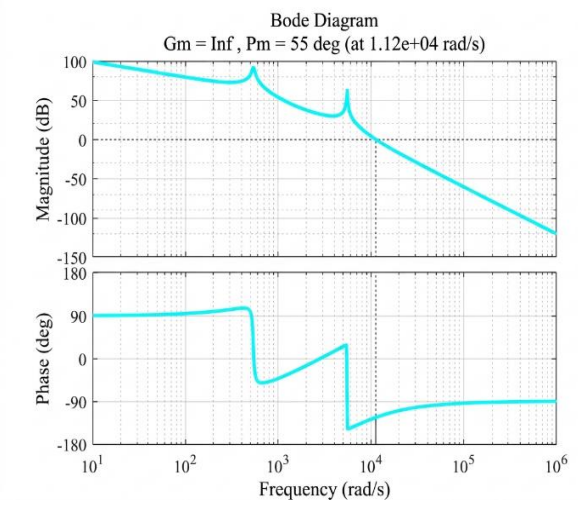

Fig. 11 Frequency response with PID controller

Table 3. The QBC performance with the PI and PID controller

Plant conditions	PI	PID
Rise Time	0.7509 s	0.456 s
Percent Overshoot	0.04	0.000
Settling time	1.2929 s	0.808 s
Steady state error	0.08%	0.007 %
Gain Margin	23.4 dB	inf
Phase margin	54.9˚	55˚

5.3. The Effect of Disturbance

A well-designed control system needs to be tested to see how well it can adapt to changes in its surroundings or changes that happen outside of it. Figure 12 shows the disturbance profile that was used on the QBC input voltage. It goes from 40 V to 50 V every 2 seconds, then to 60 V, and finally back to 40 V. This test checks the strength of the converter controller and how long it takes to return to an output voltage of roughly Vo = 400 V. Figure 13 demonstrates how the QBC's output voltage changes when the 400 V reference in V_{in} is disturbed at about t = 2 s, 4 s, and 6 s, as well as how it recovers. The PI controller (orange) has a lot more variation for each disturbance.

It goes too low during the first two disturbances and too high at t = 6 s. It also takes the PI controller longer to calm down and come back to 400 V. The PID controller (blue), on the other hand, has better damping, less overshoot and undershoot, shorter oscillation period, and faster settling. This makes it more stable for load adjustment and disturbance rejection. The derivative component of the PID controller helps it be more stable by lessening the amplitude and the time of the changes in V_{in}. The PI controller, though, is more reactive to big changes, and it takes more time to return to the normal state.

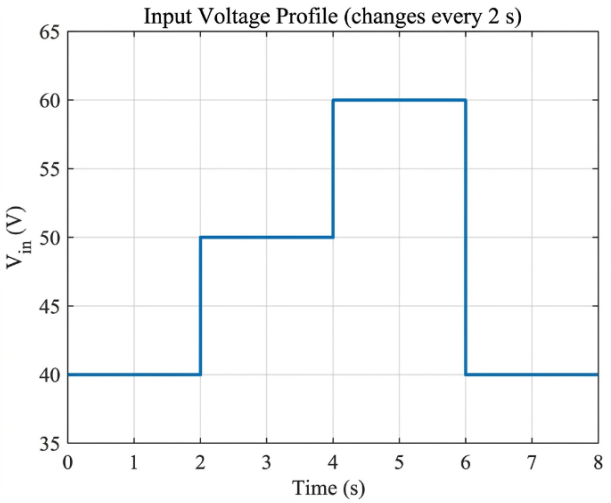

Fig. 12 Varying disturbances on the plant system

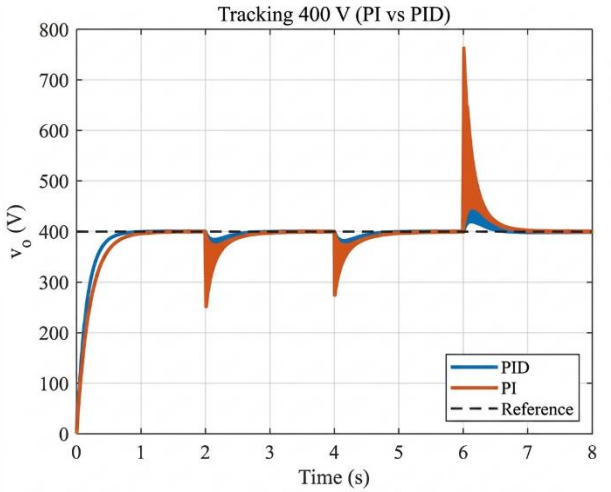

Fig. 13 Recovery process under disturbance

Tables 4 and 5 demonstrate the efficiency of the system when PI and PID controllers are used. The investigation has considered both steady-state and transient responses. The settling time, rise time, and percentage overshoot for the transient response, as well as the steady-state error, are all fulfilled. Both PI and PID controllers are able to remove the steady-state error; nevertheless, the phase margin with the PI controller is lower than anticipated. The PID controller, however, brings the phase margin to the level that was required (550). The PID controller accelerates how the system reacts. Hence, based on these findings, the system has accomplished the performance criteria that were set.

Table 4. The effect of disturbances with PI controller

Vin	OS (%)	Tr (s)	Ts (s)	ess
40	0.014	0.4646	0.8074	0.0328
50	37.50	0.0000	0.9029	0.0389
60	30.79	0.0000	1.0894	0.1155
40	95.00	0.0000	0.7321	-0.0145

Table 5. The QBC performance with the PID controller

Vin	OS (%)	Tr (s)	Ts (s)	ess
40	0.000	0.3311	0.5925	0.0270
50	2.500	0.0000	0.6721	0.0011
60	1.250	0.0000	0.8051	0.0114
40	2.500	0.0000	0.5612	0.0015

6. Conclusion

This work has shown how to construct and compare PI and PID controllers for a Quadratic Boost Converter based on their frequency response. Using Bode-plot analysis with clear phase-margin specifications, the controllers were tuned starting from the averaged state-space model and small-signal transfer function. The converter was made to boost 40 V to 400 V at 400 W with a switching frequency of 33 kHz.

Its behaviour was tested while there were changes in the step reference and input voltage. The results show that the uncompensated QBC is not stable in either open or closed loop, with a lot of overshoot, slow decay, and very small phase margins. This means that just closing the loop without a controller does not give good voltage regulation.

The frequency-response-based PI controller makes the stability margins and time-domain performance much better, resulting in a well-damped response with very little overshoot and a modest steady-state error. Rise and settling times, overshoot, and steady-state error are reduced even further by PID controllers with the same objective phase margin. Input-voltage disturbances dampen and recover faster than the PI controller, indicating its robustness and ability to reject disturbances.

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References

[1] Dharani Kolantla et al., “Critical Review on Various Inverter Topologies for PV System Architectures,” *IET Renewable Power Generation*, vol. 14, no. 17, pp. 3418-3438, 2020. [CrossRef] [Google Scholar] [Publisher Link]

[2] V. Arun, and I. Kumaraswamy, “DC-DC Converters in Solar PV System,” *International Journal of Innovative Technology and Exploring Engineering*, vol. 9, no. 3, pp. 1692-1699, 2020. [CrossRef] [Google Scholar] [Publisher Link]

[3] Farzad Karimian, Ali Nahavandi, and Pouria Pakbaz, "A Novel Structure of High Voltage Gain DC-DC Converters for Photovoltaic (PV) Applications," *Engineering Reports*, vol. 7, no. 1, pp. 1-18, 2025. [CrossRef] [Google Scholar] [Publisher Link]

[4] Wei Jiang, and Babak Fahimi, "Multi-Port Power Electric Interface for Renewable Energy Sources," *2009 Twenty-Fourth Annual IEEE Applied Power Electronics Conference and Exposition*, Washington, DC, USA, pp. 347-352, 2009. [CrossRef] [Google Scholar] [Publisher Link]

[5] Moien A. Omar, and Marwan M. Mahmoud, "Design and Simulation of DC/DC Boost Converter with Maximum Power Point Tracking for Grid Connected PV Inverter Considering the Nonlinearity of the PV Generator," *International Journal on Energy Conversion*, vol. 7, no. 6, pp. 241-242, 2019. [CrossRef] [Google Scholar] [Publisher Link]

[6] Ferdian Ronilaya, and Hajime Miyauchi, "Frequency and Voltage Control for an Autonomous Distributed Variable-Speed Wind Turbine based on a PID-Type Fuzzy Controller with Battery Support," *International Review on Modelling and Simulations*, vol. 7, no. 2, pp. 271-278, 2014. [Google Scholar] [Publisher Link]

[7] Ezhilarasan Ganesan, and Subhransu Sekhar Dash, "A New Approach in Modelling and Control of Distributed Energy Resources for Performance Optimisation and Reliability Improvement in a Micro Grid," *International Review on Modelling and Simulations*, vol. 8, no. 1, pp. 26-40, 2015. [CrossRef] [Publisher Link]

[8] A.S. Valarmathy, and M. Prabhakar, "High Gain Interleaved Boost-Derived DC-DC Converters-A Review on Structural Variations, Gain Extension Mechanisms and Applications," *E-Prime - Advances in Electrical Engineering, Electronics and Energy*, vol. 8, pp. 1-15, 2024. [CrossRef] [Google Scholar] [Publisher Link]

[9] A. Gopi, N.S. Harikrishna, and R. Saravanakumar, "Isolated High Boost Dc-Dc Flyback Converter," *International Review on Modelling and Simulations*, vol. 6, no. 2, pp. 336-341, 2013. [Google Scholar] [Publisher Link]

[10] Madhav Kumar et al., "A Critical Analysis of Quadratic Boost based High-Gain Converters for Electric Vehicle Applications: A Review," *Sensors*, vol. 24, no. 7, pp. 1-36, 2024. [CrossRef] [Google Scholar] [Publisher Link]

[11] Anindya Sundar Jana et al., "A High Gain Modified Quadratic Boost DC-DC Converter with Voltage Stress Half of Output Voltage," *Applied Sciences*, vol. 12, no. 10, pp. 1-25, 2022. [CrossRef] [Google Scholar] [Publisher Link]

[12] Preeti Sharma, Sara Hasanpour, and Rajneesh Kumar, "Ultra-High Voltage Gain Achieved with Quadratic DC/DC Converter Design," *Scientific Reports*, vol. 14, no. 1, pp. 1-20, 2024. [CrossRef] [Google Scholar] [Publisher Link]

[13] Tole Sutikno et al., "A Review on Non-Isolated Low-Power DC-DC Converter Topologies with High Output Gain for Solar Photovoltaic System Applications," *Clean Energy*, vol. 6, no. 4, pp. 557-572, 2022. [CrossRef] [Google Scholar] [Publisher Link]

[14] Babak Allahverdinejad, Ali Ajami, and Ali Makaremi, "Coupled Inductor based Quadratic High-Gain DC-DC Converter with Wide Range of CCM Operation for Photovoltaic Applications," *IET Renewable Power Generation*, vol. 19, no. 1, pp. 1-14, 2025. [CrossRef] [Google Scholar] [Publisher Link]

[15] Francesco Alonge et al., "Sliding Mode Control of Quadratic Boost Converters based on Min-Type Control Strategy," *IEEE Access*, vol. 11, pp. 39176-39184, 2023. [CrossRef] [Google Scholar] [Publisher Link]

[16] Nesrine Boujelben, Mohamed Djemel, and Nabil Derbel, "Analysis of a Quadratic Boost Converter using Sliding Mode Controller," *2020 17th International Multi-Conference on Systems, Signals and Devices (SSD)*, Monastir, Tunisia, pp. 969-973, 2020. [CrossRef] [Google Scholar] [Publisher Link]

[17] Saban Ozdemir, Necmi Altin, and Ibrahim Sefa, "Fuzzy Logic based MPPT Controller for High Conversion Ratio Quadratic Boost Converter," *International Journal of Hydrogen Energy*, vol. 42, no. 28, pp. 17748-17759, 2017. [CrossRef] [Google Scholar] [Publisher Link]

[18] Francesco Alonge et al., "Nonlinear Robust Control of a Quadratic Boost Converter in a Wide Operation Range, based on Extended Linearization Method," *Electronics*, vol. 11, no. 15, pp. 1-21, 2022. [CrossRef] [Google Scholar] [Publisher Link]

[19] F. Alonge et al., "Dynamic Modelling of a Quadratic DC/DC Single-Switch Boost Converter," *Electric Power Systems Research*, vol. 152, pp. 130-139, 2017. [CrossRef] [Google Scholar] [Publisher Link]

[20] Said Oucheriah, "Robust Controller for a Quadratic Boost Converter," *Research Square*, pp. 1-7, 2023. [CrossRef] [Google Scholar] [Publisher Link]

[21] Durgesh Sarankar, and Ashish Kumar Shinghal, "Designing of Higher Order DC-DC Converter," *IRE Journals*, vol. 1, no. 9, pp. 116-121, 2018. [Google Scholar] [Publisher Link]

[22] G. Nethajig, and J. Kathirvelan, "Performance Comparison Between PID and Fuzzy Logic Controllers for the Hardware Implementation of Traditional High Voltage DC-DC Boost Converter," *Heliyon*, vol. 10, no. 17, pp. 1-21, 2024. [CrossRef] [Google Scholar] [Publisher Link]

[23] Sigurd Skogestad, and Ian Postlethwaite, *Multivariable Feedback Control Analysis and Design*, 2nd ed., *Wiley*, 2005. [Google Scholar] [Publisher Link]

[24] Ramakant S. Patil, Sharad P. Jadhav, and Machhindranath D. Patil, "Review of Intelligent and Nature-Inspired Algorithms-based Methods for Tuning PID Controllers in Industrial Applications," *Journal of Robotics and Control*, vol. 5, no. 2, pp. 336-358, 2024. [CrossRef] [Google Scholar] [Publisher Link]

[25] Aytekin Bağiş, and Halit Şenberber, "ABC Algorithm based PID Controller Design for Higher Order Oscillatory Systems," *Electronics and Electrical Engineering*, vol. 23, no. 6, pp. 3-9, 2017. [CrossRef] [Google Scholar] [Publisher Link]

[26] Stephen Bassi Joseph et al., "Metaheuristic Algorithms for PID Controller Parameters Tuning: Review, Approaches and Open Problems," *Heliyon*, vol. 8, no. 5, pp. 1-29, 2022. [CrossRef] [Google Scholar] [Publisher Link]

[27] Khadiza Akter et al., "Design and Investigation of High-Power Quality PV Fed DC-DC Boost Converter," *E-Prime - Advances in Electrical Engineering, Electronics and Energy*, vol. 9, pp. 1-18, 2024. [CrossRef] [Google Scholar] [Publisher Link]

[28] Siavash Shirali, Saeed Zolfaghari Moghaddam, and Mortaza Aliasghary, "An Interval Type-2 Fuzzy Fractional-Order PD-PI Controller for Frequency Stabilization of Islanded Microgrids Optimized with CO Algorithm," *International Journal of Electrical Power and Energy Systems*, vol. 164, pp. 1-10, 2025. [CrossRef] [Google Scholar] [Publisher Link]

[29] Emad A. Mohamed et al., "An Optimized Hybrid Fractional Order Controller for Frequency Regulation in Multi-Area Power Systems," *IEEE Access*, vol. 8, pp. 213899-213915, 2020. [CrossRef] [Google Scholar] [Publisher Link]

[30] Heru Dibyo Laksono, et al., "Performance Evaluation of Load Frequency Control in Reheat Power Systems with Filtered PID Controllers," *Andalas Journal of Electrical and Electronic Engineering Technology*, vol. 5, no. 1, pp. 23-30, 2025. [CrossRef] [Google Scholar] [Publisher Link]

[31] Cihan Ersali, Baran Hekimoğlu, and Musa Yilmaz, "Designing A Filtered Proportional–Integral–Derivative Controller with Disturbance Rejection for a Nonideal Buck Converter Utilizing an Upgraded Genetic Algorithm and Pattern Search," *Advanced Control for Applications: Engineering and Industrial Systems*, vol. 7, no. 1, pp. 1-18, 2025. [CrossRef] [Google Scholar] [Publisher Link]

[32] B. Saidi et al., "Digital Design of Robust Fractional PID Controller for Uncertain Systems," *International Review on Modelling and Simulations*, vol. 9, no. 5, pp. 389-398, 2016. [CrossRef] [Google Scholar] [Publisher Link]

[33] Farag Elghabsi et al., "An Enhanced Voltage Gain Techniques in Quadratic Boost Converters - A Systematic Review," *ELEKTRIKA-Journal of Electrical Engineering*, vol. 23, no. 2, pp. 144-156, 2024. [CrossRef] [Google Scholar] [Publisher Link]

[34] Oswaldo Lopez-Santos et al., "Quadratic Boost Converter with Low-Output-Voltage Ripple," *IET Power Electronics*, vol. 13, no. 8, pp. 1605-1612, 2020. [CrossRef] [Google Scholar] [Publisher Link]

[35] Majid Hosseinpour et al., "A Novel Interleaved Nonisolated High Gain DC–DC Boost Converter based on Voltage Multiplier Rectifier," *Scientific Report*, vol. 15, no. 1, pp. 1-29, 2025. [CrossRef] [Google Scholar] [Publisher Link]

[36] Souheyb Mohammed Belhadj et al., "Control of Multi-Level Quadratic DC-DC Boost Converter for Photovoltaic Systems using Type-2 Fuzzy Logic Technique-Based MPPT Approaches," *Heliyon*, vol. 11, no. 3, pp. 1-25, 2025. [CrossRef] [Google Scholar] [Publisher Link]

[37] Modou Badiane et al., "Quadratic Boost Converter: An Analysis with Passive Components Losses," *Open Journal of Applied Sciences*, vol. 11, no. 2, pp. 202-215, 2021. [CrossRef] [Google Scholar] [Publisher Link]

[38] R. Selva Kumar et al., "Design and Comparison of Quadratic Boost Converter with Boost Converter," *International Journal of Engineering Research and Technology*, vol. 5, no. 1, pp. 877-881, 2016. [Google Scholar] [Publisher Link]

[39] Xinxin Zhang, Marcin B. Kaczmarek, and S. Hassan HosseinNia, "Frequency Response Analysis for Reset Control Systems: Application to Predict Precision of Motion Systems," *Control Engineering Practice*, vol. 152, pp. 1-18, 2024. [CrossRef] [Google Scholar] [Publisher Link]

[40] Xiaoqiang Li et al., "Stability Design of Single-Loop Voltage Control with Enhanced Dynamic for Voltage-Source Converters with a Low LC-Resonant-Frequency," *IEEE Transactions on Power Electronics*, vol. 33, no. 11, pp. 9937-9951, 2018. [CrossRef] [Google Scholar] [Publisher Link]

[41] Jorge Alberto Morales-Saldana et al., "Average Current-Mode Control Scheme for a Quadratic Buck Converter with a Single Switch," *IEEE Transactions on Power Electronics*, vol. 23, no. 1, pp. 485-490, 2008. [CrossRef] [Google Scholar] [Publisher Link]

[42] Mikulas Huba et al., "Making the PI and PID Controller Tuning Inspired by Ziegler and Nichols Precise and Reliable," *Sensors*, vol. 21, no. 18, pp. 1-26, 2021. [CrossRef] [Google Scholar] [Publisher Link]

[43] Tarakanath Kobaku et al., "Experimental Verification of Robust PID Controller under Feedforward Framework for a Nonminimum Phase DC-DC Boost Converter," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 9, no. 3, pp. 3373-3383, 2021. [CrossRef] [Google Scholar] [Publisher Link]

[44] Deepa Somasundaram, and Samuel Babu, "A Closed Loop Control of Quadratic Boost Converter using PID-Controller," *International Journal of Engineering*, vol. 27, no. 11, pp. 1653-1662, 2014. [Google Scholar] [Publisher Link]

[45] I. Ketut Wiryajati, Ade Safitra, and Muh. Izzul Islam, "Comparative Analysis of the Performance of Linear Quadratic Regulator and State Feedback Control on DC-DC Shunt Boost Converter," *Journal of Computer Science and Informatics Engineering*, vol. 8, no. 2, pp. 128-135, 2024. [CrossRef] [Google Scholar] [Publisher Link]

[46] Wentao Jiang, Satyajit Hemant Chincholkar, and Chok-You Chan, "Modified Voltage-Mode Controller for the Quadratic Boost Converter with Improved Output Performance," *IET Power Electronics*, vol. 11, no. 14, pp. 2222-2231, 2018. [CrossRef] [Google Scholar] [Publisher Link]

[47] Hari Agus Sujono et al., "Quadratic Boost Converter with Proportional Integral Control in the Mini Photovoltaic System for Grid," *Electrotechnical Review*, vol. 96, 2020. [CrossRef] [Google Scholar] [Publisher Link]

[48] Fatema A. Mohammed et al., "Design of a Maximum Power Point Tracking-based PID Controller for DC Converter of Stand-Alone PV System," *Journal of Electrical Systems and Information Technology*, vol. 9, no. 1, pp. 1-15, 2022. [CrossRef] [Google Scholar] [Publisher Link]

[49] Charles L. Phillips, and Royce D. Habor, *Feedback Control Systems*, Simon and Schuster, Inc., United States, 1995. [Google Scholar] [Publisher Link]

[50] Juan Garrido et al., "Design of Multivariable PID Control using Iterative Linear Programming and Decoupling," *Electronics*, vol. 13, no. 4, pp. 1-24, 2024. [CrossRef] [Google Scholar] [Publisher Link]

[51] Johannes Günther et al., "Interpretable PID Parameter Tuning for Control Engineering using General Dynamic Neural Networks: An Extensive Comparison," *PLOS One*, vol. 15, no. 12, pp. 1-17, 2020. [CrossRef] [Google Scholar] [Publisher Link]

[52] Arun R. Pathiran, "Improving the Regulatory Response of PID Controller using Internal Model Control Principles," *International Journal of Control Science and Engineering*, vol. 9, no. 1, pp. 9-14, 2019. [Google Scholar] [Publisher Link]

[53] V.M. Alfaro, and R. Vilanova, "PID Control: Resilience with Respect to Controller Implementation," *Frontiers in Control Engineering*, vol. 3, pp. 1-13, 2022. [CrossRef] [Google Scholar] [Publisher Link]

[54] Zhijun Li, Hangwei Zhang, and Wen Tan, "Comparison of PI/PID/PIDD2 Controllers for Higher Order Processes," *IFAC-PapersOnLine*, vol. 58, no. 7, pp. 340-345, 2024. [CrossRef] [Google Scholar] [Publisher Link]

[55] Driss Khouili, "Design of a Robust Nonlinear PID Controller: Simulation and Experimental Validation for a Computer Aided Aerothermic System," *International Review of Automatic Control*, vol. 15, no. 1, 2022. [CrossRef] [Google Scholar] [Publisher Link]

[56] Charles L. Phillips, and H. Troy Nagle, *Digital Control System Analysis and Design*, Prentice Hall Press, United States, 2007. [Google Scholar] [Publisher Link]