Developed Cascaded Integrator for High Speed Wideband FrequencyVariation

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ABSTRACT

Today's SDR is rotating the hardware problems into software difficulties, around or the complete physical layer determinations are software certain. Digital down conversion (DDC) and Digital up conversion (DUC) is one of the core knowledges in SDR, as well as animportantcomponent of numerical intermediate frequency (IF) receiver system. Cascade Integrator Comb (CIC) strainers are expansively used in multi rate signal handling as a filter in similarly decimator (reduction in the assortment rate) and interpolator (increase in the sampling rate). When a wide band indication is to be quantityrehabilitated to a different clock frequency then different filter constructionsconsecutively at high clock rates are required. Normal FIR architectures and its substitutes fail to work at such high occurrences. Cascaded Integrator comb (CIC) destruction filter is respected to decrease the data sampling amountlevel in such high bandwidth requirements. In this paper a CIC filter, an improved class of linear filters is performed for digital up conversion (DUC) and digital down conversion (DDC) for capable transmission and reaction in Software Defined Radio (SDR) declaration system. In this project a full-fledged arithmetical down difference and digital up adaptationsocieties are developed in VHDL for FPGA established software defined radio needs. The CIC created architecture is executed in VHDL and will be tested on Xilinx FPGAs. All the components functionality is confirmed with Modalism simulator. Xilinx ISE devices are used for FPGA combination, Place & Route and timing exploration. Spartan 3E development board with Chip scope Pro Analyzer device is used for on-chip authentication.

KEYWORDSCIC Filter, Field Programmable Gate Array (FPGA), Decimator, Interpolator, Modalism and Chipscope.

I. INTRODUCTION

Software dissimilar radio is adevelopingknowledge that is influentiallyaltering the radio system engineering. To application software definite radios, the FPGA allocates the greatest reconfigurable answer for high speed signal dispensationdevices that are extremely parallel.

FPGA assigns the best constancybetweenperformance, low power feasting, and insignificantenterprise cycle. Also, the novel Xilinx FPGA procedureallocates a dynamic and defective reconfiguration functionality which is the capability to dynamically modification a local area of logic by transferringimperfect reconfiguration files though the enduring logic sustains to function without commotion. Software Defined Radio (SDR) phasestype use of Digital down Converter (DDC) and Digital up Converter (DUC), while implementation baseband release. Digital up-conversion and down-conversion are well recognized sample rate changeprocedures in Digital Signal Processing.

These approaches are comprehensively used for altering a baseband signal to band pass suggestion and vice versa to allow the transmission and reaction. For the baseband signal to be transported, it wants to be controlled on to an IF/RF importerincidence. In simple, down alteration can be separate as rejectinginstances and creating new examples by asset of addition zeroes and comprise the new examples. The main blocks in scheming DDC and DUC would include Numerical dignified oscillator (NCO), digital mixer, CIC destruction filter and CIC interpolation and compensation FIR filter.

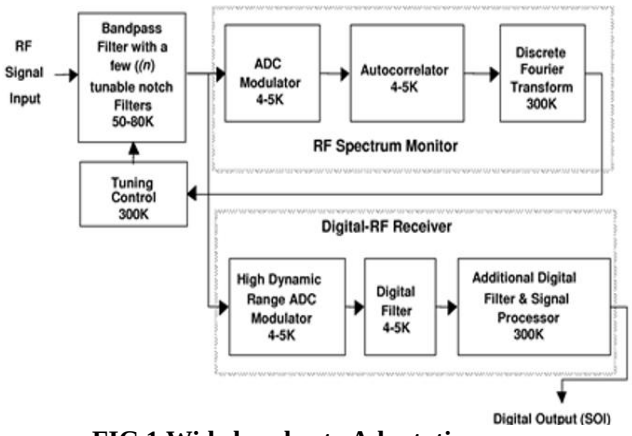


FIG 1 Wide band rate Adaptation

CIC filters are suitableselect for performingobliteration or disruption because they don't use multipliers and their occurrenceanswers canreduction aliasing and imaging difficultiessubsequent due to demolition and speakingrespectively. A CIC filter is typically used in requirements where the system example rate is much advanced than the bandwidth engaged by the suggestion. They are frequently used to form Digital down Converters and Digital up Converters. Some requirements that use the CIC filter contains software intended radios, chain modems, satellite receivers, 3G base positions, and radar systems.

Direct Digital Synthesizers license micro-Hertz alterationdetermination, mainlyperverted frequency jumping, digital control interface and abolition of guidealteration to tweak the concert. DDS submission is actualdiffident; it can be built intense a phasepayment circuitry and a look-up table conserving the signal instances. Requiring DDS on chip leakages the essential of selection circuits and transportsanavoidable flexibility in modification to the requiredincidence. In this scheme a whole digital up modification and digital down renovationpreparations will be documented in VHDL for FPGA originated software separate radio requests.

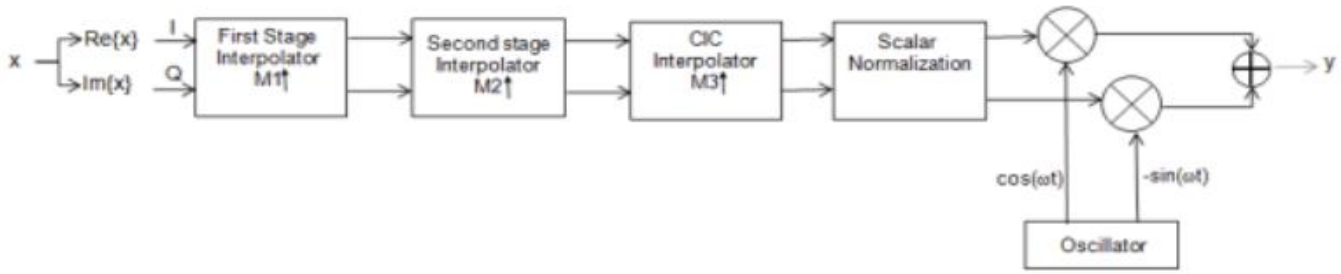


FIG 2 Digital up and down conversion

II. DIGITAL UP AND DOWN CONVERSIONS

Digital up converters (DUCs) and digital down converters (DDCs) are importantmechanisms of eachpresent wireless base locationinitiative. DUC are typically used in digital receivers to filter, up sample, and reasonableindications from baseband to the transferor frequency.

A DDC, on the additional hand, resides in the digital receiver to demodulate, filter, and down example the signal down to baseband so that extra processing on the predictable signal can be done at lower assortmentincidences. In digital signal handling, a digital down-converter converts a digitized real signal absorbed at acentral frequency to a base banded complex signal focused at zero frequency. A DDC comprises of three subcomponents: a direct digital synthesizer, a low-pass filter, and a down sampler.

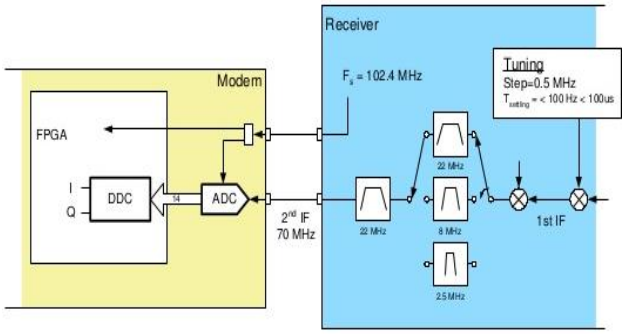
Digital Down-Converter is a key module of digital radios. The DDC attains the incidenceadaptationessential to alteration the high input sample rates create in a numerical radio, down to lower instance rates for extra and easier handling.

The DDC comprises of a Numeric Controlled Oscillatorand a mixer to down alteration the input indication to baseband. The baseband indication is then low licenseprepared by a Flowed Integrator-Comb filter monitored by two FIR terminating filters to achieve a low sample-rate. The DDS creates a combined sinusoidal signal at the middle to down changing by creating a change signal at the IF impairment the DDS frequency, they also up alteration, creating an unwanted signal at the sum of the two incidences.DDCs are most usuallyperformed in logic in field-programmable gate arrays or application-specific mutual circuits. While software requests are also conceivable, processes in the DDS, multipliers and input phases of the low pass filters all run at the sampling rate of the input data.

This is done by multiplying the incoming signal with sine and cosine signal created using a DDFS or NCO at the same frequency as the carrier frequency. This new signal, focused on the baseband frequency, is approvedfinishednumerous cascaded destroying CIC filter to outline the signal and decrease the sampling rate of the signal. Classically, the signal transformed by the DDC gets conveyed and established at very high selection rates.

However, the receiver commonly does not essential such high signal purpose to attain the necessary signal processing. Therefore, it is significant to destroy (reduce the number of samples) the incoming signal so that the respite of the signal handling can be done at lower, more sensible sampling rates.

2.1 Digital up conversion



- 70 MHz IF, 2.5. 8, & 22 MHz BWs (3dB).
- 102.4 MHz ADC Sample Rate
- Modem provides 25 KHz fine tune step
- Receiver/Exciter minimum freq step = 0.5 MHz, settling time < 100 us to 100Hz.

FIG 3 Digital up conversion

A DUCcomprises of a sequence of disruption cascade integrator comb filters, a zero stuffer, and a direct digital synthesizer or statisticallymeasured oscillator. The block illustration of the DUC and the two clock incidences given to the frequentstages in the DUC.In, the zero stuffer is used for manufacturing new instances by virtue of totaling zeroes and interrupts the new examples. CIC filter is used to form and development the example rate of the convey signal. The output signal from these filters is then different with the importer signal prior to diffusion. In simple, down adaptation can be defined.

A quantity of mutual building blocks is used to purpose narrowband DUC/DDC systems. These compriseapparatuses to devicedeterminations such as descriptive, carrier collection, and mutualgrowth. The DUC and DDC contain of the succeedingimportant blocks:

1. Numerically Controlled Oscillator (NCO)
2. The Mixer
3. Cascaded Integrated Comb (CIC)
4. Compensation Finite Impulse Response

2.2 Numerically Controlled Oscillator

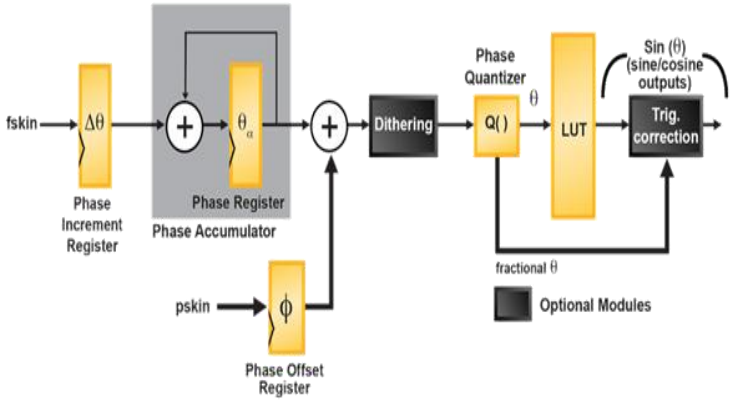


FIG 4 Numerically Control Oscillator

A numerically restrained oscillator is also called the Direct Digital Synthesizer. NCO is a digital signal manufacturercreation a synchronousisolated time, separaterespecteddepiction of the sinusoidal waveform. It is apredictable method of manufacturedintermittent sinusoid suggestions whenever high incidencefortitude, fast variations in occurrence and stage and high rangecompression of the output signal is important. The major benefit of NCO is enormously fast hopping speed in frequency or phase tuning and familiar programmability. The Through digital synthesizer purposes by storing the waveform opinion which is in arithmetical format and later it recollectionsproducing the waveform. The rate at which the synthesizer surfaces one waveform then supervises the incidence. The application of NCO comprises the following significant blocks.

1. Phase accumulator
2. Phase to amplitude converter and
3. Sin / cos LUT

ADDS produces a sine wave at a given frequency. The frequency depends on two variables, the reference clock frequency and the binary number programmed into the frequency catalog. The binary amount in the frequency register delivers the central input to the stage accumulator.

If a sine look-up board is used, the phase accumulator computes a phase address for the look-up table, which manufactures the numericalworth of amplitude - compliant to the sine of that phase angle - to the arithmetical to analog converter.

2.3 The Mixer

A mixer is used to alteration the IF suggestion to baseband sign by accumulative the input signal with compound sinusoidal signal cos (wt)-j sin (wt) = e-jwt which is formed by NCO thus charitable two indications as output i.e.

1. In-Phase signal
2. Quadrature-Phase signal

2.4. Cascade Integrator Comb Filter

Cascaded Integrator Comb filter theatersanactive role to frequent high volume wireless communication tasks and devices with CIC highlyattaindependability, performance and reduction cost. The Cascaded Integrator Comb (CIC) first familiar by Hogenauer, donations a modest but definitephase for execution of such ruin and disruption. CIC filters are well-suited for anti-aliasing expressive prior to destruction (sample-rate reduction), and for anti-imaging demanding for common signals (sample-rate increase). This type of strainer has extensiveneeds in low cost Performance of interpolators and decimators. And centraladvantage of CIC is the mathematicscontrol use adders and subtracts and record they don't essentialgrowth.

However some disadvantage of CIC filters like documentation band droop in this filter but they are separate using paymentapproaches.The CIC filter includes of N stages of integrator and comb filter. The two simple building blocks of a CIC sieve are an integrator and a comb is as visible below.

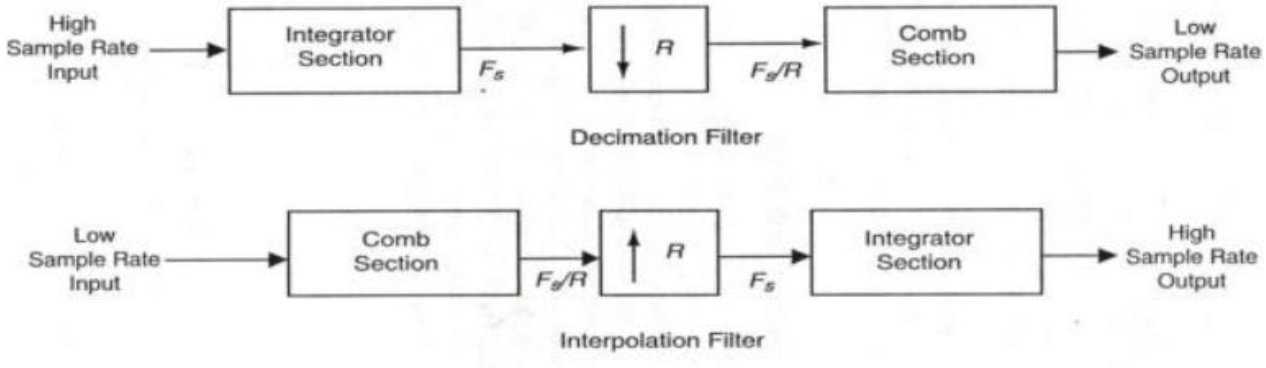


FIG 5 Determination and Interpolation using Comb and Integrator Filters

An integrator is essentially a single-pole IIR filter with anagreement feedback coefficient: y[n] =y [n-1] +x[n]thisscheme is also known as an accumulator. The assignment function for an integrator on the z-plane isa comb filter successively at the low assortment rate, f s / R, for a rate modification of R is an odd- symmetric FIR filter. Y[n] = x[n]-x [n-RM]. In this intention, M is anenterpriseconstraint and is called the alteration delay. M can be any optimistic integer, but it is regularly limited to 1 or 2. The conformingassignment at fs When we build a CIC filter, we cascade, or chain output to input, N integrator sections collected with N comb units. This filter would be fine, but we can shorten it by connection it with the rate changer. The CIC filters purpose blocks for interpolator and decimator is as tracks To summarize, a CIC decimator would have N flowed integrator stages clocked at fs, checked by a rate change by a factor R, shadowed by N cascaded comb phasesconsecutively at fs/R. A CIC interpolator would be N cascaded comb stages consecutively at fs/R, followed be a Zero-stuffer, monitored by N cascaded integrator stages running at fs.

III. SOFTWARE & HARDWARE REQUIREMENT

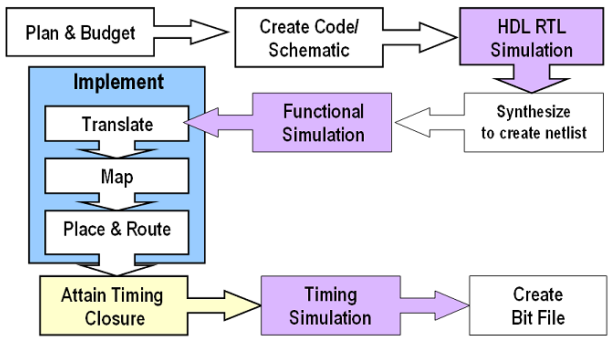


FIG 6 Xilinx Design flow

Asupport of expending an FPGA for the DDC/DUC is that we can alteration the filter chain to precisely meet our necessities. ASSPs don't offer the initiativesuppleness or combinationattainable in an FPGA. Finished the design, acommunicating model of the entire digital down adaptation and digital down conversion methods are recognized using Xilinx ISE software by writing VHDL code for each dispersed block and their process is tested by imagining the design using Modelsim Simulator.

Advanced the design is industrial and practical on an FPGA by manufacturing a .bit file of the initiative and programming, establishing the FPGA with the .bit file. The Xilinx Design flow is exposed below. Spartan 3E expansion board with Chippossibility Pro tools is secondhand for on chip examination and modifying. The detailedProcess of the design in the FPGA is tested using ChipScope Pro Analyzer tool which performs three central blocks to inspect any ration of DDC. These blocks are fashioned through the IP Core Producer tool in Xilinx ISE The blocks are: **ICON***:* Combinedexecutive is use as an interface among the other two blocks and PC, JTAG which is related to FPGA on which the enterprise is automatic. **ILA***:* Integrated Logic Analyzer is used to control the inputs of any part of DDC thus attaining Controllability of internal circuits. **VIO:**Simulated input manufacture is used to notice the outputs of any part of DDC thus achieving observability.

VI CONCLUSION

The subjects in scheming digital down converter and up converter are deliberate. The main requests where DDC develops the front end of software distinct radio are understood. Two architectures; CIC based DDC and DUC are analyzed and realized for FPGAs. VHDL common coding style is monitored to kind the blocks extremely configurable so that the similar design with general map can be arranged for dissimilardestruction rates. Stability problems in understanding CIC filters are deliberate.

REFERENCE

[1] E. B. Hogenauer, "An economical class of digital filters for decimation and interpolation", IEEE Transactions on Acoustics, Speech, Signal Processing, Vol. ASSP-29, pp. 155-162, April 1981.

[2] Ramesh Bhakthavatchalu, Karthika V.S., LekshmiRamesh,"Design and Implementation of Improved Attenuation CIC Decimator and Interpolator in FPGA", International Journal of Recent trends in Engineering and Technology, ACEEE, pg. 18-22, Vol. 6, No.2, Nov2011.

[3] Fredric J. Harris, Multirate Signal Processing for Communicating Systems, 2004.

[4] Matthew P. Donadio, "CIC Filter Introduction", IEEE International Symposium on Communications, July 2000.

[5] High performance digital down converter for FPGAs.

[6] The basic information on Digital up Converter is taken from www.latticesemi.com.

[7] Xilinx FPGA data sheet for Spartan 3E FPGA.

[8] Uwe Meyer-Baese. "Digital Signal Processing with Field Programmable Gate Arrays". Springer-Verlag, New York, Inc.,Secaucus, NJ, USA, pp. 70-75, 200.

[9] K.-Y. Khoo, Z. Yu, and A. N. Willson, Jr., "Efficient high-speed CIC decimation filter," Proc. 11th Annual IEEE International ASICConference, pp. 251-254, 1998.

[10] Matthew P. Donadio, "CIC Filter Introduction", July 18, 2000.