Analysis of Low Power Consuming Adder using Microwind EDA Tool

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Abstract

Addition is one of the basic arithmetic operations. Low power adders are used to reduce the overall power consumption of micro-electronic systems. The role of adders are important in almost all filed .With the help of low power adders , all the other systems which make use of adders may dissipate less power. This project presents a detailed comparison between the full adders designed using gates and different styles of full adder designed using transistors. This project focus mainly on the comparisons among conventional CMOS adder, transmission gate adder, square root based adder, static energy recovery adder . All the simulation results are done using Digital Schematic editor (DSCH) and the functionality is verified using the layout editor tool, MICROWIND. The sole objective of this project to conclude with a better estimate and ease in selecting a low power consuming adders.

Keywords

CMOS adder, lowPower, Microwind, transmission gate adder, SERF.

I. INTRODUCTION

Addition is most commonly performed arithmetic operation.Adder is basic building block of most digital system.The role of adders are important in almost all field of engineering.

A) Adders

In digital electronics, adders is a digital circuit that performs addition of two numbers.Adders are used not only in the ALU, but also in other part of the processors, where they are used to calculate addresses, table indices, and many more.

B) Half adder

A Half Adder (HA) is a logical circuit that performs an addition operation on two binary digits. The half adder produces a sum and carry value which are both binary digits.

A HA adds two one bit binary numbers A and B. It has two outputs S and C. The simplest half adder design shown in the figure 1.

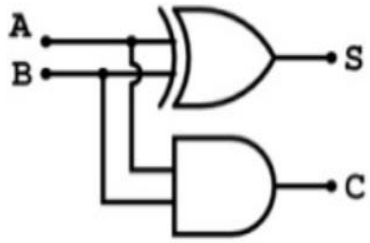

Figure 1. Half Adder

C) Full adder

A Full Adder (FA) is a logical circuit that performs an addition operation on three binary digits. The full adder produces the sum and carry value, which are both binary digits . The logical diagram of full adder is shown in figure 2.

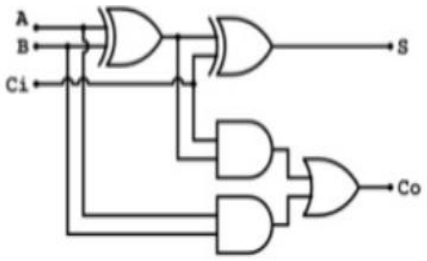

Figure 2. Full Adder

D) Ripple carry adder

It is possible to create a logical circuit using multiple full adders to add *N*-bit numbers. Each full adder inputs a C_{in}, which is the C_{out} of the previous adder. This kind of adder is called a ripple-carry adder, since each carry bit "ripples" to the next full adder. Note that the first (and only the first) full adder may be replaced by a half adder (under the assumption that $C_{in} = 0$).

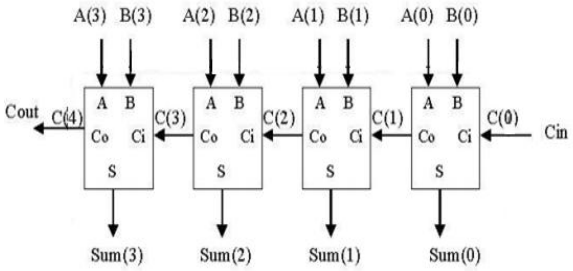

Figure 3. 4- bit ripple carry adder

E) Low power consuming adder

Low power adders help in producing the low power multipliers which are most important in all kind of computing applications . The importance of green energy and smart application based systems are understood by all kind of people to save the energy and power . Nowadays, these low power circuit designs are most suitable for the better environment . Since the battery technology evolution growth is poor compared semiconductor technology growth, the engineers focous designing low power systems by proposing suitable optimized circuits.

With respect to power there are two major categories . They are,

1. Staic Power Dissipation

2. Dynamic Power Dissipation

F) Static power dissipation

Static or leakage power occurs while the transitors are in "off" mode. By suppressing the unwanted transistors during the operation of the system , the static or leakage power are reduced in a significant manner.

G) Dynamic power dissipation

Dynamic power dissipation occurs during the switching activity of the transistor. By reducing the supply voltage and the clock frequency of the system , the dynamic power dissipation is reduced dramatically. Also less loading capacitance helps in reduction of switching power of the system.

II. PROPOSED SYSTEM

In this project we are going to design four 3-bit full adder which may consume low power when compared with the full adder designed using gates.The four 3-bit full adder which we are going to design are,

a. Standard CMOS full adder

b. Transmission gate full adder

c. Square root based full adder

d. Static energy recovery full adder

A. Standard CMOS adder

CMOS is a combination of PMOS and NMOS.It is immune towards noise occurring condition.It is also used in designing integrated circuits,microprocessor and microcontroller.
The advantages of this adder is that it is robustness against voltage scaling and transistor sizing which ensure reliable operation at low voltage with arbitrary transistor sizes .

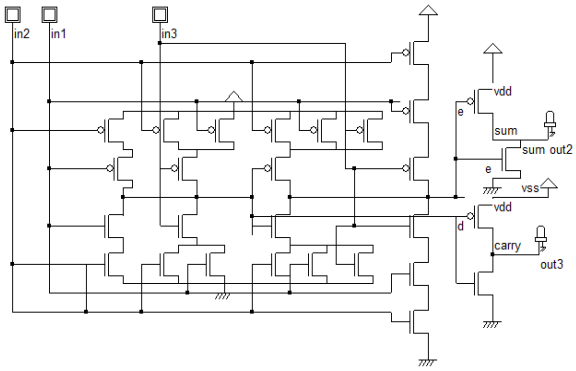

Figure 4. Standard Cmos Full Adder

B. Transmission gate adder

A transmission gate is defined as an electronic element that will selectively block or pass a signal level from the input to the output. This solid-state switch is comprised of a PMOS transistor and NMOS transistor. The transmission gate consists of two MOSFETs, one n-channel responsible for correct transmission of logic zeros, and one p-channel, responsible for correct transmission of logic ones.

A transmission gate adder is constructed with the help of just 12 transistors (excluding the 8 transistors used for negating the inputs). This circuit is viewed as an extended version of pass transistor logic, providing a maximum voltage level at the output. This adder is quite mentioned in the literature many times as it consumes almost half of the power consumed by a conventional full adder.

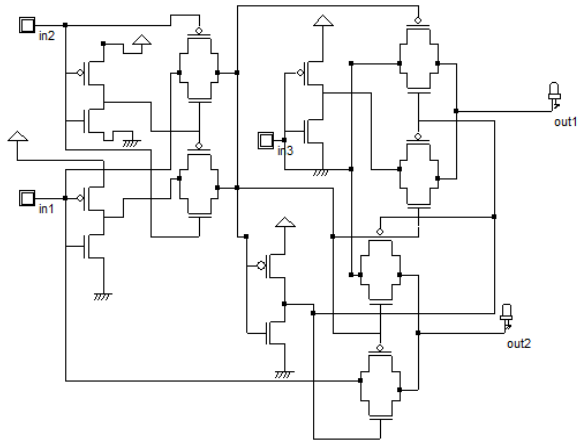

Figure 5. Transmission gate full adder

C. Square Root Based Full Adder

The square root based full adder has been chosen for comparison with the proposed design as it has a more balanced delay, and requires lower power and area.

This adder uses the Multiplexing Control Input Technique (MCIT) and Boolean reduction techniques for the sum and carry calculations . This circuit is constructed with the help of 15 transistors including the invertors at the three inputs. Though this adder provides very less power consumption, its output voltage levels and time delays are found to be compromising.

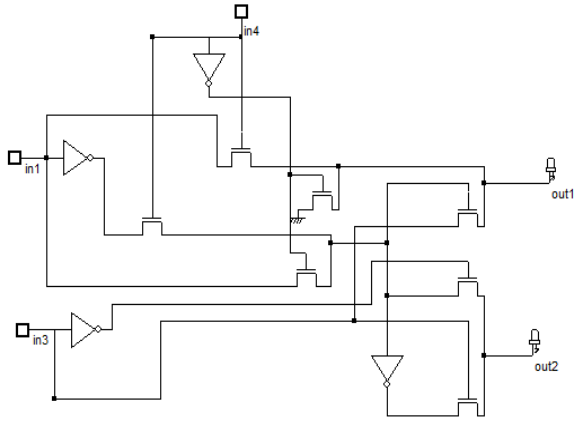

Figure 6. Square root based adder

d.Static energy recovery full adder

Static energy recovery full adder is the one which consumes least power.Here the requirement of ground and its corresponding connections are completely eliminated. A low logic level in the circuit substitutes the functionality of ground. This design saves up to 18 transistors when compared with the standard CMOS transistor. The area occupied by its layout has also been recorded to be very less. It does not needed inverted inputs. The static energy recovery adder uses 10 transistors. The circuit is claimed to be extremely low power because it does not contains direct path to the ground and the charge stored at the load capacitance is reapplied to the control gates (energy recovery).

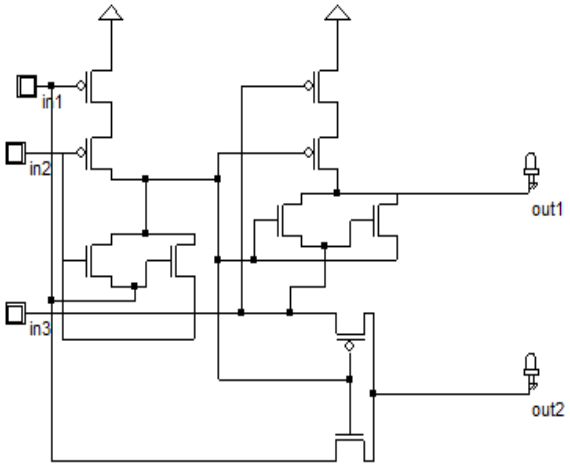

Figure 7. Static energy recovery full adder

III. RESULT & DISCUSSION

The circuit of the four different styles of full adder is designed using MICROWIND tool and it's layout are generated with the help of Microwind layout editor and it's functionalities are verified in each style.

The circuit of standard CMOS adder which is designed in Microwind tool is shown in fig.8.

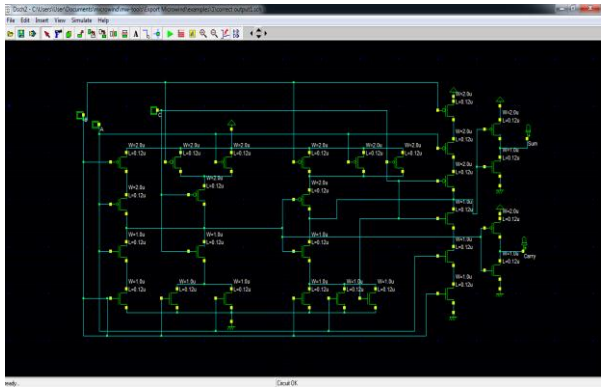

Figure 8. Circuit of standard CMOS adder

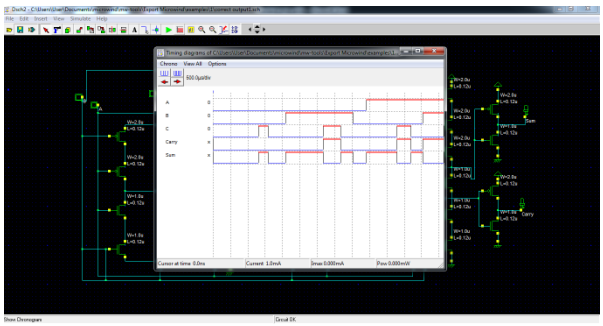

Figure 9.Timing diagram results

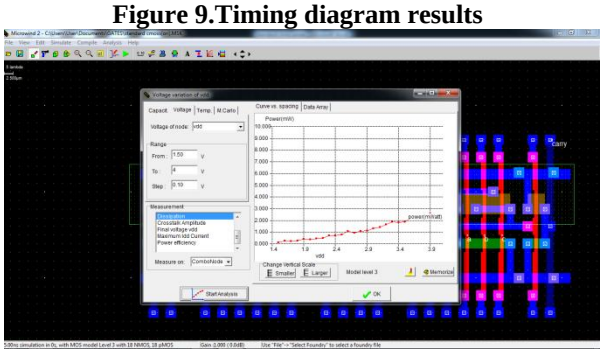

Figure 10.Power dissipation of standard CMOS adder.

The circuit of transmission gate full adder which is designed in Microwind tool is shownin fig.11

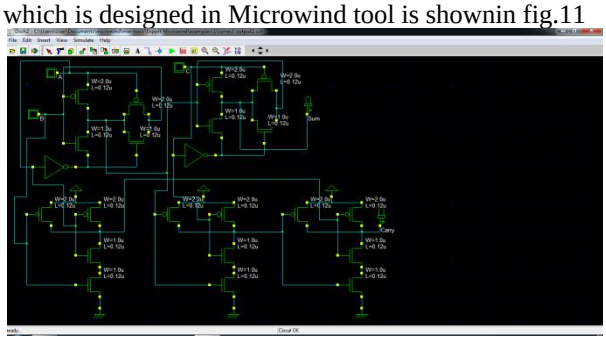

Figure 11.Transmission gate adder

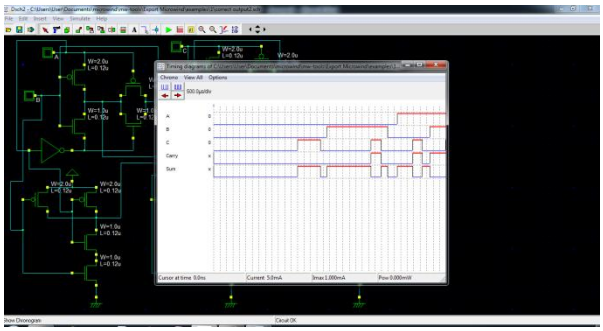

Figure 12. Timing diagram results

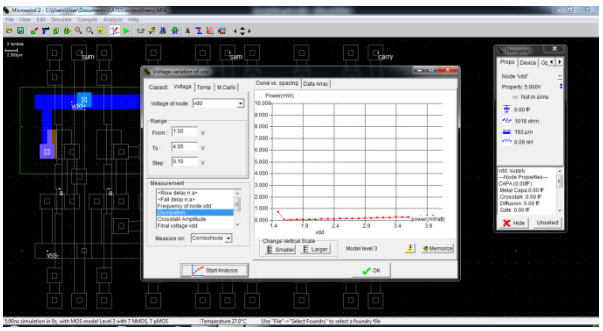

Figure 13. Power dissipation of transmission gate full adder

The circuit of square root based full adder which is designed in Microwind tool is shownin fig.14

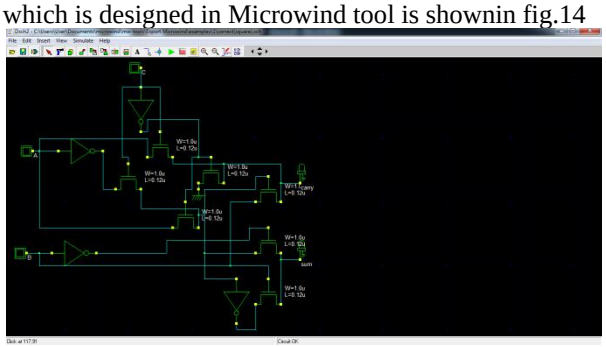

Figure 14. Circuit of square root based full adder

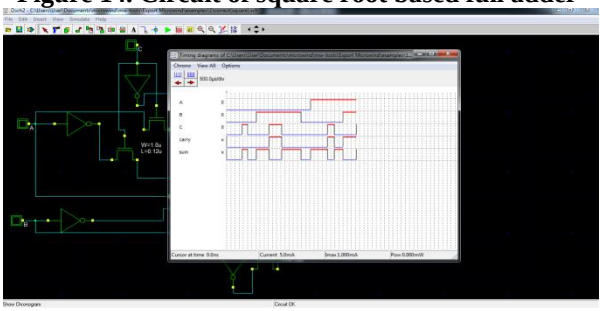

Figure 15. Timing diagram results

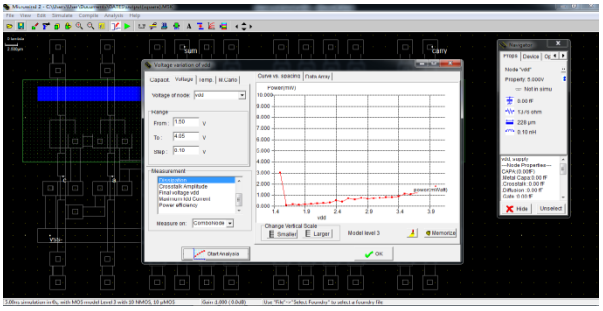

Figure 16. Power dissipation of square root based full adder

The circuit of static energy recover full adder which is designed in Microwind tool is shownin fig.17

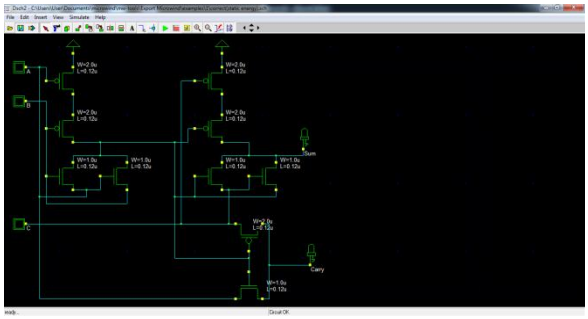

Figure 17. Circuit of static energy recover full adder

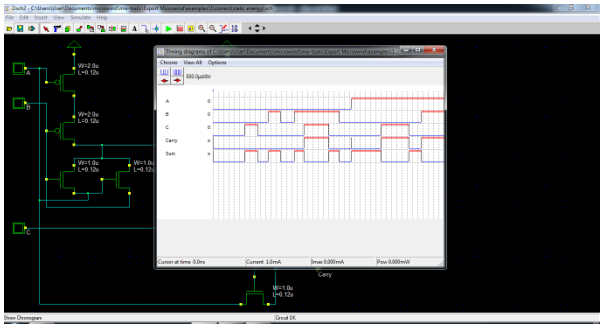

Figure 18. Timing diagram results

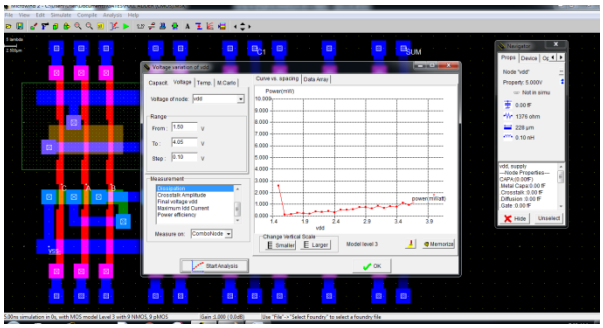

Figure 19. Power dissipation of static energy recovery full adder

The circuit of full adder using gates which is designed in Microwind tool is shownin fig.20

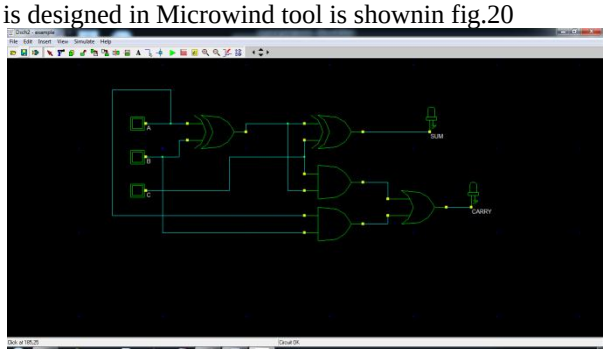

Figure 20. Circuit of full adder using gates

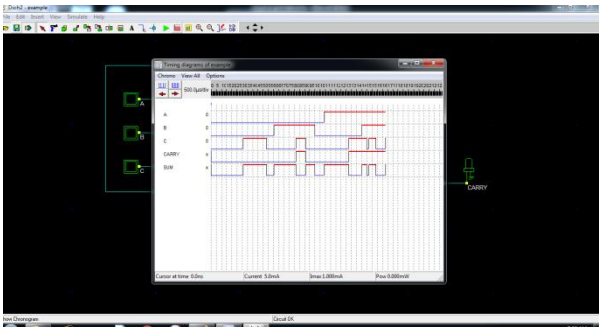

Figure 21. Timing diagram results

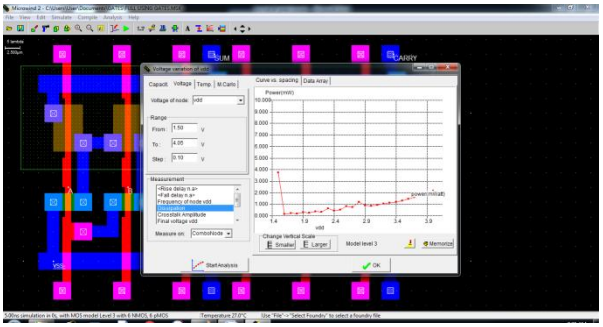

Figure 22.Power dissipation of recovery full adder using gates

COMPARISION TABLE

Design	Power Dissipation (mW)	Number of transistors
Full adder using gates	3.745	-
Standard CMOS full adder	2.645	28
Transmission gate full adder	0.707	20
Square root based full adder	3.015	15
Static energy recovery full adder	2.570	10

Table 1.Comparision of adder-Power dissipation

IV. CONCLUSION

This work presents many important points that are used while selecting a suitable low power adder. The simulation results show no significant difference between a CMOS full adder, transmission gate full adder, square root based full adder, static energy recovery full adder when compared with the full adder designed using gates. Transmission gate adder in terms of their output response, making them a suitable choice for replacing the conventional adder. The remaining two adders that is the square root based full adder and static energy recovery full adder may consume very less power but are compromising in their output voltage levels.

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