SSRG International Journal of Electronics and Communication Engineering
ISSN: 2348-8549/ https://doi.org/10.14445/23488549/IJECE-V11I6P106

Volume 11 Issue 6, 63-73, June 2024

Original Article

Low-Power and High-SFDR Current Steering DAC Design in 65-nm CMOS Using C-DEM Method

Ashok Kumar Adepu[1,2], Balaji Narayanam[1]

[1]*Department of Electronics and Communication Engineering, Jawaharlal Nehru Technological University Kakinada, Kakinada, Andhra Pradesh, India.*
[2]*Department of Electronics and Communication Engineering, MVGR College of Engineering, Vizianagaram, Andhra Pradesh, India.*

[1]*Corresponding Author : adepuashokkumar@gmail.com*

Received: 12 April 2024 Revised: 23 May 2024 Accepted: 08 June 2024 Published: 29 June 2024

Abstract *- Wireless Sensor Networks (WSNs) with low power consumption are getting more and more important. This work introduces an innovative low-power Digital-to-Analog Converters (DACs) architecture designed specifically for operating low-power WSNs. The emphasis is placed on the essential role of DACs within WSNs, acknowledging their significant power consumption. This study presents a Compact Dynamic Element Matching (C-DEM) method, aiming to mitigate the power and area redundancies associated with conventional DEM techniques and to achieve power and area efficiency through the implementation of C-DEM. Dynamic element matching stands out as a widely recognized technique employed in the design of high-performance DACs. The present research was motivated by the noteworthy finding that DAC input data typically displays appropriate randomness. As an alternative to the traditional reliance on a Pseudo Random Number Generator (PRNG) in usual DEM approaches, this feature allows using the input data itself for random selection of current sources. When the PRNG is removed from a DAC and input data is used instead, the DAC's space and power consumption are significantly reduced while still providing the performance requirements of low-power WSNs. This is brought on by the PRNG's high power requirements and substantial DAC footprint. In comparison to a DAC employing the traditional DEM, the C-DEM-based DAC consumes less power and area reduction. In the proposed C-DEM, when DAC uses a traditional DEM, the Spurious-Free Dynamic Range (SFDR) is not as good.*

Keywords *- Cascode current source, Differential Non-Linearity (DNL), Integral Non-Linearity (INL), Barrel shifter, SFDR, C-DEM.*

1. Introduction

Wireless Sensor Nodes (WSN) have come a long way, but they still have one major drawback: power consumption. Due to power consumption, the service life of the majority of wireless sensor nodes is severely constrained [1]. As a result, extensive research has been done to reduce WSN nodes' energy usage. For instance, research and development are being done on low-power processors for wireless sensor nodes. Adopting low-power network protocols is another strategy for low-power sensor nodes [2]. Digital-to-Analog Converters (DAC) which is usually power-hungry elements in a wireless sensor node. So, for the last two decades, researchers have been trying to design low-power and high-performance (particularly when Spurious Free Dynamic Range (SFDR) is high) DACs [3-5]. However, these DACs require significant effort to minimize mismatched induced nonlinearities. However, this approach faces challenges in terms of compromised dynamic performance at elevated frequencies and sustains a substantial area penalty. On the other hand, the background calibration technique, particularly the Dynamic-Element-Matching (DEM) method, efficiently mitigates the adverse impacts of mismatch-induced nonlinearities on the dynamic performance of the DAC, successfully avoiding the previously mentioned drawbacks [6, 7]. The array of unary current sources is randomly selected in DEM. Unsigned current cells are used in the construction of the strongly weighted segments, including the MSB segments, and DEM blocks independently control each segment. On the other hand, the digital input directly controls the binary current cells that make up the LSB segments. SFDR performance is enhanced by increasing the bit width, particularly for the MSB; the DEM block's circuit complexity grows instantly as the bit width increases. Additionally, digital blocks with higher stage numbers introduce a time skew issue. Consequently, state-of-the-art designs usually limit the width of the MSB bit to fewer than five bits [8-14]. This restriction frequently limits the attainable SFDR performance. To eliminate the limitation mentioned above, nested segmented

DEM DACs have been implemented [15]. Although high SFDR has been achieved in nested segmented DEM DACs, they require high operating power and footprint area. Hence, this research focuses on the DAC and introduces a novel design technique that significantly lowers the power consumption of the DAC, a crucial component of the wireless sensor node's transmitter. To achieve this, first analyse the power requirements of traditional current-steering DAC architectures commonly found in transmitters [16]. They focus on the shortcomings of traditional methods and techniques for DAC designs that place a higher priority on high efficiency, as shown by sampling frequency and S FDR. The related energy and area overhead have increased, even if the prior approaches for the high SFDR DAC were successful in producing the intended outcome [17].

This is because the earlier solutions call for additional, heavily power-intensive circuitries with a big footprint. However, the creation of a compact, low-power DAC is the main objective of this work. Introduce an innovative design technique that, following a thorough analysis of the power and space overhead associated with existing technologies [8–12], has the potential to deliver comparable performance while significantly reducing power consumption and spatial requirements. The DEM method serves as the foundation for the suggested method, which is among the earlier methods most reliable for high SFDR. In current steering Digital-to-Analog Converters (DACs), there are several research gaps and challenges that need to be addressed to improve performance and adaptability in various applications. Here are some of the primary research gaps and issues.

1.1. Linearity and Distortion

Problem: Achieving high linearity in current steering DACs is challenging due to mismatches and non-idealities in the current sources. Research Gap: Developing techniques to improve matching accuracy and reduce distortion is crucial. This involves both design-level innovations and advancements in fabrication processes.

1.2. Dynamic Performance

Problem: Maintaining high-speed performance without compromising accuracy is difficult. Research Gap: To enhance the dynamic performance of current steering DACs, specifically in minimizing glitches and enhancing settling time, further research is necessary**.** Investigating novel circuit topologies and layout techniques could be beneficial.

1.3. Power Efficiency

Problem: Balancing power consumption with performance requirements is a key challenge. Research Gap: Innovative power-saving techniques, such as dynamic power management and efficient biassing schemes, need further exploration. The aim is to enhance power efficiency without sacrificing speed or accuracy. For more details, the main stages of the proposed approach are as follows: The substantial power consumption of Digital-to-Analog Converters (DACs) is acknowledged, and their crucial significance in WSNs is emphasized. A Compact Dynamic Element Matching (C-DEM) method aims to mitigate the power and area redundancies associated with conventional DEM techniques and to achieve power and area efficiency through the implementation of C-DEM. C-DEM also simplifies the design by eliminating PRNG and reducing the active area of the DAC. When input data is utilized in place of the PRNG in a DAC, the DAC's area and power consumption are drastically decreased while still meeting low-power WSN performance requirements. The following describes the way the paper is established: Section I illustrates the introduction. Section II provides a description of the relevant works. Section III describes the proposed techniques, Section IV displays the simulation results, and Section V provides a summary.

2. Related Work

In a current-steering DAC, this brief suggests a method for glitch minimization via Compensating for dynamic capacitance in binary-weighted current switches (DAC) [18]. This study proposes a novel type of current-steering Digital-to-Analog Converter (DAC) based on Differential-Quad Switching (DQS) with excellent efficiency and no tuning required. It operates at 500 MS/s and has a 14-bit resolution. Enhancing the spurious-free dynamic range involves minimizing input-code transition-dependent distortion through DQS and suppressing element mismatch-related harmonics using GRTC. The current cell design method is provided in this paper to reduce random mismatches [19].

The gradient mismatch is subsequently fixed with a novel Data-Weighted Averaging (DWA) method, which is less buggy and needs less expensive hardware. The proposed DAC successfully achieves SFDR augmentation, and complexity is also low by adopting both the row-column structure and the (CSA) structure as its ground plan. Using the Dynamic Element Matching (DEM) method, a two-dimensional DAC structure is compressed. In contrast to the DAC's utilization of a segmented structure for implementing DEM [18], the novel structure introduces randomization to inter-segmentation errors. High precision and performance levels are available with this structure. In this study, a non-uniform sine-weighted DAC was employed to construct the Direct Digital Frequency Synthesizer (DDFS) DAC. Parallel DACs, employed to speed up relaxation within a single DAC, along with the utilization of the Return-to-Zero (RZ) technique, were implemented to generate signals approaching and surpassing the Nyquist rate without the need for a tough filter. To minimize space and power requirements in parallel DACs, a design strategy featuring a non-uniform sine-weighted DAC was introduced [13]. To address the mismatch issue that results in SFDR degradation, the DEM approach has been recommended [18, 19]. It also requires a randomizer, which is commonly made with the barrel shifter, to choose the current sources at random (PRNG). The low-power barrel shifter was introduced [23-

25]. In this paper [24], the barrel shifter was designed using different techniques, such as mux and conventional CMOS logic. In terms of power consumption, barrel shifters with mux are more efficient than those with traditional CMOS circuitry, delay and transistor count because it shows 76.37% less power consumption and 57.14% less number of transistors than conventional CMOS logic. A low-power dynamic barrel shifter based on mux was designed using footed diode domino logic [25]. This paper compares and analyses barrel shifters using footed diode domino multiplexer and pseudo-NMOS multiplexer architectures. Power is reduced by 99.97% for footed diode domino-based multiplexer. The barrel shifter implemented using a footed diode domino multiplexer consumes 92.02% less power than a pseudo-NMOS-based multiplexer.

The literature on low-power and high-SFDR current steering DACs reveals a variety of techniques aimed at optimizing low-power and high-SFDR design techniques. Low-power design approaches are primarily focused on efficient biasing and switching techniques. For high SFDR, strategies revolve around improving matching and calibration, minimizing glitches, and reducing noise. Future research is likely to continue exploring these areas, with an increasing emphasis on integrating digital calibration and leveraging new materials and processes.

3. Proposed Method

The proposed technique in this paper, which targets low-power and high SFDR DACs, is called a compact DEM (C-DEM). This work is unique in that it involves designing a 12-bit DAC using a nested segment structure method with 3-level segmentation [3U+3U+3U+3B]. The entire architecture of the proposed DAC design is displayed in Figure 1.

The study that shows the PRNG in the randomizer adds a lot of extra power and space to a DAC using the RRBS DEM is what led to the idea of getting rid of the PRNG in the DAC while still using enough random input data. The PRNG should be removed, eliminating the power and space overhead it causes. The rotation number is then set by the input data's unpredictability, preserving the DAC's SFDR performance.

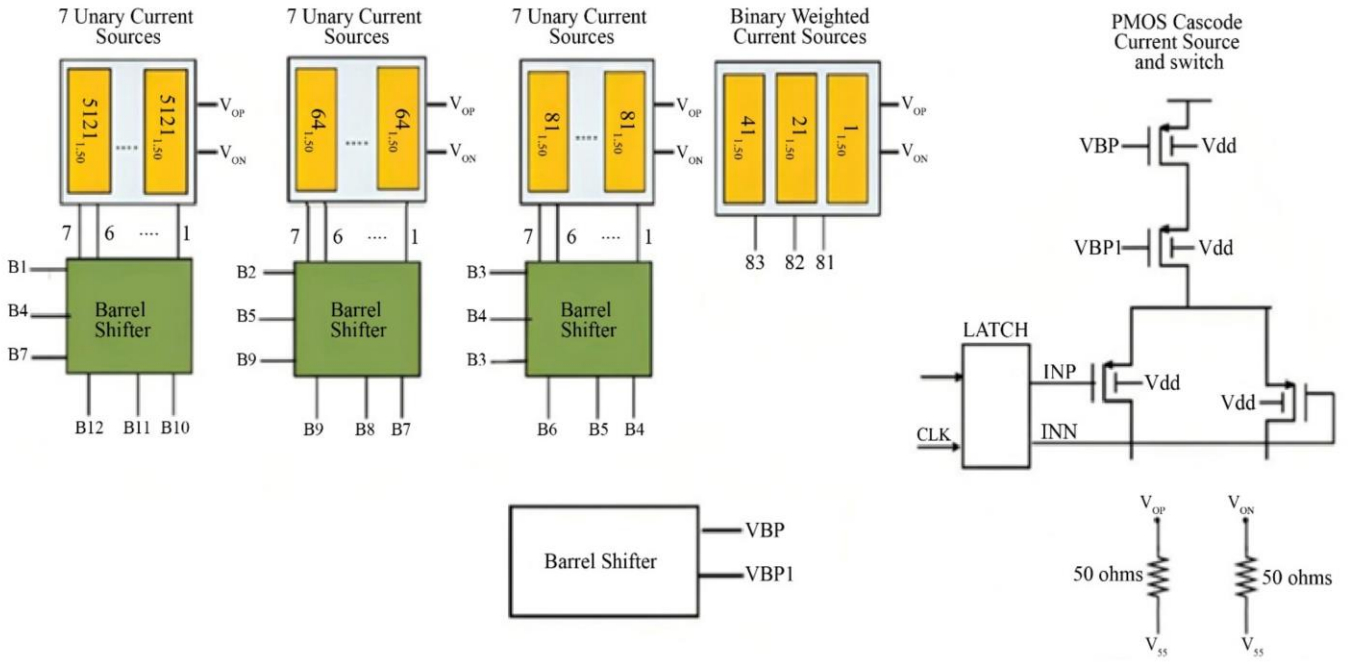

Fig. 1 Proposed C-DEM architecture for the 12-bit DAC without PRNG

The proposed method uses a single input code for a sample period, while the PRNG used in the conventional DEM method generates a random bit once each sample period, therefore, there is no additional overhead based on sample rate. The logarithmic barrel shifter, as seen in Figure 2, is an additional design option for multiple data shifting; an integrated circuit with n inputs, n outputs, and m select lines that are intended to manage bit shift operations is called a barrel shifter.

Numerous irreversible barrel shifters have been developed as a result of the fact that multiple and variable bit shifting is preferable to single-bit operations.

Barrel shifters come in two varieties: unidirectional, which can only rotate or shift in one direction (to the left or right), and bidirectional, which can do both.

Barrel Shifter

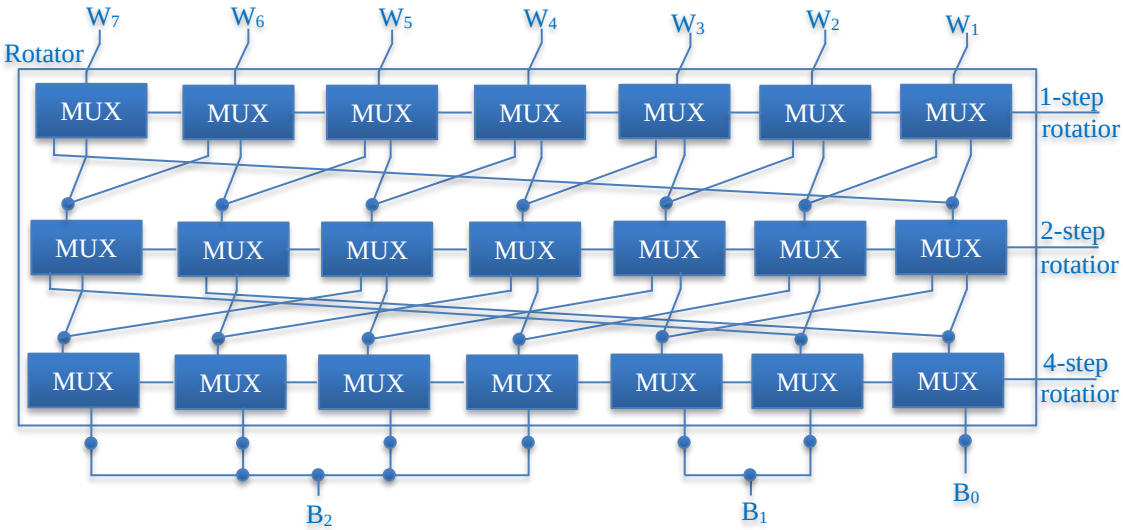

Fig. 2 3-bit barrel shifter with 1-step, 2-step and 3-step rotations

Modified Gate Diffusion Input (MGDI) based 2:1 Multiplexer

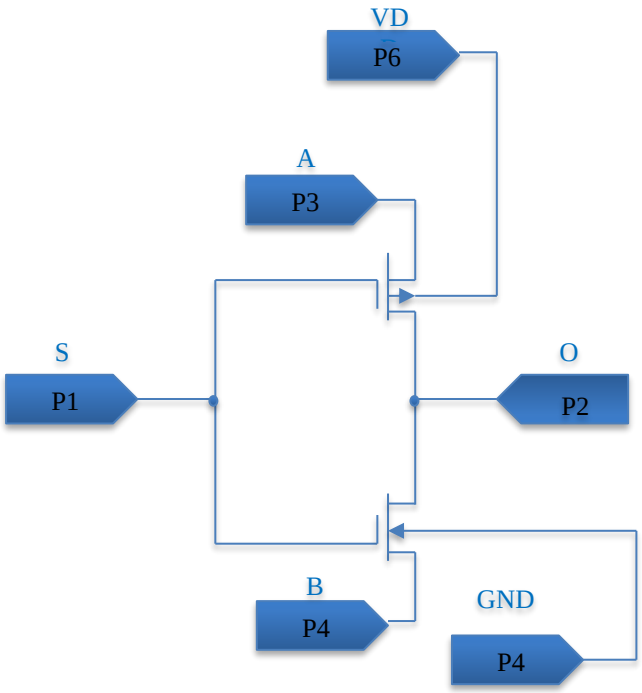

Fig. 3 3-bit barrel shifter with 1-step, 2-step and 3-step rotations

As shown in Figure 3, the Modified GDI logic circuit. The modified GDI-based multiplexer functions similarly to the PMOS and NMOS transistors used in the GDI technique. The substrate terminal of an NMOS transistor is connected to the ground, and the substrate terminal of a PMOS transistor is connected to VDD. Thus, the circuit differs from the GDI technique-based multiplexer circuit, which is made to improve logic level swings. Signal A is applied to the source terminal of the PMOS transistor, and Signal B is applied to the source terminal of the NMOS transistor.

Both of the transistors' gate terminals receive signal S as an input. With the exception of the deviation, which can be either from the ground if the output is low or from VDD if the output is high, the output has improved when compared to the GDI technique in terms of delay, power, and power delay product.

4. Simulation Results

The 2:1 multiplexer's schematic diagram is shown in Figure 4.

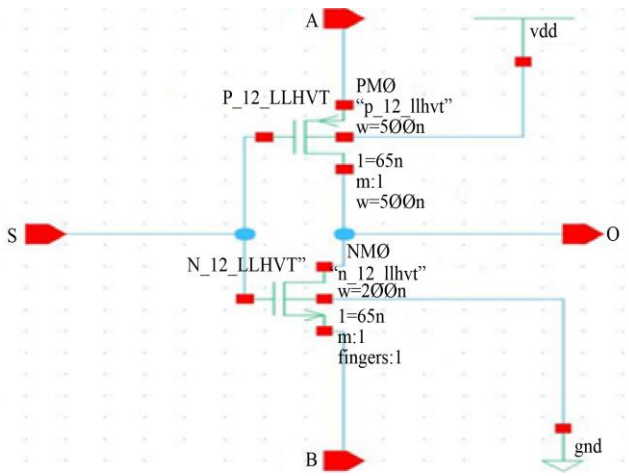

Fig. 4 Diagram for the 2:1 multiplexer

The simulation result of the 2:1 multiplexer is shown in Figure 5.

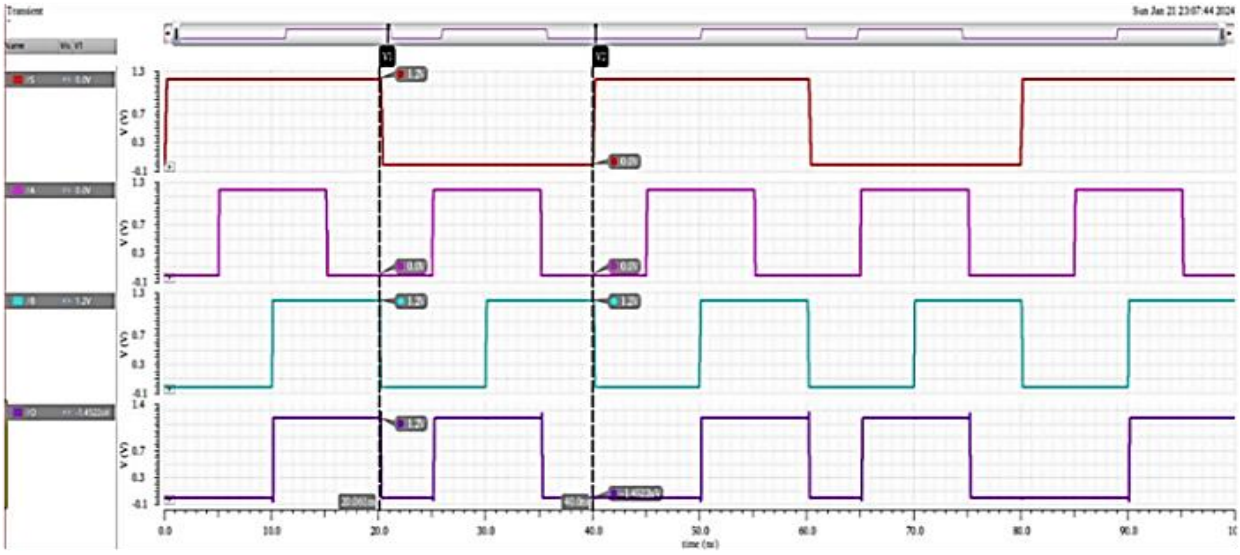

Fig. 5 Multiplexer simulation result of 2:1 multiplexer

Figure 6 displays the power waveform of an MGDI-based multiplexer.

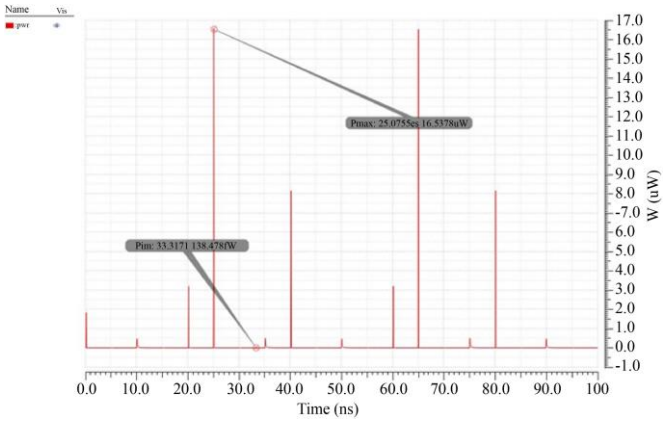

Fig. 6 Power waveform of MGDI based multiplexer

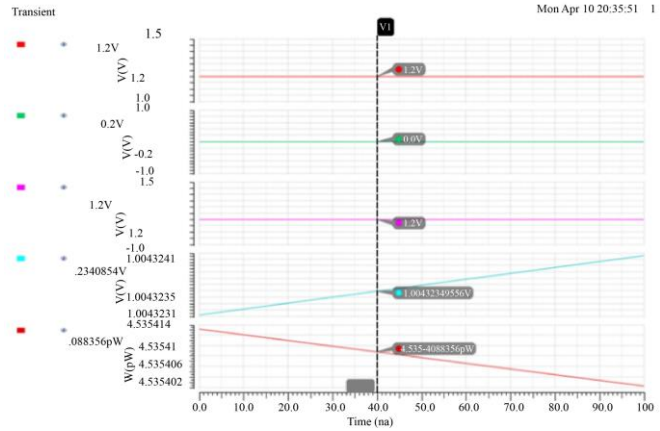

Fig. 7 Static power analysis of MGDI based multiplexer

The MGDI technique is implemented to overcome the drawback of the GDI technique, that is, to obtain a better output voltage swing. The design is similar to that of the GDI technique but differs in the connection of bulk terminals of the transistors. Even the power dissipations are reduced. The minimum power dissipated is 138.478fWatts, and the maximum power dissipated is 16.5378uWatts. Figure 7 shows the static power analysis of the MGDI-based multiplexer. If the selection signal (S) is set to 1.2V, SBAR, which is considered as 0V, and the input signals applied as A with 0V and B with 1.2V, the output voltage obtained is 1.00432349858V and the power consumption is 4.5354088356pWatts. When compared to other multiplexers modified GDI-based multiplexers consumed less power. The average power dissipation for a modified GDI-based multiplexer is 16.67 n watts, with maximum and minimum power dissipation of 16.54uwatts and 138.5 f watts. The Modified GDI-based multiplexer exhibits a static power dissipation of 4.535 p watts. This MGDI-based multiplexer is used in the design of a 3-bit barrel shifter using a 2x1 configuration.

The required area is reduced in GDI and MGDI techniques compared to the remaining techniques shown in Table 1. On comparing the average power of all the different techniques, the least is for the MGDI technique, which is 16.67nwatts. Coming to the delay, it should be less indicating the device speed is high. Delay values of all the techniques are almost similar to each other.

However, the least delay is observed for the transmission gate technique, which is 5.013 seconds. Multiplying the average power with the delay related to the respective multiplexers yields the Power Delay Product (PDP). So, it is desired to be low. Moreover, it is less for the MGDI technique, which is 84.85×10^-18. So, out of all the techniques, GDI and MGDI techniques have reasonable powers and delay; thus, these techniques are considered for further analysis.

4.1. Static Power Dissipation

In the static power dissipation analysis, the output power is calculated by setting all the signals at constant input. There are state transitions in the dynamic power dissipation from high to low or from low to high. For designing a 3-bit barrel shifter, 21 2:1 Multiplexers are required. The 3-bit barrel shifter-right rotator is shown in Figure 8.

Table 1. Comparison of various 2:1 multiplexer design techniques

2:1 Multiplexer design based on	Total number of Transistors required	Static power dissipation	Average power
Pass Transistor	4	9.956pw	42.46nw
Static CMOS	12	25.43pw	256.1nw
Domino Logic	10	17.75pw	232.1nw
GDI	2	11.18pw	59.92nw
MGDI	2	4.535pw	16.67nw

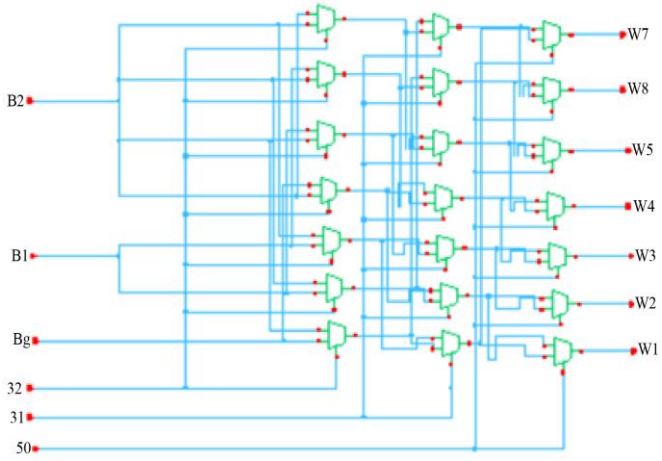

Fig. 8 3-bit barrel shifter-right rotator

The output waveforms of the MGDI-based barrel shifter are displayed in Figure 9.

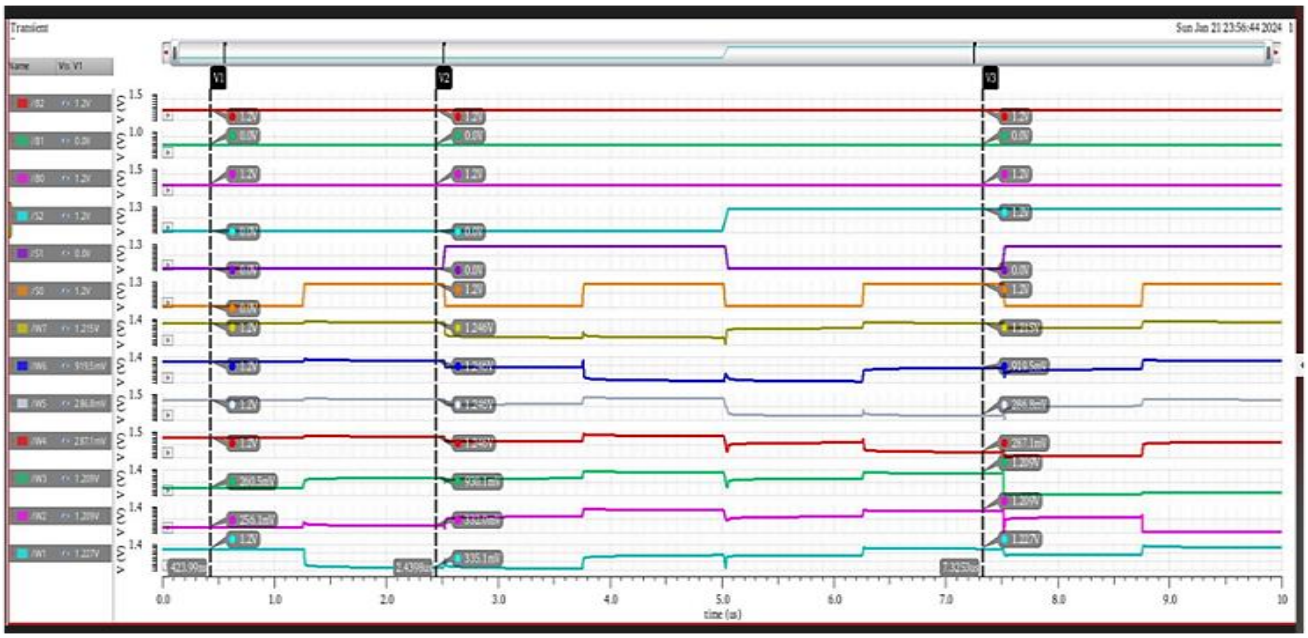

Fig. 9 Output waveforms of MGDI-based barrel shifter

It consists of three stages where each stage output is connected to the next stage inputs. The first stage of multiplexers is capable of performing 4-bit right rotation, the second stage of multiplexers is capable of performing 2-bit right rotation, and the third stage of multiplexers is capable of performing 1-bit right rotation. B2 B1 B0 are the input signals, S2 S1 S0 are the control signals and W7 W6 W5 W4 W3 W2 W1 are the output signals.

Various MGDI comparison time periods are shown in Table 2. When input signal B2B1 B0=101, Table 3 displays combinations of selection signals along with their matching outputs. A 3-bit barrel shifter with right rotation is implemented in Cadence virtuoso tool at 65nm technology and verified the outputs with combinations of selection signals.

4.2. Proposed C-DEM Architecture

Figure 10 illustrates the proposed C-DEM design (3U+3U+3U+3B) for the 12-bit DAC.

Table 2. Timing values

Selection signals	Time period (nsec)	Pulse width (nsec)	Delay (nsec)
S2	40	20	20
S1	20	10	10
S0	10	5	5

Table 3. Combinations of selection signals stand their corresponding outputs

Selection signals			Output signals						
S_2	S_1	S_0	W_7	W_6	W_5	W_4	W_3	W_2	W_1
0	0	0	1	1	1	1	0	0	1
0	0	1	1	1	1	1	1	0	0
0	1	0	0	1	1	1	1	1	0
0	1	1	0	0	1	1	1	1	1
1	0	0	1	0	0	1	1	1	1
1	0	1	1	1	0	0	1	1	1
1	1	0	1	1	1	0	0	1	1
1	1	1	1	1	1	1	0	0	1

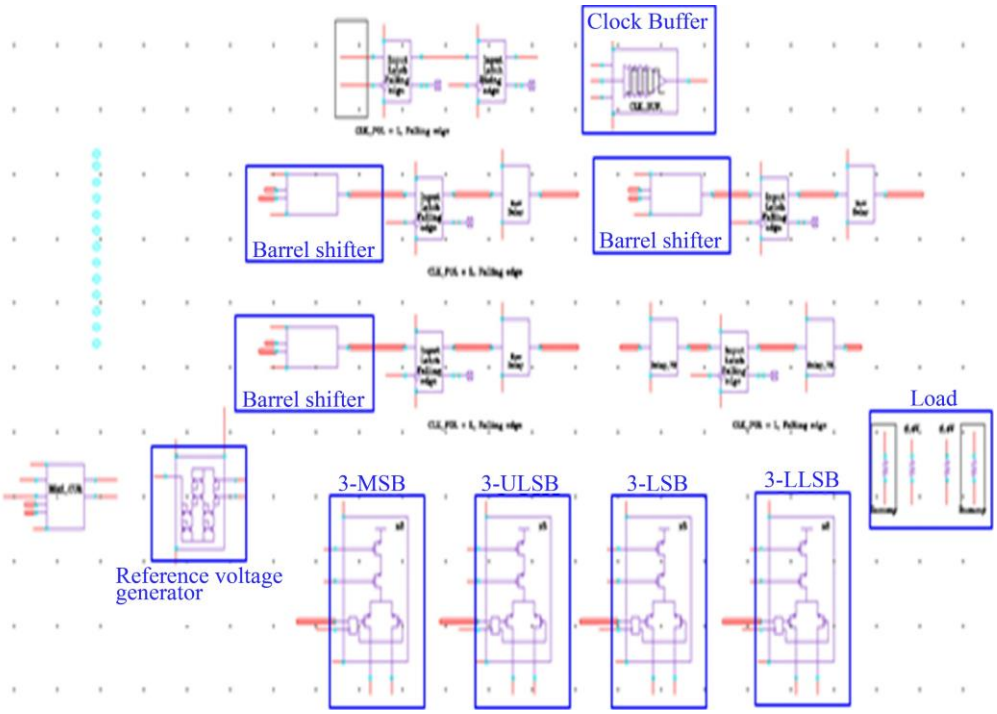

Fig. 10 Proposed C-DEM architecture (3U+3U+3U+3B) for the 12-bit DAC

The proposed C-DEM DAC core's layout is shown in Figure 11.

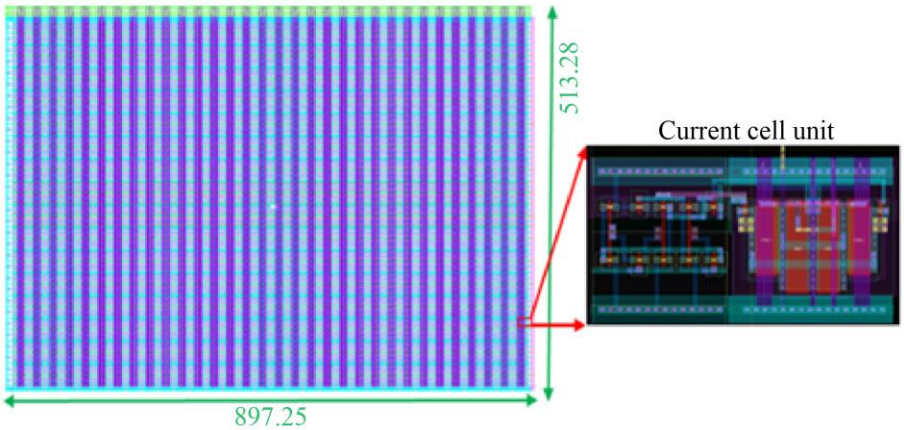

Fig. 11 Layout of proposed C-DEM DAC core

4.3. INL & DNL of C-DEM DAC Core

Table 4. Simulation result of proposed 12-bit C-DEM architecture

Parameters	Proposed Compact DEM
Resolution	12 Bit
Technology (nm)	65
Supply Voltage (V)	1.2
Sample rate (MS/s)	100
ENOB (bits)	11.805
SNR (dB)	72.834
SFDR (dB)	79.14
DNL(LSB)	0.04
INL(LSB)	0.26
P_{total} (mW)	6.996
I_{load} (mA)	5.83

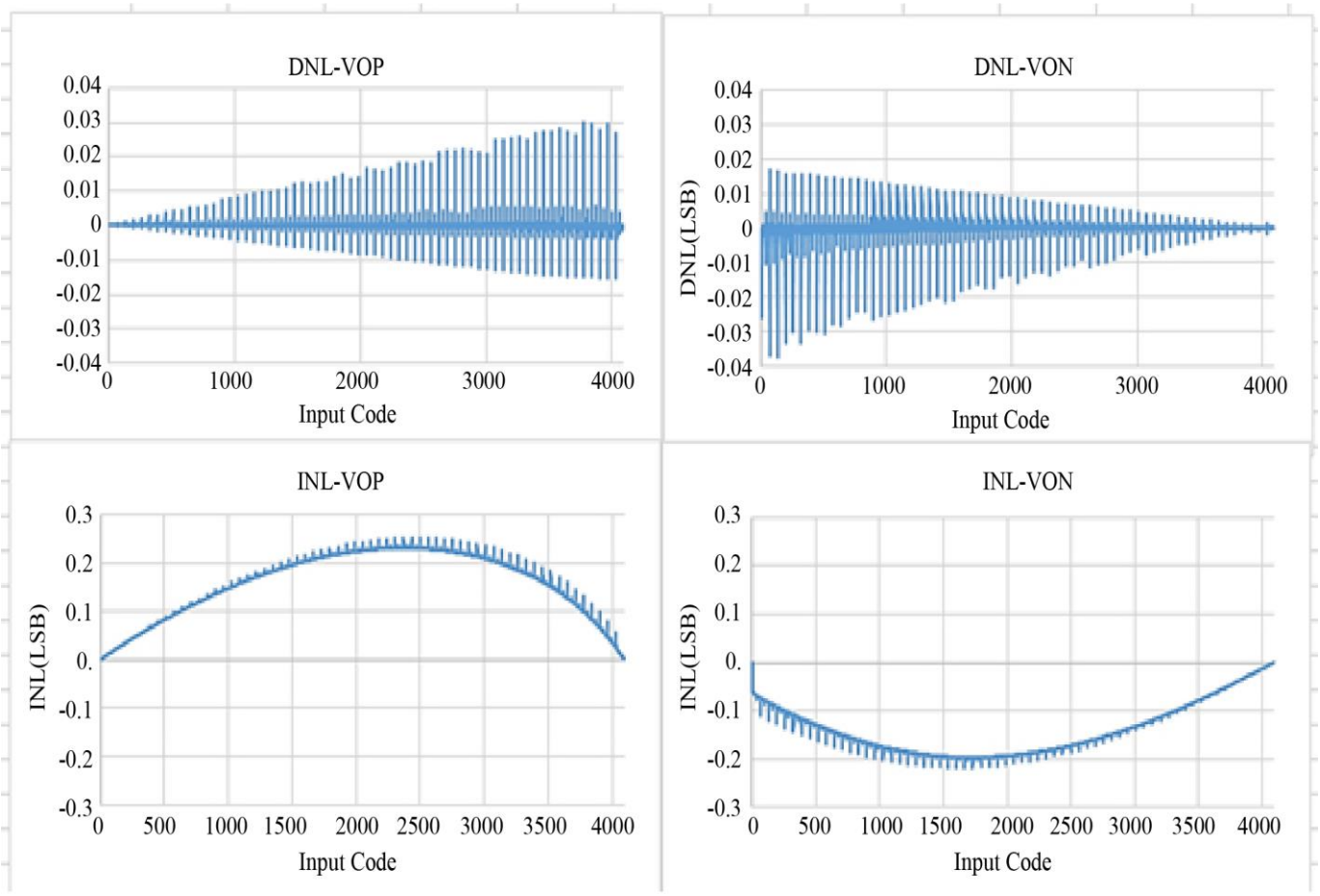

Fig. 12 DACs' measured static performance (INL & DNL)

Table 4 presents the results of the simulation for the proposed 12-bit C-DEM architecture. The performance of static linearity is tested both with and without the DEM block enabled. The related measured Integral Nonlinearity (INL) values are shown in Figure 12. The intersegment mismatches have the greatest impact on the INL error for segmented DACs with thermometer-coded units. The dynamic performance of the DAC is shown in Figure 13.

A comparison of various DAC metrics, such as power consumption and SFDR, between the proposed current steering DAC and the present DACs is carried out in Table 5.

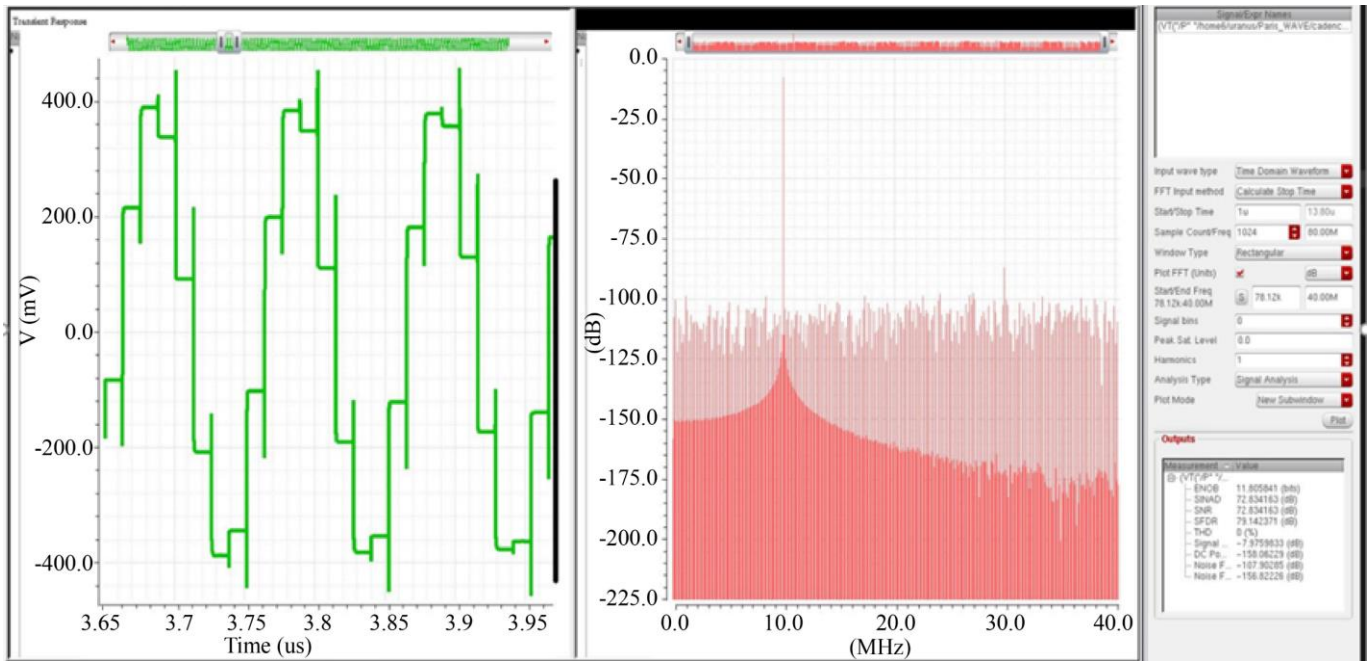

Fig. 13 DAC dynamic performance

Table 5. Comparison of the state-of-the-art of the current steering DAC

Parameters	This work	Ref. [21] (Nested Segment-DEM)	Ref. [19] (GRTC-DEM)	Ref. [20] (DRZ-DEM)	Ref. [15] (RRBS-DEM)	Ref. [18] Glitch energy & SFDR
Resolution	12 bit	12	14	12	10	10
Technology (nm)	65	130	180	40	180	180
Sample rate(MS/s)	100	100	500	1600	500	400
SFDR(dB)	79.14	62.1	68.9	74	61	58
P_{total} (mW)	6.996	18	67.7	40	24	20.7
I_{load} (mA)	5.83	16	10	16	10	--

5. Conclusion

This summary outlines the introduction of a 12-bit, 100 MS/s current-steering DAC that incorporates a novel compact DEM method. The demonstrated C-DEM method has been proven to deliver superior static and dynamic performance compared to traditional segmented structures. As stated at the beginning of this paper, the conventional DEM technique is employed to improve the SFDR performance of DACs. The randomizer for the DEM approach can eliminate the randomizer's PRNG, saving a significant amount of power and space by selecting the constant current at random using the input data rather than the PRNG. This is because the Pseudo-Random Generator (PRNG) in a DAC has unavoidably high power and space requirements. In this work, a low-power 3-bit barrel shifter has been designed using less number of transistors. The proposed DAC uses two fewer MSBs for DEM and performs similarly to traditional ones. Lowering the MUX count considerably simplifies the DEM block in comparison to nested segment structures, RRBS, and GRTC approaches.

According to the simulation results, the introduced architecture exhibits low power consumption at 6.99 mW and achieves a high SFDR of 79.14 dB. Linearity is also improved by achieving INL and DNL values of 0.26 and 0.04. In addition, the C-DEM also simplifies the design by eliminating PRNG and reducing the active area of the DAC.

Acknowledgments

The author would like to express his heartfelt gratitude to the supervisor for his guidance and unwavering support during this research for his guidance and support.

References

[1] Subin Choi et al., "A Multisensor Mobile Interface for Industrial Environment and Healthcare Monitoring," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 3, pp. 2344-2352, 2017. [CrossRef] [Google Scholar] [Publisher Link]

[2] Byungjoo Oh, Kyeonghwan Park, and Jae Joon Kim, "A Triple-Mode Performance-Optimized Reconfigurable Incremental ADC for Smart Sensor Applications," *IEEE Access*, vol. 7, pp. 19013-19023, 2019. [CrossRef] [Google Scholar] [Publisher Link]

[3] Meng-Hung Shen, Jen-Huan Tsai, and Po-Chiun Huang, "Random Swapping Dynamic Element Matching Technique for Glitch Energy Minimization in Current-Steering DAC," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 57, no. 5, pp. 369-373, 2010. [CrossRef] [Google Scholar] [Publisher Link]

[4] Wei-Te Lin, and Tai-Haur Kuo, "A Compact Dynamic-Performance-Improved Current-Steering DAC with Random Rotation-Based Binary-Weighted Selection," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 2, pp. 444-453, 2012. [CrossRef] [Google Scholar] [Publisher Link]

[5] Wei-Hsin Tseng, Chi-Wei Fan, and Jieh-Tsorng Wu, "A 12-Bit 1.25-GS/s DAC in 90 nm CMOS With >70 dB SFDR up to 500 MHz ," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 12, pp. 2845-2856, 2011. [CrossRef] [Google Scholar] [Publisher Link]

[6] A.R. Bugeja, and Bang-Sup Song, "A Self-Trimming 14-b 100-MS/s CMOS DAC," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 12, pp. 1841-1852, 2000. [CrossRef] [Google Scholar] [Publisher Link]

[7] Tao Chen, and Georges G.E. Gielen, "A 14-Bit 200-MHz Current-Steering DAC with Switching-Sequence Post-Adjustment Calibration," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 11, pp. 2386-239, 2007. [CrossRef] [Google Scholar] [Publisher Link]

[8] M. Vesterbacka et al., "Dynamic Element Matching in D/A Converters with Restricted Scrambling," *ICECS 2000. 7th IEEE International Conference on Electronics, Circuits and Systems*, Jounieh, Lebanon, vol. 1, pp. 36-39, 2000. [CrossRef] [Google Scholar] [Publisher Link]

[9] Niklas U. Andersson et al., "Models and Implementation of a Dynamic Element Matching DAC," *Analog Integrated Circuits and Signal Processing*, vol. 34, pp. 7-16, 2003. [CrossRef] [Google Scholar] [Publisher Link]

[10] Meng-Hung Shen, Jen-Huan Tsai, and Po-Chiun Huang, "Random Swapping Dynamic Element Matching Technique for Glitch Energy Minimization in Current-Steering DAC," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 57, no. 5, pp. 369-373, 2010. [CrossRef] [Google Scholar] [Publisher Link]

[11] Wei-Te Lin, and Tai-Haur Kuo, "A Compact Dynamic-Performance-Improved Current-Steering DAC with Random Rotation-Based Binary-Weighted Selection," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 2, pp. 444-453, 2012. [CrossRef] [Google Scholar] [Publisher Link]

[12] Wei-Hsin Tseng, Chi-Wei Fan, and Jieh-Tsorng Wu, "A 12-Bit 1.25-GS/s DAC in 90 nm CMOS With >70 dB SFDR up to 500 MHz," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 12, pp. 2845-2856, 2011. [CrossRef] [Google Scholar] [Publisher Link]

[13] A.R. Bugeja, and Bang-Sup Song, "A Self-Trimming 14-b 100-MS/s CMOS DAC," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 12, pp. 1841-1852, 2000. [CrossRef] [Google Scholar] [Publisher Link]

[14] Longqiang Lai et al., "A 14-bit 500-MS/s DAC with 211-MHz 70 dB SFDR Bandwidth Using TRI-DEMRZ," *Analog Integrated Circuits and Signal Processing*, vol. 96, pp. 133-145, 2018. [CrossRef] [Google Scholar] [Publisher Link]

[15] Wei Mao et al., ''High Dynamic Performance Current-Steering DAC Design With Nested-Segment Structure," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 26, no. 5, pp. 995-999, 2018. [CrossRef] [Google Scholar] [Publisher Link]

[16] Usman Raza, Parag Kulkarni, and Mahesh Sooriyabandara, "Low Power Wide Area Networks: An Overview," *IEEE Communications Surveys & Tutorials*, vol. 19, no. 2, pp. 855-873, 2017. [CrossRef] [Google Scholar] [Publisher Link]

[17] Mike O. Ojo et al., "A Review of Low-End, Middle-End, and High-End Iot Devices," *IEEE Access*, vol. 6, pp. 70528-70554, 2018. [CrossRef] [Google Scholar] [Publisher Link]

[18] Fang-Ting Chou, and Chung-Chih Hung, "Glitch Energy Reduction and SFDR Enhancement Techniques for Low-Power Binary-Weighted Current-Steering DAC," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 24, no. 6, pp. 2407-2411, 2016. [CrossRef] [Google Scholar] [Publisher Link]

[19] Maliang Liu, Zhangming Zhu, and Yintang Yang, "A High-SFDR 14-bit 500 MS/s Current-Steering D/A Converter in 0.18 μ m CMOS," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 23, no. 12, pp. 3148-3152, 2015. [CrossRef] [Google Scholar] [Publisher Link]

[20] Wei-Te Lin, Hung-Yi Huang, and Tai-Haur Kuo, "A 12-bit 40 nm DAC Achieving SFDR > 70 dB at 1.6 GS/s and IMD < –61dB at 2.8 GS/s With DEMDRZ Technique," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 3, pp. 708-717, 2014. [CrossRef] [Google Scholar] [Publisher Link]

[21] Wei-Te Lin, and Tai-Haur Kuo, "A Compact Dynamic-Performance-Improved Current-Steering DAC with Random Rotation-Based Binary-Weighted Selection," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 2, pp. 444-453, 2011. [CrossRef] [Google Scholar] [Publisher Link]

[22] Meng-Hung Shen, Jen-Huan Tsai, and Po-Chiun Huang, "Random Swapping Dynamic Element Matching Technique for Glitch Energy Minimization in Current-Steering DAC," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 57, no. 5, pp. 369-373, 2010. [CrossRef] [Google Scholar] [Publisher Link]

[23] Poornima Mittal, Bhawna Rawat, and Nishant Kumar, "Tetra-Variate Scrutiny of Diverse Multiplexer Techniques for Designing a Barrel Shifter for Low Power Digital Circuits," *Microprocessors and Microsystems*, vol. 90, 2022. [CrossRef] [Google Scholar] [Publisher Link]

[24] Deepika Bhadauria, and Shweta Agrawal, "A Review on Barrel Shifter," *International Journal of Engineering Development and Research*, vol. 7, no. 1, pp. 241-244, 2019. [Publisher Link]

[25] N. Bharathesh Patel, and Manju Devi, "A Novel Low Power MUX Based Dynamic Barrel Shifter Using Footed Diode Domino Logic," *International Journal of Innovative Technology and Exploring Engineering*, vol. 8, no. 6S3, pp. 307-311, 2019. [Google Scholar] [Publisher Link]