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Original Article

Novel GaAs-on-Si MOSFET: A Breakthrough in Analog Performance over Conventional Si MOSFET

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Abstract *- The paper introduces a novel Gallium Arsenide on Silicon (GaAs-on-Si) MOSFET, formed by epitaxial deposition of a Galium Arsenide (GaAs) layer on a silicon substrate. This device offers significant improvements in analog performance over conventional Silicon MOSFETs, with a 40% increase in on-state current (ION) due to the higher electron mobility of GaAs. The paper provides a comparative analysis of the electrical characteristics and performance parameters, demonstrating the superiority of the GaAs-on-Si MOSFET. The device structure utilizes a planar configuration with GaAs as the channel material on a Si substrate fabricated through a cost-effective Molecular Beam Epitaxial (MBE) process. The study highlights enhanced analog performance metrics, making the GaAs-on-Si MOSFET a promising candidate for high-frequency and analog applications. The findings suggest that integrating GaAs with established Si technology can lead to significant advancements in semiconductor devices, offering better performance for analog integrated circuits and Radio Frequency (RF) applications. The fabrication process and detailed performance analysis underscore the potential of this novel device in advancing semiconductor technology, inspiring optimism for the future of semiconductor research and development.*

Keywords *- GaAs-on-Si MOSFET, Analog characteristics, Gate capacitance, Unity gain frequency, Output transconductance.*

1. Introduction

Silicon (Si) has long been the cornerstone of the semiconductor industry due to its advantageous properties. However, as the demand for high-performance devices increases, the limitations of silicon, particularly its electron mobility, become more pronounced. Researchers have turned to materials with higher electron mobility, such as GaAs, to enhance device performance. With its superior electron mobility, GaAs are a promising candidate for replacing or complementing silicon in specific applications. To harness the benefits of GaAs while maintaining the advantages of silicon, a novel device named GaAs-on-Si MOSFET has been proposed. This device involves the epitaxial deposition of a GaAs layer on a silicon substrate, combining the high electron mobility of GaAs with the well-established silicon technology. This device structure's Molecular Beam Epitaxial (MBE) process offers a cost-effective method to enhance device performance. Previous studies have shown that this approach can significantly increase ION and other key performance metrics.

The analog performance parameters, such as C_{GG}, F_T, G_M, and the G_M/I_D ratio, are critical indicators of a MOSFET's suitability for high-frequency and analog applications. In the proposed GaAs-on-Si MOSFET, a reduction in C_{GG} is observed due to the lower insulating area generated between the inversion layer and the substrate, resulting from the deposition of GaAs on Si [6, 7]. This lower capacitance is beneficial for high-frequency applications, as it minimizes the capacitive loading effects, thereby enhancing the device's speed [8, 9]. F_T is another vital parameter that indicates the frequency at which the transistor's current gain drops to unity. The GaAs-on-Si MOSFET exhibits a higher F_T compared to conventional Si MOSFETs, primarily due to the higher electron mobility of GaAs, which facilitates faster switching [10, 11]. This improvement in F_T is significant for RF applications, where high-frequency performance is essential. Additionally, the higher F_T ensures better performance in analog circuits, where bandwidth and speed are critical [12, 13].

G_M and the G_M/I_D ratio are measures of a MOSFET's efficiency in converting gate voltage changes into drain current changes. The proposed GaAs-on-Si MOSFET shows a notable improvement in G_M, indicating a more efficient control of the I_D by the gate voltage (V_G) [14, 15]. The greater electron mobility in the GaAs channel is the leading cause. Moreover, the subthreshold region's G_M/I_D ratio is enhanced, which is particularly advantageous for low-power analog applications [16]. The higher G_M/I_D ratio in the subthreshold

region implies that the device can achieve significant current drive with minimal power consumption, making it ideal for power-sensitive applications [17]. The GaAs-on-Si MOSFET's improved performance is mainly dependent on its manufacturing method. The use of MBE for depositing GaAs on Si ensures a high-quality and uniform GaAs layer, which is essential for achieving the desired electrical characteristics [18, 19].

The subsequent steps, including ion implantation for source and drain formation, gate oxide layer creation, and metallization, are carried out meticulously to maintain the GaAs layer's integrity and ensure optimal device performance [20, 21]. Carefully controlling these fabrication steps minimizes defects and dislocations, which could otherwise degrade the device's performance [22, 23].

The comparative analysis of the GaAs-on-Si MOSFET with conventional Si MOSFETs underscores the advantages of using GaAs as the channel material. GaAs' higher electron mobility enhances I_{ON} and improves other analog performance parameters, making the GaAs-on-Si MOSFET a promising candidate for high-frequency and analog applications [24, 25]. Integrating GaAs with silicon through MBE offers a feasible and cost-effective solution for achieving these performance improvements without sacrificing silicon technology's scalability and manufacturing advantages [26, 27]. Apart from these electrical properties, the effect of the GaAs-on-Si MOSFET on the device's overall performance is remarkable. Studies have shown that the device exhibits lower power consumption while maintaining high-speed operation, making it suitable for high-performance and energy-efficient applications [28, 29]. The enhanced thermal stability of GaAs also contributes to the device's robustness, enabling it to operate reliably under a wide range of temperatures [30, 31]. This characteristic is essential for applications in harsh environments where thermal management is critical.

Furthermore, the GaAs-on-Si MOSFET's potential for integration into existing silicon-based fabrication processes presents a significant advantage. This compatibility allows for the adoption of GaAs-on-Si technology in current semiconductor manufacturing without requiring extensive modifications, thereby reducing production costs and time [32, 33]. This approach's scalability guarantees that GaAs' advantages may be applied to various applications, including sophisticated communication systems and consumer electronics [34, 35]. The GaAs-on-Si MOSFET represents a significant advancement in semiconductor technology, offering superior performance for analog and high-frequency applications. The higher electron mobility of GaAs, combined with the well-established silicon technology, results in a device that outperforms conventional Si MOSFETs in key analog performance metrics. The careful fabrication process and the detailed performance analysis highlight the potential of the GaAs-on-Si MOSFET to revolutionize the semiconductor industry, paving the way for more efficient and high-performance electronic devices [36, 37].

Integrating GaAs with silicon through MBE offers a viable path for future innovations, ensuring that the semiconductor industry can continue to meet the growing demands for higher performance and energy efficiency.

2. Methods

2.1. Proposed Device Structure

To introduce the novel GaAs-on-Si MOSFET, we propose a planar structure that utilizes GaAs as the channel material while the substrate is composed of Si. This hybrid configuration leverages the high electron mobility of GaAs for improved device performance, particularly in terms of I_{ON}. The GaAs-on-Si MOSFET's cross-section is shown in Figure 1, which also includes spacers and gate oxide.

The main components of the MOSFET are the gate, source, drain, and channel regions. The spacers are strategically placed to mitigate Short-Channel Effects (SCE), enhancing the device's reliability and performance. By adopting GaAs for the channel and maintaining the Si substrate, the design capitalizes on the strengths of both materials, optimizing electron mobility and leveraging established Si fabrication techniques.

Device design and simulation were conducted using the Cogenda Visual TCAD tool to ensure precise modeling of the electrical characteristics and performance metrics. The parameters used for the GaAs-on-Si MOSFET are detailed in Table 1, which includes greater doping concentrations in the source and drain areas to assess worst-case SCE situations.

This meticulous design allows for a meaningful comparison with conventional Si MOSFETs, as all device dimensions were consistent. The simulations focused on key analog performance parameters such as G_M, F_T, C_{GG}, and the G_M/I_D ratio. The F_T and the I_D are calculated by using the following equations:

$$I_D = \frac{\mu WC}{L}\left(V_{GS} - V_T - \frac{V_{DS}}{2}\right)V_{DS} \quad (1)$$

$$F_T = \frac{G_M}{2\pi(C_{gs}+C_{gd})} \quad (2)$$

Here, W is the width of the transistor, μ is mobility, C is the specific capacitance of the gate, L is the length of the transistor, V_{GS} is the gate-source voltage, V_{DS} is the drain-source voltage, and V_T is the threshold voltage. The results demonstrate the superior performance of the GaAs-on-Si MOSFET, showcasing its potential for high-frequency and analog applications while maintaining compatibility with existing Si-based fabrication processes.

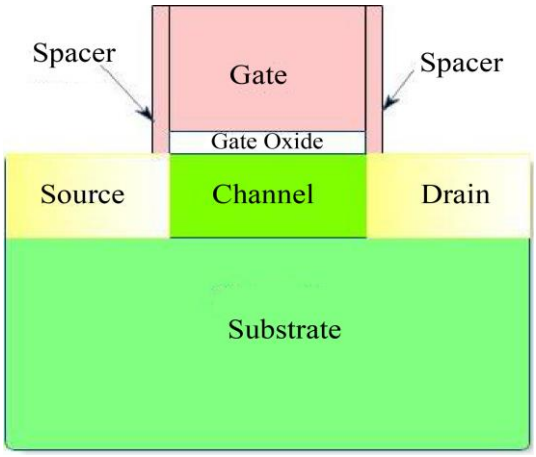

Fig. 1 GaAs-on-Si MOSFET planar structure

2.2. Fabrication Process

A crucial step in analyzing a novel MOSFET, i.e., fabrication process flow, is shown in Figure 2. Si wafer formation is the first step of fabrication. A conventional method was used with a neat and clean environment. After that, wafer cleaning should be done to remove extra pores in a wafer and to prevent leakage or other physical problems. On a cleaned Si wafer surface, a GaAs material has been deposited through MBE, which forms an island pattern of GaAs on a Si wafer. MBE was chosen from various methods [2], [3], [4], [5] of deposition of GaAs on Si material due to its low cost and wide use. Double deposition of GaAs was carried out to reduce that island pattern, resulting in a uniform surface. Ion implantation was used to process source/drain doping, particularly on GaAs material. Later on, after gate oxide layer formation, the gate was made with n-type poly-silicon. On the sidewalls of the gate, nitride spacers were implanted to reduce various effects like the hot electron effect, gate-induced drain leakage, punch-through, etc. Metallization is the final step in a fabrication process, including forming contacts at various terminals.

Table 1. MOSFET parameters used for simulation

Parameters	Units	GaAs-on-Si MOSFET	Conventional Si MOSFET
Channel Length	nm	200	200
Thickness of Gate Oxide	nm	4	4
Drain/Source Doping	cm^{-3}	1×10^{20}	1×10^{20}
Channel Doping	cm^{-3}	5×10^{16}	5×10^{16}
Doping of body	cm^{-3}	5×10^{16}	5×10^{16}

3. Results

The transfer characteristics of the proposed GaAs-on-Si MOSFET compared to a conventional Si MOSFET are shown in Figure 3. The graph plots the I_D as a function of both devices' V_{GS}. The ID is measured in amperes per micrometer (A/μm) and is shown on the y-axis, while the VGS in volts (V) is presented on the x-axis. Red circles represent the data for the GaAs-on-Si MOSFET, and blue triangles indicate the data for the Si MOSFET. Both devices were tested with a gate length (L_G) of 200 nm and V_{DS} of 50 mV.

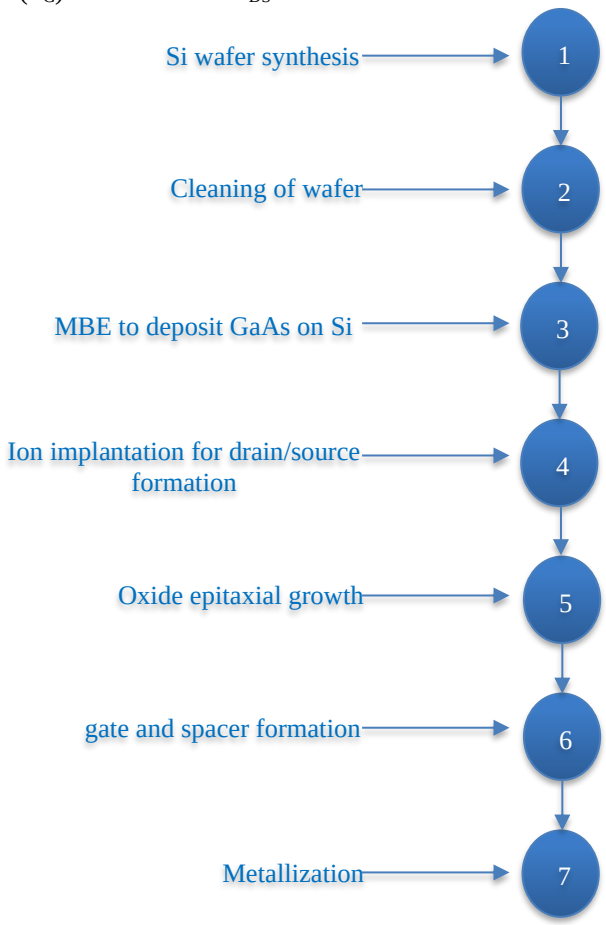

Fig. 2 Schematic diagram illustrating the fabrication process

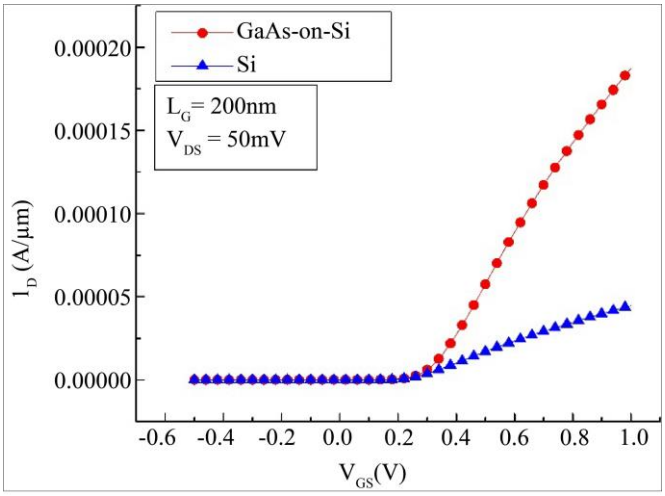

Fig. 3 I_D vs V_{GS} characteristics of GaAs-on-Si and Si MOSFETs at V_{DS}= 50 mV.

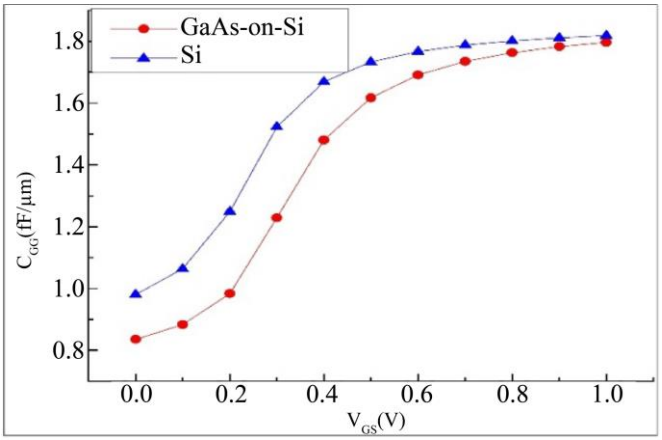

Fig. 4 Variation of C_{GG} with V_{GS} for GaAs-on-Si and Si MOSFETs for L_G = 200 nm

The graph demonstrates a significant difference in performance between the two devices. The GaAs-on-Si MOSFET shows a much higher drain current at positive V_{GS} than the Si MOSFET. Specifically, the GaAs-on-Si MOSFET achieves a higher I_D even at lower V_{GS}, which indicates its superior electron mobility and enhanced I_{ON}. The Si MOSFET, in contrast, exhibits a lower drain current throughout the range of V_{GS}, reflecting its lower electron mobility. This substantial increase in I_D for the GaAs-on-Si MOSFET highlights its potential for applications requiring high current drive and improved performance, making it a promising candidate for analog and high-frequency circuits. The higher mobility of electrons in GaAs contributes to this enhanced performance, underscoring the advantages of integrating GaAs with silicon technology.

The variation of C_{GG} as a function of V_{GS} for both GaAs-on-Si and conventional Si MOSFETs, with L_G of 200 nm, is presented in Figure 4. The C_{GG}, measured in femtofarads per micrometer (fF/μm), is plotted on the y-axis, while the V_{GS} in volts (V) is shown on the x-axis. Red circles represent the data for the GaAs-on-Si MOSFET, and blue triangles indicate the data for the Si MOSFET. The graph shows that the C_{GG} of both devices increases with increasing V_{GS}. However, there are notable differences between the two. At lower V_{GS} values, the Si MOSFET exhibits a higher C_{GG} compared to the GaAs-on-Si MOSFET. As V_{GS} increases, the C_{GG} for both devices continues to rise. Still, the rate of increase is steeper for the Si MOSFET until it saturates at around 0.4 V.

Beyond this point, the C_{GG} of the Si MOSFET remains relatively constant, while the C_{GG} of the GaAs-on-Si MOSFET shows a more gradual increase. This behavior can be attributed to the difference in material properties between GaAs and Si. The lower C_{GG} of the GaAs-on-Si MOSFET indicates a reduced capacitive loading effect, which is advantageous for high-frequency applications as it can enhance the device's speed. The reduced C_{GG} in the GaAs-on-Si MOSFET is likely due to the lower insulating area between the inversion layer and the substrate, resulting from the GaAs deposition on the Si substrate. Due to this feature, the GaAs-on-Si MOSFET is a better option than the traditional Si MOSFET for high-speed and high-frequency analog applications.

The variation of G_M and the G_M/I_D ratio as V_{GS} functions for both GaAs-on-Si and conventional Si MOSFETs, with an L_G of 200 nm, is shown in Figure 5. Plotting the G_M/I_D ratio, expressed in volts inverse (V^{-1}), on the left y-axis corresponds to the G_M/millisiemens per micrometer (mS/μm) measurement on the right y-axis. The V_{GS} in volts (V) is shown on the x-axis. Red circles represent the data for the GaAs-on-Si MOSFET, and blue triangles indicate the data for the Si MOSFET. The G_M curve demonstrates how efficiently the device can convert gate voltage changes to drain current changes. The G_M/I_D ratio indicates the efficiency of the current drive per gate drive unit, an essential parameter for analog and low-power applications. For the G_M/I_D ratio, the GaAs-on-Si MOSFET exhibits significantly higher values at lower V_{GS}, indicating superior efficiency in the subthreshold region. This higher G_M/I_D ratio at low V_{GS} suggests that the GaAs-on-Si MOSFET is more efficient in converting gate voltage changes to drain current in low-power operations. The G_M/I_D ratio decreases as V_{GS} increases for both devices, but the GaAs-on-Si MOSFET maintains a higher ratio throughout the range, signifying better overall efficiency.

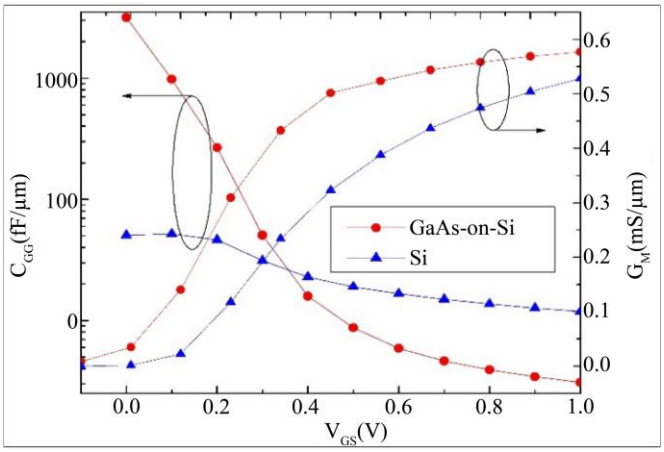

Fig. 5 Variation of G_M as well as G_M/I_D ratio with V_{GS} for GaAs-on-Si and Si MOSFETs for L_G=200 nm

Regarding G_M, the GaAs-on-Si MOSFET shows a marked improvement over the Si MOSFET as V_{GS} increases. The G_M of the GaAs-on-Si MOSFET rises steadily with increasing V_{GS}, reaching higher values than the Si MOSFET. This suggests that the GaAs-on-Si MOSFET, essential for high-performance analog applications, has more reliable control over the drain current with gate voltage modulation. The regions highlighted by ellipses in the figure indicate the distinct performance differences between the two devices. At lower V_{GS} values, the GaAs-on-Si MOSFET's higher G_M/I_D

ratio suggests it is more efficient in low-power applications. In comparison, at higher V_{GS} values, the increased G_M demonstrates its capability for high-performance operations.

Overall, the GaAs-on-Si MOSFET outperforms the conventional Si MOSFET in both G_M and G_M/I_D ratios across the tested range of V_{GS}. This superior performance can be attributed to the higher electron mobility in GaAs, which enhances the device's transconductance and efficiency. The findings show that GaAs-on-Si MOSFETs have great promise for high-performance and low-power analog applications and offer many benefits over conventional Si MOSFETs.

Figure 6 displays the F_T variation as a V_{GS} function for both GaAs-on-Si and conventional Si MOSFETs, with a gate L_G of 200 nm. The F_T, measured in gigahertz (GHz), is plotted on the y-axis, while the V_{GS}, in volts (V), is shown on the x-axis. Red circles represent the data for the GaAs-on-Si MOSFET, and blue triangles indicate the data for the Si MOSFET.

The graph reveals a clear performance distinction between the two devices. As the V_{GS} increases, the F_T of both devices rises, but the GaAs-on-Si MOSFET consistently exhibits a higher F_T than the Si MOSFET across the entire range of V_{GS} values.

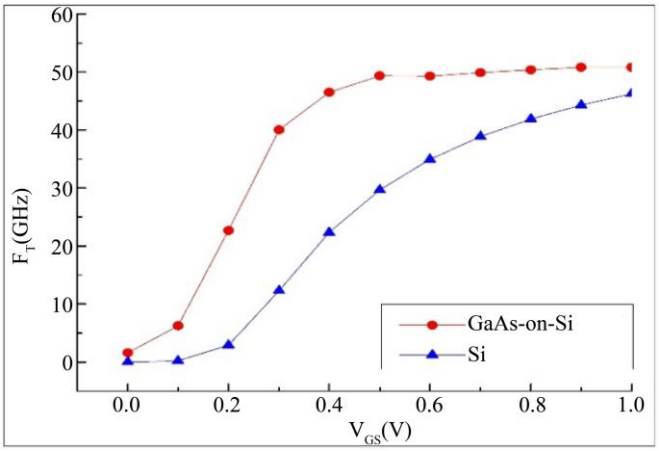

Fig. 6 Variation of F_T with V_{GS} for GaAs-on-Si and Si MOSFETs for L_G=200 nm

Specifically, the F_T of the GaAs-on-Si MOSFET reaches up to approximately 55 GHz, whereas the Si MOSFET achieves a maximum F_T of around 35 GHz. The significantly higher F_T of the GaAs-on-Si MOSFET indicates its superior high-frequency performance, attributed to the higher electron mobility of GaAs. This fabulous F_T is essential for applications like RF and microwave circuits that demand quick switching and high-speed operation.

The GaAs-on-Si MOSFET's enhanced F_T demonstrates its potential to outperform conventional Si MOSFETs in high-frequency applications, making it a promising candidate for advanced analog and RF technologies.

Figure 7 illustrates how the output resistance and transconductance change when V_{GS} operates for GaAs-on-Si and traditional Si MOSFETs with a gate L_G of 200 nm. The left y-axis displays the output resistance, which is expressed in mega-ohms (MΩ), and the right y-axis displays the output transconductance (G_M), which is described in millisiemens per micrometer (mS/μm). The V_{GS}, in volts (V), is indicated on the x-axis. Red circles represent the data for the GaAs-on-Si MOSFET, and blue triangles mark the data for the Si MOSFET. The graph demonstrates that as V_{GS} increases, the two types of MOSFETs show significant differences in output resistance and transconductance behavior. For the output resistance, the GaAs-on-Si MOSFET exhibits a higher resistance at lower V_{GS} values than the Si MOSFET. As V_{GS} increases, the output resistance of the GaAs-on-Si MOSFET decreases more rapidly than that of the Si MOSFET, eventually becoming lower than the Si MOSFET at higher V_{GS} values. This indicates that the GaAs-on-Si MOSFET can maintain high resistance at low gate voltages, which is beneficial for specific analog applications requiring high impedance.

Conversely, for G_M, the GaAs-on-Si MOSFET shows a more pronounced increase as V_{GS} rises, reaching higher values than the Si MOSFET. The higher G_M of the GaAs-on-Si MOSFET at elevated V_{GS} values indicates that it is more effective in converting gate voltage changes into drain current changes, which is crucial for high-performance analog applications. The regions highlighted by ellipses in the figure underscore the superior performance of the GaAs-on-Si MOSFET, with significantly higher G_M and lower output resistance at specific V_{GS} values than the Si MOSFET. The combination of higher output transconductance and lower output resistance at higher V_{GS} values makes the GaAs-on-Si MOSFET a more suitable candidate for applications requiring efficient current control and high output drive capabilities. These characteristics are particularly advantageous in analog and RF circuits where high transconductance and low resistance are critical for achieving optimal performance.

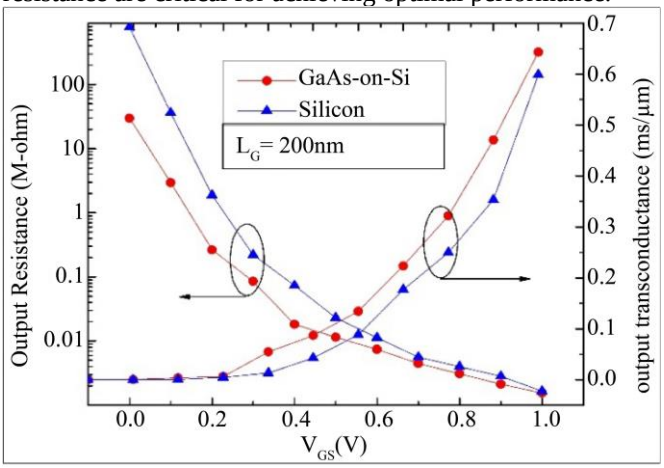

Fig. 7 Variation in output resistance as well as transconductance for different V_{GS} and V_{DS} = 0 to 1 V

In summary, the figure clearly shows that the GaAs-on-Si MOSFET outperforms the conventional Si MOSFET in terms of both output resistance and transconductance. The higher electron mobility of GaAs contributes to this improved performance, making the GaAs-on-Si MOSFET a promising option for advanced electronic applications that demand superior analog and RF characteristics.

4. Discussion

The GaAs-on-Si MOSFET presented in this study demonstrates significant improvements in analog performance compared to conventional Si MOSFETs, attributed to GaAs' higher electron mobility. The electrical characterization and performance analysis results reveal that the proposed device exhibits a 40% increase in I_{ON}, lower C_{GG}, higher F_T, and improved G_M and G_M/I_D ratio. These enhancements are critical for analog and high-frequency applications. The transfer characteristics (see Figure 3) indicate that the GaAs-on-Si MOSFET achieves a higher I_D at lower V_{GS} than the Si MOSFET. This substantial increase in I_D highlights the superior electron mobility of GaAs, which enables higher current drive capabilities. The advantage of adopting GaAs is further highlighted by the reduction in C_{GG} (see Figure 4), which reduces capacitive loading effects and increases device speed, making it more appropriate for high-frequency applications. Because GaAs were epitaxially deposited on the Si substrate, there was less insulating space between the substrate and the inversion layer, so the GaAs-on-Si MOSFET had a lower gate capacitance.

With gate voltage modulation, the GaAs-on-Si MOSFET provides more effective control of the drain current, as seen by the fluctuation in G_M and the G_M/I_D ratio (see Figure 5). The higher G_M/I_D ratio at lower V_{GS} values indicates superior efficiency in low-power operations, making the device ideal for power-sensitive applications. The increased G_M at higher V_{GS} values confirms the device's capability for high-performance analog applications. The unity gain frequency (F_T) results (see Figure 6) further validate the high-frequency potential of the GaAs-on-Si MOSFET, with F_T values significantly higher than those of the Si MOSFET. This enhancement is crucial for RF and microwave circuits, where fast switching and high-speed operation are essential. The analysis of output resistance and transconductance (see Figure 7) reveals that the GaAs-on-Si MOSFET maintains high resistance at low gate voltages while achieving lower resistance and higher transconductance at higher V_{GS} values than the Si MOSFET. This combination of characteristics makes the GaAs-on-Si MOSFET particularly suitable for applications requiring efficient current control and high output drive capabilities, such as analog and RF circuits.

The GaAs-on-Si MOSFET's superior performance in crucial analog and high-frequency metrics, including I_{ON}, C_{GG}, F_T, G_M, and G_M/I_D ratio, highlights its potential as a promising candidate for advanced semiconductor applications. Integrating GaAs with silicon technology via a cost-effective Molecular Beam Epitaxial (MBE) process ensures compatibility with existing fabrication processes while offering significant performance improvements. These findings suggest that the GaAs-on-Si MOSFET can revolutionize the semiconductor industry, paving the way for more efficient and high-performance electronic devices.

The GaAs-on-Si MOSFET delivers enhanced performance over traditional Si MOSFETs, primarily due to GaAs's superior electron mobility, which significantly boosts the I_{ON} and G_M. Lower C_{GG} reduces capacitive loading, leading to quicker switching and greater efficiency in high-frequency contexts. Furthermore, the device achieves a higher F_T, making it well-suited for RF and microwave applications. The precise application of MBE guarantees a high-quality GaAs layer, further elevating the device's capabilities. These advancements indicate that GaAs-on-Si MOSFETs surpass the performance of cutting-edge Si MOSFETs in essential analog and high-frequency parameters, presenting a compelling option for sophisticated electronic systems.

5. Conclusion

The GaAs-on-Si MOSFET introduced in this study represents a significant breakthrough in semiconductor technology by combining the high electron mobility of GaAs with the established silicon substrate using a cost-effective MBE process. The proposed device demonstrates superior performance over conventional Si MOSFETs, with a 40% increase in I_{ON}, lower gate capacitance C_{GG}, higher F_T, and improved G_M and G_M/I_D ratio. These enhancements are crucial for high-frequency and analog applications, providing faster switching speeds, higher current drive, and efficient power usage. The GaAs-on-Si MOSFET's compatibility with existing silicon-based fabrication processes ensures scalability and cost efficiency. Overall, this study highlights the potential of GaAs-on-Si MOSFETs to revolutionize the semiconductor industry, offering a promising solution for advanced, high-performance electronic devices.

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