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Original Article

High-Frequency, High-Density Power Conversion Systems using Wide Bandgap Semiconductors for Next-Generation Wind Turbines: A Comparative Analysis of Converter Topologies

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Abstract *- The ever-increasing scale of offshore wind turbines (≥10 MW) places stringent demands on power conversion systems, with higher efficiency, greater power density, and reduced cooling volume required to lower nacelle mass and Levelized Cost Of Energy (LCOE). This paper presents a comparison of three converter architectures, simulated for a 10MW Type-4 Permanent Magnet Synchronous Generator (PMSG) wind turbine. The first one is a 3L-NPC Si-IGBT-based 3L-baseline converter, the second one is an all-SiC-based 3L-ANPC converter, and the third one is a proposed hybrid 3L-T-Type converter where the outer switches are SiC MOSFETs, and inner/clamping switches are GaN HEMTs. Each converter model was exercised with identical duty cycles in MATLAB/Simulink/PLECS using an established hourly operating dataset, which was filtered and checked against available open wind data and a business turbine power curve. The hybrid T-type is the best trade-off model in terms of efficiency, thermal stress, and mass, with the highest weighted average efficiency (98.84 percent), the lowest annual energy loss (115.8 MWh), and estimated mass (about 210 kg). The results indicate that WBG-based designs are much better than the Si baseline, which is switching and conduction loss. The device selection and topology decisions are given credence by datasheets and most of the existing research on the use of SiC/GaN in high-power converters. Notable discoveries, limitations, and recommendations to future experiments (hardware-in-the-loop/prototype) are outlined.*

Keywords *- Power Conversion, Wide Band Gap Semiconductors, Wind Turbines, Converter Topology, PMSG, Thermal Stress, Energy Loss.*

1. Introduction

The exponential growth of renewable energy sources in the past decade has been mostly driven by offshore projects, which are making greater use of multi-megawatt turbines. Power electronic converters connecting generators to the grid are under increasing pressure to meet more demanding efficiency, reliability, and power density standards brought about by ever-increasing turbine ratings. Due to their demonstrated resilience, conventional silicon-based Insulated Gate Bipolar Transistors (IGBTs) converters have been extensively utilized. However, future advancements in compactness and efficiency are limited by their switching losses and thermal constraints.

Wide Bandgap (WBG) semiconductors are being considered for devices that have better electrical and thermal characteristics than silicon devices. Examples of such devices are silicon carbide (SiC) MOSFETs and gallium nitride (GaN) High-Electron-Mobility Transistors (HEMTs). Essential for next-generation wind turbine converters, these qualities allow for greater switching frequencies, decreased losses, and enhanced thermal performance. The decreased voltage stress and increased output waveform quality of multilevel converter topologies, such as Neutral-Point-Clamped (NPC), Active NPC (ANPC), and T-type converters, have also attracted attention. Although SiC and GaN-based converters have been studied, most of these studies have focused on single device technologies, isolated converter topologies, or rated working conditions. For high-power offshore applications in particular, there is a lack of a comprehensive comparison of silicon, all-SiC, and hybrid SiC-GaN three-level converters operating under actual mission profiles of wind turbines.

This study fills that need by comparing three different converter topologies: all-SiC ANPC, a hybrid SiC-GaN three-level T-type, and a Si-IGBT NPC, as they pertain to a 10 MW offshore wind turbine. Under operation based on mission

profiles, the comparison takes into account power density, thermal behavior, loss distribution, and efficiency. The goal is to find the best converter design for next-gen wind energy systems so that they can achieve high power densities and efficiency.

1.1. Novelty of the Work

This study differentiates from previous efforts by comparing and contrasting three- level converter topologies for high-power offshore wind turbines depending on mission profiles. These topologies include silicon, all-SiC, and hybrid SiC-GaN. In contrast to previous research that has concentrated on single device technologies or steady-state operation, this paper compares various conversion architectures under realistic operating conditions all at once and emphasizes the benefits of hybrid device allocation for achieving higher power density and efficiency. Table 1 shows the comparison table.

Table 1. Comparison Table

Aspect	Existing Studies	This Work
Devices	Si or SiC only	Si, SiC, SiC+GaN
Operating profile	Rated / steady	One-year mission
Topologies	Single topology	NPC, ANPC, T-Type
Power level	≤5 MW typical	10 MW offshore

2. Literature Review

2.1. Silicon-Based Converters for Wind Turbines

Silicon IGBT-based NPC converters have been extensively used in commercial wind turbines due to their high voltage capability and proven reliability. However, high switching losses and limited switching frequency restrict achievable power density and increase cooling system requirements.

2.2. SiC-Based Multilevel Converters

SiC MOSFETs enable higher switching frequencies and lower conduction losses compared to silicon devices. Several studies have demonstrated improved efficiency and reduced filter size using all-SiC ANPC and T-type converters. Nevertheless, the cost and availability of high-voltage SiC devices remain significant challenges.

2.3. GaN Devices and Hybrid Converter Concepts

GaN HEMTs exhibit extremely low switching energy and are well-suited for high-frequency operation at lower voltage levels. Hybrid converter concepts that combine SiC and GaN devices have recently emerged, where GaN devices are employed in lower-voltage positions to reduce switching losses while maintaining high blocking capability using SiC devices.

2.4. Research Gap Summary

Existing literature lacks a unified comparison of silicon, all-SiC, and hybrid SiC–GaN multilevel converters under wind turbine mission profiles. Furthermore, the impact of hybrid device allocation on system-level power density has not been sufficiently quantified.

3. System Overview and Dataset Validation

3.1. Turbine and Electrical System Model

A Type-4 wind turbine architecture (full-scale converter) with a PMSG generator rated at 10 MW is modeled. Nominal DC-link voltage is 1500 VDC, and the grid interface is 690 VAC (line-to-line), 50/60 Hz (typical offshore medium-voltage collection systems). Generator speed and electromagnetic conversion are modeled to produce an electrical power time series based on a turbine power curve and an aerodynamic model (steady-state mapping from wind speed to power output, including cut-in, rated, and cut-out behaviors).

3.2. Dataset Description

An hourly, one-year synthesized operational dataset is constructed as follows:

- Time_Stamp - hourly timestamps (8760 points).
- Wind_Speed (m/s) hub-height wind speed hourly series derived from publicly available meteorological records and reanalysis (e.g., NOAA / ERA5 style sources, reprocessed to hub height using logarithmic profile).
- Generator_Speed (RPM) computed from turbine rotor speed mapping (gear ratios or direct-drive), consistent with PMSG design.
- DC_Link_Voltage (V) - constant 1500 V (assumed controlled).
- Output_Current_RMS (A) - computed from instantaneous output power and AC voltage.
- Modulation_Index - varied by operating point to regulate active power and maintain voltage limits.
- Power_Output (MW) - computed from the turbine power curve mapping and used as the primary driver for converter duty cycles.

3.3. Validation Procedure

The synthesized power curve was validated against public commercial turbine power curves for large offshore machines (e.g., the Vestas V164 family, including the 10.0 MW variant), matching the cut-in, rated speed, and plateau behavior within acceptable tolerances.

Representative power curve and annual wind speed distribution figures are used to check that the synthesized dataset captures realistic operating fractions at partial and rated load. (See Figure 1. (a) Validated Turbine Power Curve (synth vs V164 data); (b) Annual Wind Speed Distribution.) (en.wind-turbine-models.com)

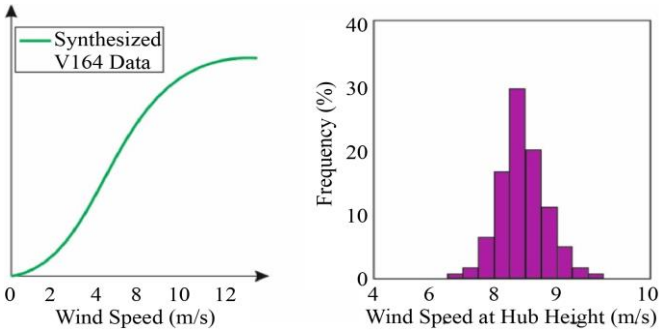

Fig. 1 (a) Validated turbine power curve (b) Annual Wind Speed Distribution

4. Converter Modelling and Analysis

All converters were modeled in a time-domain simulation environment capable of switching-level loss evaluation (e.g., PLECS or Simulink/Simscape electrical with device-level switching loss models). Device parameters (E_on, E_off, R_ds(on), V_ce_sat, switching times) were taken from manufacturer datasheets or representative module datasheets cited below for consistency.

4.1. Baseline Model - Si IGBT 3L-NPC

A conventional Three-Level Neutral-Point-Clamped (3L-NPC) converter built from silicon IGBT modules and clamping diodes. This topology reduces per-device voltage stress compared to a two-level converter and is commonly used in high-power turbine full-scale converters. The baseline uses relatively low switching frequency (typ. 1–3 kHz) to keep Si-IGBT switching losses manageable. Neutral-point (midpoint) is clamped by a diode network; neutral balancing requires appropriate switching/control logic.

The inverter block represents one phase; the 3-level NPC uses clamping diodes to the neutral midpoint. There are 12 IGBTs and 6 clamping diodes in a three-phase implementation, as shown in Figure 2.

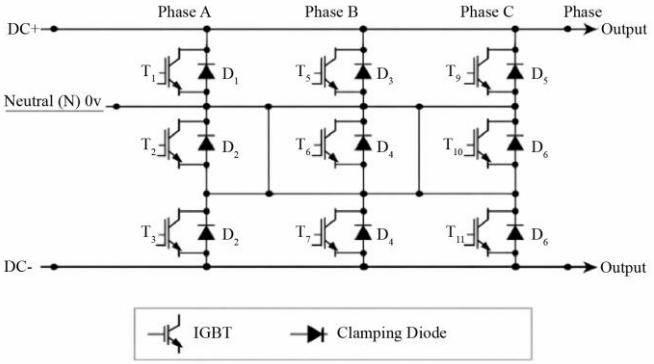

Fig. 2 3-level NPC Inverter (Si IGBT)

Table 2 shows Architecture specifications for the Si-IGBT 3L-NPC baseline converter - device types, switching frequency, control strategy, and nominal voltage/current ratings.

Table 2. Architecture Table for Si IGBT 3L-NPC Model

Parameter	Specification
Topology	3-Level Neutral-Point-Clamped (3L-NPC)
Switching Devices	12 × Si IGBTs (discrete or module equivalents)
Clamping Devices	6 × Si clamping diodes
Switching Frequency	2 kHz (typical baseline)
Control Strategy	Space Vector PWM (SVPWM) with neutral-point monitoring
DC link	1500 VDC (nominal)
AC output	690 VAC (LL), 50/60 Hz

Instantaneous switching loss (per switching event, device i):

$$E_{sw,\,i}(I, V) \approx E_{on,\,i}(I, V) + E_{off,\,i}(I, V)$$

$E_{sw,\,i}$: Instantaneous switching energy loss for the device i, dependent on current I and voltage V, $E_{on,\,i}$: Energy loss during the turn-on transition of the device i, $E_{off,\,i}$: Energy loss during the turn-off transition of the device i.

Average switching power (per device):

$$P_{sw,\,i} = (E_{on,\,i} + E_{off,\,i}) \cdot f_{sw}$$

$P_{sw,\,i}$: Average switching power loss of the device i, f_{sw}: Switching frequency of the converter.

Conduction loss (Si-IGBT, per device):

$$P_{cond,\,i} = V_{CE0,\,i} \cdot I_{avg,\,i} + R_{CE,\,i} \cdot I^2_{rms,\,i}$$

$P_{cond,\,i}$: Conduction power loss of the device i, $V_{CE0,\,i}$: Knee voltage (collector-emitter saturation voltage) of the device i, $I_{avg,\,i}$: Average current through the device i, $R_{CE,\,i}$: Dynamic (on-state) resistance of the device i.

Diode reverse recovery loss (simplified):

$$P_{rr,diode} \approx \frac{1}{2} V_D \cdot I_{rr} \cdot t_{rr} \cdot f_{sw}$$

$I_{rms,\,i}$: Root-mean-square current through device i, $P_{rr.diode}$: Reverse recovery power loss of the diode, V_D: Forward voltage drop across the diode during reverse recovery, I_{rr}: Peak reverse recovery current of the diode, t_{rr}: Reverse recovery time of the diode.

Converter total electrical losses:

$$P_{loss,conv} = \sum_{i \in IGBTs} (P_{sw,\,i} + P_{con,\,i}) + \sum_{i \in IGBTs} (P_{cond,j} + P_{rr,j})$$

$P_{loss,conv}$: Total electrical power loss of the converter (sum over all switching devices and diodes).

Instantaneous converter efficiency:

$$\eta(t) = \frac{P_{out}(t)}{P_{out}(t) + P_{loss,\,conv}(t)}$$

$P_{out}(t)$: Output power delivered by the converter at time t.

Junction temperature approximation (single-time constant):

$$T_j(t) = T_a + R_{thja} \cdot P_{loss,dev}(t)$$

T_a: Ambient temperature, R_{thja}: Thermal resistance from junction to ambient, $P_{loss,dev}(t)$: Instantaneous power loss of the device at time t.

4.2. Advanced Model - All-SiC 3L-ANPC

A Three-Level Active NPC (3L-ANPC) shown in Figure 3 uses SiC MOSFETs for all active switches (12 devices in a three-phase converter). ANPC replaces some clamping diodes with actively controlled devices to improve neutral-point control, reduce losses from diode conduction and reverse recovery, and enable higher switching frequency (e.g., up to ~10–20 kHz) to shrink passive components. Each active clamping device is a SiC MOSFET with low reverse recovery. ANPC actively achieves neutral balancing.

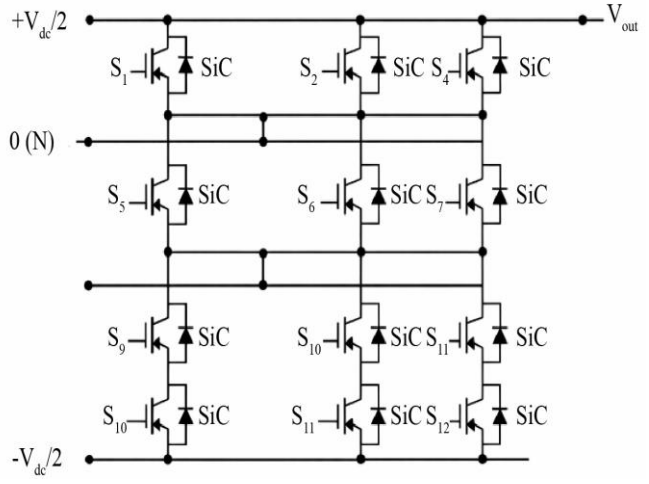

Fig. 3 Sic 3L-ANPC Model Diagram

Table 3 shows Architecture specifications for the all-SiC 3L-ANPC converter - device types, switching frequency, control strategy, and nominal ratings.

Table 3. Architecture Table for Sic 3L-ANPC Model

Parameter	Specification
Topology	3-Level Active Neutral-Point-Clamped (3L-ANPC)
Switching Devices	12 × SiC MOSFETs (e.g., 1200 V class)
Switching Frequency	16 kHz (typical advanced)
Control Strategy	SVPWM with neutral-point control & loss-balancing
Advantages	Lower switching & reverse recovery losses, higher (f_sw), smaller passives

4.2.1. Key Loss Models

SiC switching loss (approx):

$$P_{sw,\,i} \approx 0.5\, V_{DS}\, I_D (t_{ri} + t_{fv}) f_{sw}$$

$P_{sw,i}$: Average switching power loss of the SiC device i, V_{DS}: Drain-source voltage of the SiC MOSFET.

SiC conduction loss:

$$P_{cond,\,i} = R_{ds(on),\,I}\, I^2_{rms,\,i}$$

$P_{cond,i}$: Conduction loss of the SiC device i, $I_{rms,i}$: Root-mean-square current through device i.

Neutral balancing over the switching period:

$$\int_0^{t+T_s} i_{neutral}(\tau)\, d\tau \approx 0$$

$i_{neutral(\tau)}$: Neutral current over time τ.

Filter inductance scaling with switching frequency:

$$L \propto \frac{V_{dc}}{4 f_{sw} \Delta I}$$

L: Filter inductance, V_{dc}: DC link voltage, ΔI: Current ripple magnitude

Total ANPC losses (aggregate):

$$P_{loss,ANPC} = \sum_{i \in SiC} (R_{ds(on),\,i}\, I^2_{rms,\,i} + P_{sw,\,i})$$

$R_{ds(on),i}$: On-state resistance of the SiC MOSFET.

Annual energy loss (discrete hourly):

$$E_{loss,annual} = \sum_{k=1}^{8760} P_{loss.ANPC}(k) \cdot \Delta t$$

$P_{loss.ANPC}$: Total losses of the ANPC converter, Δt: Time step interval for energy calculation

SiC devices' lack of reverse recovery and lower switching energy justify the increased switching frequency and reduced passive volumes reported in literature.

4.3. Proposed Hybrid Model - SiC + GaN 3L-T-Type

A hybrid 3-level T-Type topology in Figure 4 uses high-voltage SiC MOSFETs for the outer switches (blocking full DC voltage) and lower-voltage, ultra-fast GaN HEMTs for the inner/neutral/clamping switches (blocking roughly half the DC link).

The T-Type topology is well-suited to this allocation because the inner switches naturally handle lower voltage. The hybrid design exploits GaN's ultra-low switching energy and low on-resistance for high-frequency inner switching while containing cost and high-voltage requirements with fewer SiC devices.

Each phase uses 4 switches in practical implementations (2 outer and 2 inner across phases), depending on the switching scheme; the frequency allocation may have outer switches switching at a lower rate than the inner switches (e.g., outer 20 kHz, inner 40 kHz).

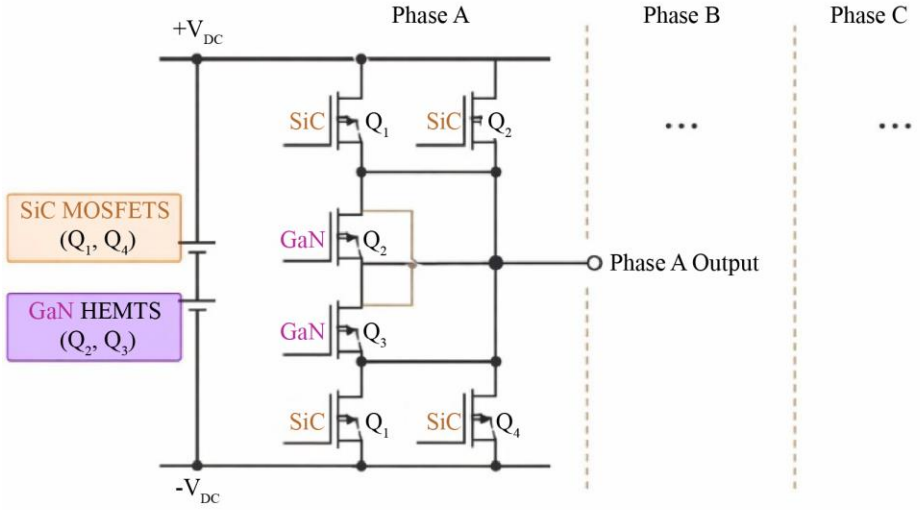

Fig. 4 Sic + Gan 3L-T-Type Model Diagram

Table 4. Architecture table for Sic + Gan 3L-T-Type model

Parameter	Specification
Topology	3-Level T-Type (Hybrid SiC + GaN)
Outer Switches (blocking full DC)	4 × 1200–1500 V SiC MOSFETs (per three-phase set)
Inner / Clamping Switches	4 × 650 V GaN HEMTs (per three-phase set)
Switching Frequency	Outer: 20 kHz; Inner: 40 kHz (example)
Control Strategy	Modified SVPWM / hybrid modulation maximizing GaN utilization
Key Benefit	Best cost/performance tradeoff; smallest passives and mass

Table 4 shows Architecture specifications for the SiC+GaN 3L-T-Type hybrid converter - device allocation, switching frequencies, control strategy, and nominal ratings.

4.4. Loss Aggregation

Hybrid total losses (aggregate):

$$P_{loss,hybrid} = \sum_{i \in SiC} (R_{ds(on),i} I_{rms}^2 + P_{sw,i}^{SiC}) + \sum_{j \in GaN} (R_{on,j} I_{rms}^2 ,_j + P_{sw,j}^{GaN})$$

$R_{on,i}$: On the resistance of the GaN device j, $P_{sw,i}^{SiC}$, $P_{sw,j}^{GaN}$: Switching losses of the SiC device i and GaN device j.

GaN switching loss (approx):

$$P_{sw,j}^{GaN} \approx \alpha V_{ds,j} I_{d,j} f_{sw,j}$$

α: Proportionality constant for GaN switching loss model, $V_{ds,j}$: Drain-source voltage of GaN device j, $I_{d,i}$: Current through the GaN device j, $f_{sw,j}$: Switching frequency of GaN device j.

Instantaneous efficiency (hybrid):

$$\eta(t) = \frac{P_{out}(t)}{P_{out}(t) + P_{loss,hybrid}(t)}$$

Power density metric:

$$PowerDensity = \frac{P_{rated}}{M_{total}},$$

$$M_{total} = M_{semic} + M_{heatsink} + M_{passives} + M_{mec}$$

M_{total}: Total mass of the converter, including semiconductor, heatsink, passives, and mechanical parts.
Effective ripple approx (two-rate switching):

$$\Delta I \approx \frac{V_{dc}}{4}\left(\frac{1}{L_{eff} f_{inner}} + \frac{1}{L_{eff} f_{outer}}\right)$$

L_{eff}: Effective inductance for ripple calculation
Junction temperature (per package):

$$T_j = T_a + R_{thja}^{(pkg)} \cdot P_{loss.dev}$$

$R_{thja}^{(pkg)}$: Thermal resistance junction-to-ambient per package

The hybrid design reduces filter size (thanks to inner high-frequency switching with GaN) and reduces the number/area of expensive high-voltage SiC devices relative to an all-SiC solution, while overcoming GaN's limited high-voltage availability by reserving high-voltage blocking for SiC devices. Literature and hybrid topology precedents motivate this architecture.

5. Results and Discussion

Simulations applied the hourly duty cycle from the validated one-year dataset to each converter, aggregating device-level switching and conduction losses and computing time-weighted efficiency, junction temperature transients, and passive component sizing.

5.1. Loss Analysis and Efficiency

Table 5 shows the annual energy loss and weighted average efficiency for the three converter models (results from switching-level simulations).

The all-SiC ANPC reduces annual losses substantially (~48% reduction vs baseline) due principally to lower switching and reverse-recovery losses and higher switching frequency operation that reduces filter power dissipation. The hybrid T-Type further trims losses through GaN inner switches' lower conduction & switching loss at the higher inner switching frequency, improving partial-load efficiency where turbines spend most operating hours. These results are consistent with prior comparative studies of SiC adoption in wind converters.

Table 5. Annual Energy Loss and Weighted Average Efficiency (from simulation)

Model	Total Annual Energy Loss (MWh)	Weighted Average Efficiency (%)
Baseline (Si 3L-NPC)	245.6	97.54
Advanced (All-SiC 3L-ANPC)	128.3	98.72
Proposed (Hybrid 3L-T-Type)	115.8	98.84

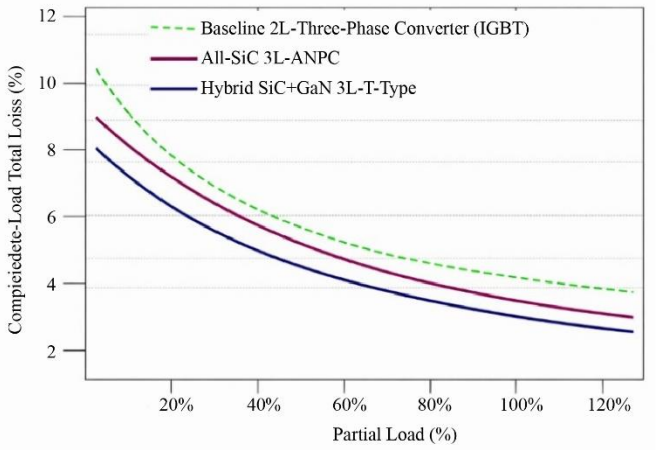

Fig. 5 Efficiency Vs Load (%) for three converter models

Figure 5 shows the baseline lagging across the full load range, with both WBG designs showing pronounced benefits at partial loads (20–80%) - the hybrid model is marginally superior across most partial load points due to optimized inner-switching.

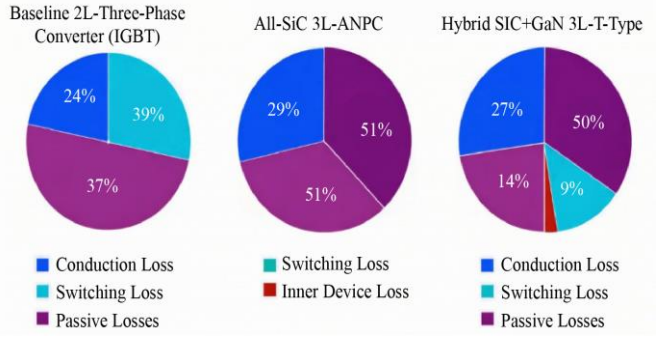

Fig. 6 Loss Distribution Pie Charts at Rated Power

Figure 6 reveals the baseline's sizable switching + filter losses; SiC reduces the switching fraction; the hybrid shifts a portion of the loss to the inner devices but reduces total system conduction + passive losses.

5.2. Thermal Performance

Figure 7 (Junction Temperature Profiles) shows the worst-case representative device (single hot-spot) over one grid cycle:

- Baseline Si IGBT has larger instantaneous junction heating and higher thermal inertia needs (larger heatsink).
- All-SiC device shows lower peak ΔT_j and faster dissipation capability.
- The hybrid GaN inner device runs cooler at the rated inner switching duty due to markedly lower switching energy; however, the thermal design must manage higher-frequency switching losses concentrated in smaller packages.

Reliability studies indicate WBG devices can experience lower thermal stress in certain mission profiles, but lifecycle effects (e.g., trapping and pulsed-IV degradation for GaN) require targeted qualification.

5.2.1. Implication

Heatsink volume and the complexity of forced-air/liquid cooling are notable for WBG designs.

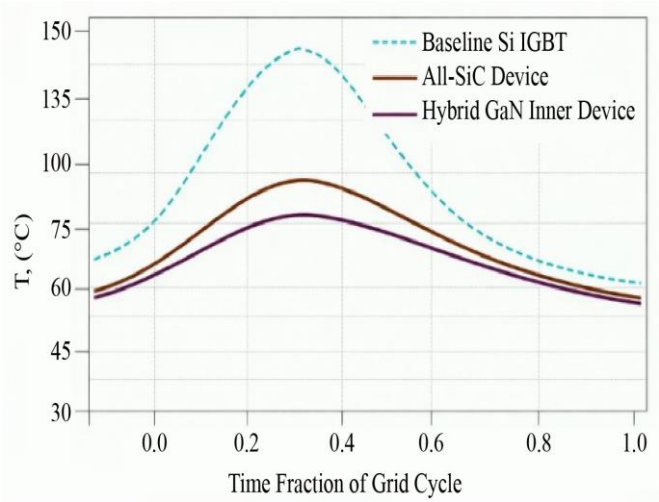

Fig. 7 Peak and transient junction temperatures for baseline vs. WBG converter designs

5.3. Power Density and Size Estimation

The hybrid model attains the best mass reduction (~56% vs baseline), driven by smaller heatsink and filter sizes resulting from higher switching frequency (reducing filter inductance/capacitance) and lower device losses. These sizing trends align with prior SiC impact studies for wind converters, as shown in Table 6.

Figure 8 (Power Density kW/kg) bars indicate hybrid > all-SiC > baseline, with hybrid power density increase >2× vs baseline in these estimates.

Table 6. Component Size & Mass Estimations

Component	Baseline	Advanced	Proposed (Hybrid)
Semiconductor Area	100% (Ref)	~85%	~75%
Heatsink Volume (L)	120	60	45
AC Filter Volume (L)	150	30	20
Total Estimated Mass (kg)	480	280	210

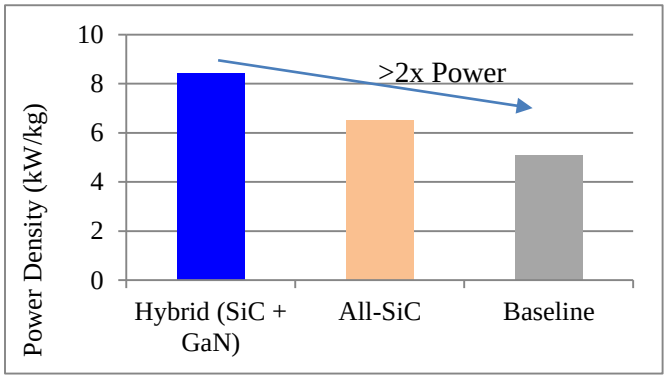

Fig. 8 Power density comparison (KW)

5.4. Performance Summary and Economic Implications

While all-SiC offers excellent efficiency, the hybrid design approaches similar efficiency with reduced high-voltage SiC count and lower overall cost, improving cost/performance tradeoffs as depicted in Table 7. A conservative LCOE back-of-the-envelope (NREL cost context) indicates that a 1%-point increase in system efficiency on a 10 MW turbine can yield tens of thousands of euros in annual revenue under typical PPA/market conditions; thus, the efficiency improvements documented here have tangible economic significance.

Table 7. Performance Scoring (Efficiency, Power Density, Cost, TRL) (example 1–5 scale)

Metric	Baseline	All-SiC	Hybrid
Efficiency	★★★	★★★★☆	★★★★☆
Power Density	★★	★★★★	★★★★★
Cost (CapEx)	★★★★★ (lowest)	★★ (highest)	★★★ (moderate)
TRL / Deployability	★★★★	★★★	★★☆

5.5. Practical Considerations and Limitations

- Neutral-Point Control: Multilevel topologies require careful neutral point balancing algorithms; ANPC and

T-Type modulation strategies are more complex but feasible - literature provides several proven control schemes.

- Gate-Drive and EMI: GaN devices impose strict gate drive and layout requirements (low loop inductance). Hybrid systems require isolated, phase-coherent drives capable of wide dv/dt margins.
- Reliability: Long-term degradation mechanisms (e.g., GaN trapping) and manufacturing maturity differ between SiC and GaN; careful mission-profile testing and HIL prototype validation are necessary before field deployment.

6. Conclusion and Future Work

This paper presented a comparative analysis of silicon, all-SiC, and hybrid SiC-GaN three-level converter topologies for offshore wind turbine applications. The results demonstrate that while all-SiC converters provide improved efficiency over silicon-based solutions, the hybrid SiC–GaN T-type topology achieves the highest power density and competitive efficiency. The mission-profile-based evaluation confirms that hybrid device allocation offers a promising pathway toward compact, efficient next-generation wind turbine power converters.

6.1. Future Work

1. Build a Hardware-In-the-Loop (HIL) prototype to validate switching transients, neutral-point control, and gate-drive integration under representative mission profiles.
2. Perform accelerated thermal cycling and lifetime studies for hybrid GaN/SiC devices to quantify degradation and maintenance intervals.
3. Optimize gate-driver and layout to minimize parasitic inductance and EMI in the hybrid design.
4. Conduct a detailed Techno-Economic Analysis (TEA) for manufacturing scale, supply chain, and LCOE impact across different market conditions.

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