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Original Article

Design of Linear Analog Systems with Dynamics Represented by Atangana-Baleanu Fractional-Order Derivatives

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Abstract *- This work presents the design of analog systems for Fractional-Order (FO) systems governed by the Atangana-Baleanu (AB) fractional derivative. A systematic design methodology is proposed for the development of analog circuits for FO systems based on Foster and Cauer network synthesis techniques, where the dynamics of systems are approximated using the Oustaloup recursive approximation. This approach enables analog realization of FO operators across a specified frequency band. The proposed analog system is designed and implemented using the LTspice simulation environment, which provides circuit-level analysis and includes advanced CMOS modeling. All circuit components are realized using a standard 180-nm CMOS technology process to ensure ease of implementation. The choice of 180-nm CMOS technology offers a balanced trade-off between device performance and design complexity, making it well-suited for analog and mixed-signal circuit realization. Time-domain and frequency-domain validations demonstrate that the designed analog systems faithfully capture the dynamics of the corresponding FO models. The time-domain performance indices of the designed systems, including rise time, settling time, peak overshoot, and the mean square error, are compared to the theoretical FO model responses.*

Keywords *- Fractional Calculus, Linear Systems, Atangana-Baleanu Definition, Analog Systems, CMOS Technology.*

1. Introduction

Fractional Calculus (FC) has attracted considerable interest as an effective solution for modeling complex dynamical systems. arbitrary non-integer real and complex order [2-10]. FC finds a variety of applications in diverse scientific and engineering domains [8-11]. The popularity of Fractional-Order (FO) differintegral operators is due to their unique property of non-locality, unlike the classical Integer-Order (IO) derivatives. A FO derivative is non-local, implying that it relies on all the history of the function from the starting point up to the current point in time. This feature makes FO differential operators suitable for modeling systems with memory and hereditary effects. The design and analysis of linear time-invariant (LTI) systems using FC have been explored in depth by the researchers. Presence of the Mittag-Leffler function (MLF) as eigen function in their response and use of Riemann surface for investigating their stability [12, 13] make FO systems stand apart from the classical IO systems. To characterize FO systems, the majority of linear systems employ the Caputo fractional derivative definition, as this allows the use of physically quantifiable initial conditions in the underlying FO differential equations (FDEs). The difficulty arises from the complexity involved in practical realization of non-integer order operators using conventional hardware components. This is because FO derivative operators possess infinite memory, which makes them difficult to implement on finite memory electronic hardware. A brief review of the real-time implementation of FO operators and systems on different hardware platforms is presented. Although the Atangana–Baleanu (AB) fractional derivative has been widely studied in theoretical and numerical frameworks, its implementation has not yet been reported in the literature.

This paper bridges this gap by presenting a novel hardware realization of the FO AB operator and outlining its integrated-circuit implementation perspective [1]. Literature survey reveals that there have been no attempts at real-time implementations on the systems of AB FDs, such as FPAAs, FPGAs, DSPs, or microcontrollers. The AB operator inherently involves memory-dependent behaviour of the derivative and also the dependence of the output on previous output and input states. This task involves challenges in direct mapping onto conventional digital or analog platforms. The presence of the Mittag–Leffler function introduces additional computational complexity, making real-time implementation

difficult. As a result, no dedicated and generalized architecture for the AB operator has been formally reported.

Operational amplifiers (op-amps) are the backbone of electrical networks. The FO system can be implemented using op-amps and other electrical components. Designing an op-amp using CMOS technology is the primary task of Integrated Circuit (IC) design, implemented in the LTspice software tool across a 180nm technology node. Designing an op-amp involves setting multiple parameters to meet trade-off requirements. The gain of the op-amp with open-loop gain (A_{OL}) configuration is configured to be very high, approximately 40-60 dB; the closed-loop gain (A_{CL}) depends on external feedback resistors and capacitors. Ideally, a maximum rail-to-rail output voltage range is expected to be high in the design. This high level of integration using CMOS technology enables the realization of compact, low-power, and high-performance electronic systems. The FO derivative operators have been implemented using analog circuits with CMOS technology [14-21].

The work presents a novel approach to real-time analog implementation of the systems in 180nm technology. The method demonstrates the realization of AB fractional derivative using CMOS circuits, a stepping stone to the implementation at the integrated circuit level. The design demonstrates Mean Squared Error (MSE) and the time domain performance indices comparison to that of the original system, making it suitable for real-time applications and VLSI integration. The design approach uses the Foster and Cauer network synthesis. The major highlights of this work are listed below:

1. Design of analog circuits for FO Atangana–Baleanu (AB) fractional derivatives.
2. Implementation of analog systems for FO using 180nm technology.
3. Performance analysis of the designed analog systems.

The article sequence is outlined as follows: Section 2 includes the Literature Review; the overall details and definitions of fractional calculus are discussed in Section 3. FO systems considered for analog system design are presented in Section 4. The design and implementation of the aforementioned systems are presented in Section 5. The overall conclusion of the work is stated in Section 6.

2. Literature Review

FO system can be designed using microcontrollers in real-time implementation due to their computational power, memory, and flexibility [22]. Many of the FO systems are developed using the definition of Caputo derivative or Grunwald-Letnikov as discussed in the section on fractional Calculus. The components of microcontrollers used for the implementation of FO systems have several parameters, like conversions from analog to digital and vice versa, sensors for the detection of the input signals, and output sensors. The Field Programmable Gate Array (FPGA) can execute multiple complex operations concurrently. FPGAs operate digitally, so FO operators must be discretized initially. For the discretization, the transfer function in continuous form is transformed to discrete form using the bilinear transformation and z-domain representations. The implementation is followed by simulation in hardware description languages like VHDL or Verilog, and verification, analysis, and implementation are carried out on the FPGA board. Custom analog circuits can be deployed on FPAA, such as filters, amplifiers, oscillators, and other complex analog functions. For the implementation of FO systems, the TF is approximated by Partial Fraction Expansion (PFE). The active filters are implemented with op-amps, resistors, and capacitors [20]. Digital Signal Processing (DSP) hardware platforms are specially designed to implement complex mathematical operations involving signal processing [25, 26]. FO derivatives use many methods for approximating the FO systems to IO, which include Oustaloup Recursive Approximations (ORA) and the same approximations modified to some extent [44]. Very recently, some novel definitions of FD, namely Atangana–Baleanu (AB), and Caputo-Fabrizio (CF) have been introduced. All the prior studies on FO system implementation have mostly relied on definitions, including Caputo, Grünwald–Letnikov, and Riemann–Liouville definitions, for which several hardware and numerical realizations have been implemented. In contrast, the realization of the Atangana–Baleanu fractional operator remains unexplored and has not been reported in the existing literature. Literature survey reveals that these definitions are gaining popularity in the research community due to their ease of computation and analysis.

3. Fractional Calculus

It is an area concerned with mathematical differentiation and the process of integration of non-integer or complex order arbitrary power values. It has been rigorously used by researchers for modeling engineering systems in the real world. The area is well developed by theoretical development of all fractional derivative concepts, leading to a well-established area [2–10]. Fractional derivatives and integrals find widespread applications across various scientific and engineering disciplines. The standard definitions are outlined as follows.

3.1. Grunwald-Letnikov definition $\alpha \in \mathbb{R}^+$

$$aD_t^{\alpha} f(t) = \lim_{h \to 0} h^{-\alpha} \sum_{j=0}^{\left\lfloor \frac{t-a}{h} \right\rfloor} (-1)^j \binom{\alpha}{j} f(t - jh) \qquad (1)$$

In the above equation, the term $\binom{\alpha}{j}$ is the binomial coefficient.

3.2. Riemannâ€ "Liouville definition $\alpha \in \mathbb{R}^+$*:*

The derivative is defined as

$$aD_t^{\alpha} f(t) = \frac{1}{\Gamma(n-\alpha)} \frac{d^n}{dt^n} \int_a^t \frac{f(\tau)}{(t-\tau)^{\alpha-n+1}} d\tau, \qquad (2)$$

For $-1 < \alpha < n$, $n \in \mathbb{Z}^+$, and Γ. is the gamma function.

3.3. Caputo Definition $\alpha \in \mathbb{R}^+$***:***

The derivative is defined as

$$aD_t^{\alpha} f(t) = \frac{1}{\Gamma(n-\alpha)} \int_a^t \frac{f^n(\tau)}{(t-\tau)^{\alpha-n+1}} d\tau, \quad (3)$$

For $-1 < \alpha < n$, $n \in \mathbb{Z}^+$, where $f^n(\tau)$ is the n^{th}order derivative of the function *f(t).*

3.4. Atangana–Baleanu (AB) $\alpha \in \mathbb{R}^+$***:***

$$aD_t^{\alpha} f(t) = \frac{B(\alpha)}{1-\alpha} \int_0^t f'(\tau)\, E_{\alpha}\left(-\frac{\alpha}{1-\alpha}(t-\tau)^{\alpha}\right) d\tau \quad (4)$$

The function $\boldsymbol{f'(\tau)}$ is the first-order derivative of $\boldsymbol{f(t)}$ with respect to time. The kernel of the integral contains the Mittag–Leffler function $E_{\alpha}(\cdot)$, which is non-singular and non-local**.** This kernel provides a more realistic description of memory and hereditary effects by avoiding the singularity present in classical fractional derivatives**.** The term $\boldsymbol{B(\alpha)}$ is a normalization constant that guarantees the correct dimensionality and consistency of the operator.

4. FO Systems for Design

This section lists the FO linear systems for which analog circuits have been designed. To establish the accuracy of the proposed design methodology, a variety of time-domain dynamic behaviours are considered. These dynamics are selected to represent different characteristics commonly observed in linear systems. The linear systems investigated in this work are systematically analysed. The considered systems are enumerated below for clarity and completeness.

4.1. System 1 (G₁(s))

The FDE governs the linear system stated below with fractional operators $\alpha$and β.

$$D_t^{\alpha} y(t) + ay(t) = D_t^{\alpha} u(t) + bu(t) \quad (5)$$

Equation (5) represents a linear fractional-order dynamic system described using the AB fractional derivative**.** The system has an output signal y(t) which not only depends on input u(t) but also past values of the input as well as past values of the output. The system has a constant DC gain. The system represented by equation (5) is stable.

Assume *a=1, b=1* where $a, b \in \mathbb{R}^+$. Taking the Laplace transform of the above AB derivative,

After substituting the value of $\boldsymbol{\beta}$ =0.3, and $\boldsymbol{\alpha}$ =0.5, the equation simplifies as,

$$G_1(s) = \frac{\left(\frac{s^{0.3}}{0.7s^{0.3}+0.3}+1\right)}{\left(\frac{s^{0.5}}{0.5s^{0.5}+0.5}+1\right)}, \quad (6)$$

After simplifying,

$$G_1(s) = \frac{0.85s^{0.8}+0.15s^{0.5}+0.85s^{0.3}+0.15}{1.05s^{0.8}+0.35s^{0.3}+0.45s^{0.5}+0.15} \quad (7)$$

4.2. System 2 (G₂(s))

The FDE represented by equation (8) has three fractional order derivatives with orders α_1, α_2, and β

$$D_t^{\alpha_1} y(t) + a_1 D_t^{\alpha_2} y(t) + a_2 y(t) = D_t^{\beta} u(t) + bu(t) \quad (8)$$

after taking the AB derivative, and substituting values of β =0.3, $\alpha_1 = 0.8$, and α_2=0.5. The arbitrary constants are set to 1.

The equation reduces to

$$\left(\frac{s^{0.8}}{0.2s^{0.8}+0.8} + \frac{s^{0.5}}{0.5s^{0.5}+0.5} + 1\right) Y(s) = \left(\frac{s^{0.3}}{0.7s^{0.3}+0.3} + 1\right) U(s) \quad (9)$$

$$\boldsymbol{G_2(s)} = \frac{\left(\frac{\boldsymbol{s^{0.3}}}{\boldsymbol{0.7s^{0.3}+0.3}}+\boldsymbol{1}\right)}{\left(\frac{\boldsymbol{s^{0.8}}}{\boldsymbol{0.2s^{0.8}+0.8}}+\frac{\boldsymbol{s^{0.5}}}{\boldsymbol{0.5s^{0.5}+0.5}}+\boldsymbol{1}\right)} \quad (10)$$

$$G_2(s) = \frac{\frac{1.7s^{0.3}+0.3}{0.7s^{0.3}+0.3}}{\left(\frac{1.2s^{0.8}+0.8}{0.2s^{0.8}+0.8}+\frac{1.5s^{0.5}+0.5}{0.5s^{0.5}+0.5}\right)} \quad (11)$$

After simplifying the expression in equation (11), it reduces to equation (12),

$$G_2(s) = \frac{0.07s^{1.6}+0.03s^{1.3}+0.07s^{1.1}+0.31s^{0.8}+0.12s^{0.5}+0.28s^{0.3}+0.12}{0.56s^{1.6}+0.24s^{1.3}+0.42s^{1.1}+1.02s^{0.8}+0.36s^{0.5}+0.28s^{0.3}+0.12} \quad (12)$$

The system represented by equation (8) is an FO order dynamic system with AB derivative. The system presents asymptotic stability, with the system states converging to equilibrium as time tends to infinity.

4.3. System 3 (G₃(s))

The nonminimum phase system with FDE, which has fractional derivative operators $\alpha$and β.

$$D^{\alpha} y(t) + ay(t) = D^{\beta} u(t) - bu(t), \quad (13)$$

TF of the equation is simplified as below, with the values of β =0.2 and α =0.8.

$$\left(\frac{s^{0.8}}{0.2s^{0.8}+0.8} + 1\right) Y(s) = \left(\frac{s^{0.2}}{0.8s^{0.2}+0.2} 1\right) U(s) \quad (14)$$

$$G_3(s) = \frac{\left(\frac{s^{0.2}}{0.8s^{0.2}+0.2}-1\right)}{\left(\frac{s^{0.8}}{0.2s^{0.2}+0.8}+1\right)} \quad (15)$$

$$G_3(s) = \frac{0.04s^{0.4}+0.2s^{0.2}-0.16}{0.8s+0.2s^{0.8}+0.16s^{0.4}+0.68s^{0.2}++0.16} \quad (16)$$

The system presents asymptotically stable behavior with FO dynamics governed by the AB operator. The non-singular kernel exhibits smooth transients, finite memory, and Mittag–Leffler-type decay.

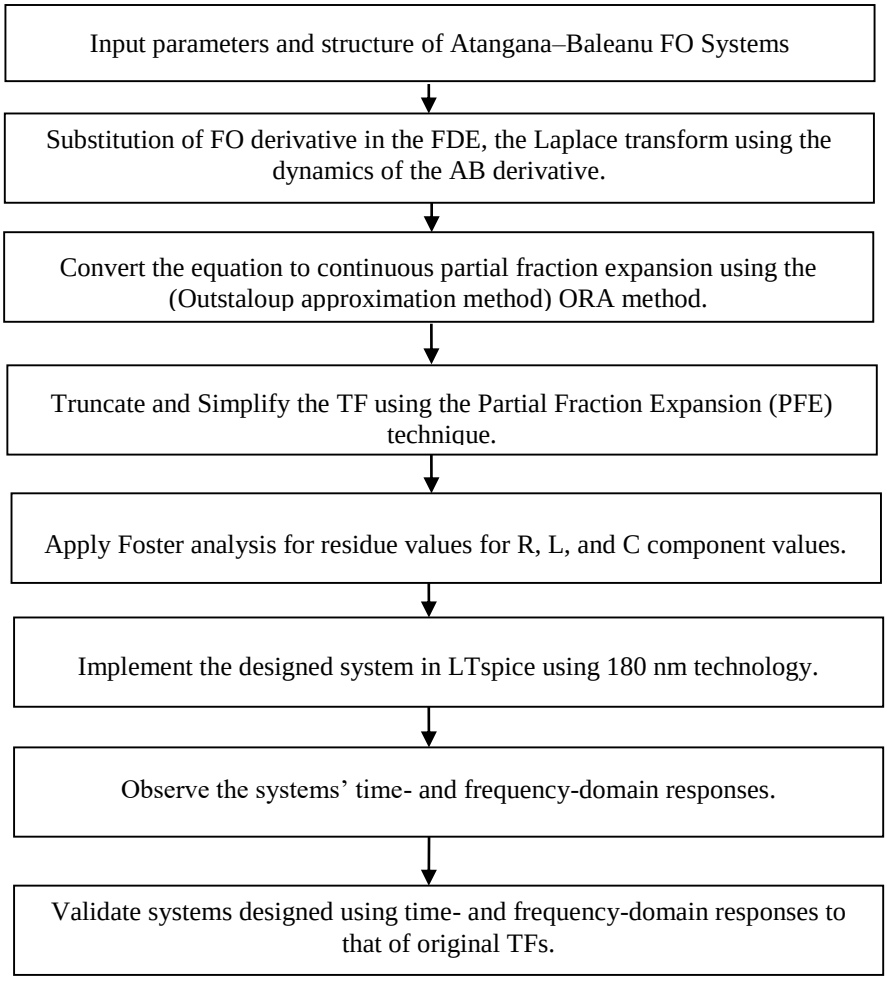

Fig. 1 Flowchart of the design process

5. Design of Analog Systems and Discussion

This section shows the analog design for the FO systems discussed in the previous section for different values of the FO derivative governed by the AB derivative. The circuit is designed and simulated using the LTspice XVII software tool, a high-performance SPICE-based circuit simulator. All simulations are carried out at the schematic level using CMOS device models to verify the functional correctness and dynamic performance of the design [22].

The configuration of the system incorporates the op-amp and resistor-capacitor network in series or parallel. This type of network synthesis is carried out using either Foster or Cauer analysis methods. This method requires the Transfer Function (TF), the Vout ratio to Vin forms the TF. The two approaches in network synthesis are used to model LTI systems with equivalent RC, RL, or LC networks. In Foster impedance form, which realizes a network as a parallel LC, LC, or RL series connection. Foster II is an admittance form system that realizes a network as a parallel connection of series LC, RC, and RL circuits. Cauer analysis is a method used in network synthesis to present a system with a given impedance or admittance function as a ladder network consisting of inductors (L), capacitors (C), or resistors (R), depending on the system. The behaviour of the designed analog systems is validated with the frequency-domain and time-domain responses of the TF generated using MATLAB [41]. The design software offers an Electronic Design Automation (EDA) tool, which starts with designing, simulating, verifying, and implementing the analog systems [45, 46].

The sequence of steps followed in the design is presented below:

1. Substitute the value of the FO derivative in the FDE governing equation and take the Laplace transform using the dynamics of the AB derivative.
2. Convert the above equation to a continued partial fraction expansion by using the Oustaloup recursive approximation method, which may have a higher-order polynomial.
3. Simplify the TF using the Partial Fraction Expansion (PFE) technique to analyse and synthesise the linear systems.
4. Design of the system is carried out using Foster analysis.

The residue values obtained from the PFE are directly mapped to the R, L, and C component values.

5. Implement the designed system in the LTSpice software in 180nm technology.
6. Validate the analog systems designed in step 5 with those of the original TFs.
7. The systems' time and frequency domain responses, including step response and Bode plots, are observed.

5.1. Design and Implementation of $G_1(s)$

This section presents the design of the analog systems following the aforementioned procedure.

$$G_1(s) = \frac{(1.7s^{0.3}+0.3)(0.5s^{0.5}+0.5)}{(0.7s^{0.3}+0.3)(1.5s^{0.5}+0.5)} \tag{17}$$

After simplifying the above equation using ORA approximation and substituting the values in MATLAB simulation software, the residue values are obtained as shown below in equation (18).

$$G_1(s) = \frac{\begin{array}{c}4.655\times10^{5}s^{20}+2.839\times10^{9}s^{19}+6.331\times10^{12}s^{18}+6.185\times10^{15}s^{17}\\+2.318\times10^{18}s^{16}+8.665\times10^{19}s^{15}+6.346\times10^{20}s^{14}+7.313\times10^{20}s^{13}\\+1.657\times10^{20}s^{12}+2.298\times10^{17}s^{11}+1.191\times10^{14}s^{10}+2.847\times10^{10}s^{9}\\+3.164\times10^{6}s^{8}+151.9s^{7}+3.252\times10^{-3}s^{6}+2.882\times10^{-8}s^{5}\\+8.816\times10^{-14}s^{4}+6.976\times10^{-24}s^{3}+1.823\times10^{-34}s^{2}\\+1.752\times10^{-45}s+5.562\times10^{-57}\end{array}}{\begin{array}{c}5.816\times10^{5}s^{20}+3.545\times10^{9}s^{19}+7.904\times10^{12}s^{18}+7.717\times10^{15}s^{17}\\+2.889\times10^{18}s^{16}+1.069\times10^{20}s^{15}+7.461\times10^{20}s^{14}+6.179\times10^{20}s^{13}\\+1.332\times10^{20}s^{12}+1.881\times10^{17}s^{11}+1.008\times10^{14}s^{10}+2.535\times10^{10}s^{9}\\+2.998\times10^{6}s^{8}+148.7s^{7}+3.235\times10^{-3}s^{6}+2.882\times10^{-8}s^{5}\\+8.816\times10^{-14}s^{4}+6.976\times10^{-24}s^{3}+1.823\times10^{-34}s^{2}\\+1.752\times10^{-45}s+5.562\times10^{-57}\end{array}}, \tag{18}$$

The steps involved in the process of design and implementation of FO systems using AB derivative are shown in Figure 1. The Partial Fraction Expansion (PFE) of the system's TF depicted in equation (19) yields the residues corresponding to its poles and zeros, which are subsequently used to calculate the resistor and capacitor values of the circuit.

$$G_1(s) = \frac{0.800405+\frac{1.20}{s+1117}+\frac{0.610}{s+0.538}-\frac{0.0232}{s+1128}}{-\frac{0.261}{s+0.378}-\frac{0.0000330}{s+0.000164}-\frac{0.00000002988}{s+0.000164}}, \tag{19}$$

The equation is compared to the Foster 1 form expression to calculate the resistor and capacitor values in the circuit.

$$Z(s) = k_0+\frac{k_1}{s-s_1}+\frac{k_2}{s-s_2}+\cdots+\frac{k_n}{s-s_n}. \tag{20}$$

Equation (20) shows Foster's form I, which is an implementation of the TF to a network containing RC pairs from its impedance function. The value of n indicates the total number of poles in the equations. The expression representing the transfer function of the system can be simplified by obtaining its PFE, which shows the coefficients of the values k_0, k_1, k_2…k_n and s_0, s_1, s_2…sn representing the poles of the expression.

The network synthesis form of the expression is the sum of parallel impedances,

$$Z(s) = R+\frac{\frac{1}{C_1}}{s-\frac{1}{R_1C_1}}+\frac{\frac{1}{C_2}}{s-\frac{1}{R_2C_2}}+\cdots+\frac{\frac{1}{C_n}}{s-\frac{1}{R_nC_n}}. \tag{21}$$

Comparing the Foster I form equation with the equations of the system $G_1(s)$, the circuit realization obtained is shown in Figure 2.

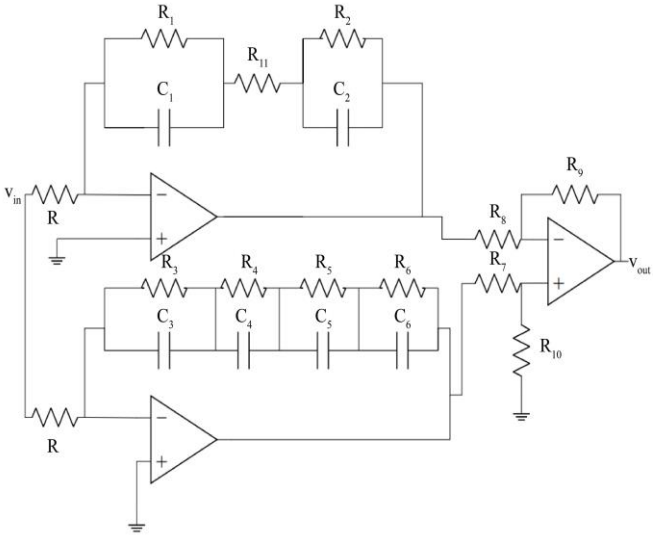

Fig. 2 Analog System design for $G_1(s)$

The component values for the above system are calculated and tabulated below.

Table 1. Components values for the system $G_1(s)$

Component	Values for $G_1(s)$
R_1 to R_{11}	1.074k,1.13M,20, 690k,201k,182, 100k,100k,10k,10k,800k
C_1 to C_6	0.83µ, 1.63 µ , 42.94 µ 3.83 µ , 0.03028, 33
R	1MΩ

Following the guidelines given in [12-14, 42], the implementation of an analog system for $G_1(s)$ starts with the two-stage op-amp design, which has a differential amplifier at the input followed by a common source amplifier as a second stage. The designed op-amp is shown in the Figure below.

The op-amp is designed for a gain value of 60dB, slew rate 5V/v, GBW 5MHz, and Power Dissipation 300mw. The designed op-amp is encapsulated in a symbol and is used in the implementation of an analog circuit for $G_1(s)$ using 180nm technology. The operational amplifier is encapsulated as a symbol. The same op-amp is used in the implementation of an analog circuit for the FO systems. Figure 3 demonstrates the op-amp designed in LTspice software.

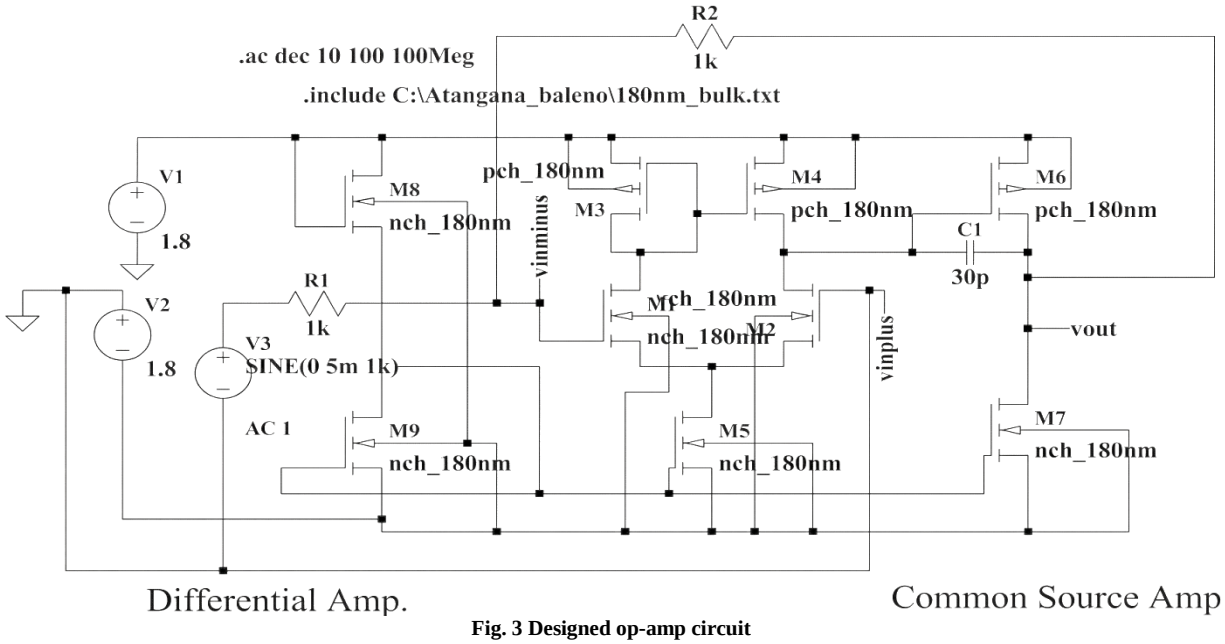

Fig. 3 Designed op-amp circuit

The op-amp has two different sections; the first section is a differential amplifier, followed by a common-source amplifier. The first section is used for a high Common Mode Rejection Ratio (CMRR), and the second circuit aids the gain for the circuit.

Table 2 mentions the MOSFET sizing required to use the op-amp circuit with high gain and takes care that all the MOSFETS work in saturation condition for maximum throughput.

Table 2. Components values for the system $G_1(s)$

Component	Value
Supply voltage	-1.8 to 1.8 V
$M_{(1,2)}$ (W/L)	20µm/500nm
$M_{(3,4)}$ (W/L)	1µm/1µm
M_5(W/L), M_6(W/L)	2µm/1µm, 40µm/500nm
W/L for M_7 to M_9	56µm/500nm,500nm/5µm, 2µm/1µm

Transistor sizing, the process of choosing the width (W) and length (L) of a MOSFET, is obtained for each transistor of the op-amp to optimize the parameters like gain, bandwidth and power requirement of the op-amp. The designed parameters are used to implement the op-amp in the LTspice simulation Software. The op-amp designed in Figure 2 is considered in this work and is used in the analog system $G_1(s)$, which is implemented in LTspice using the component values referred to in Table 1. Figure 4 shows the implemented circuit for the system mentioned in Section 3.

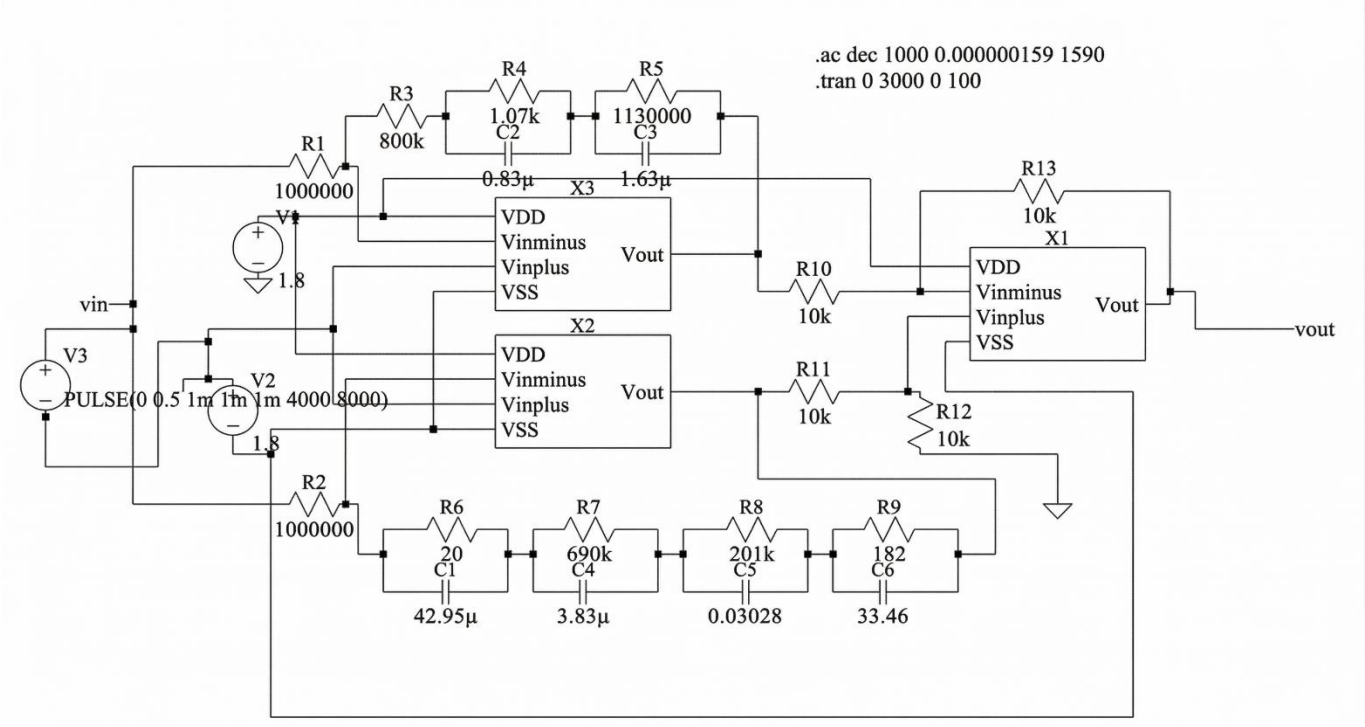

Fig. 4 Implemented Design for $G_1(s)$

To observe the step response of the analog system for $G_1(s)$, the input excitation of 0.5 V is applied to the circuit.

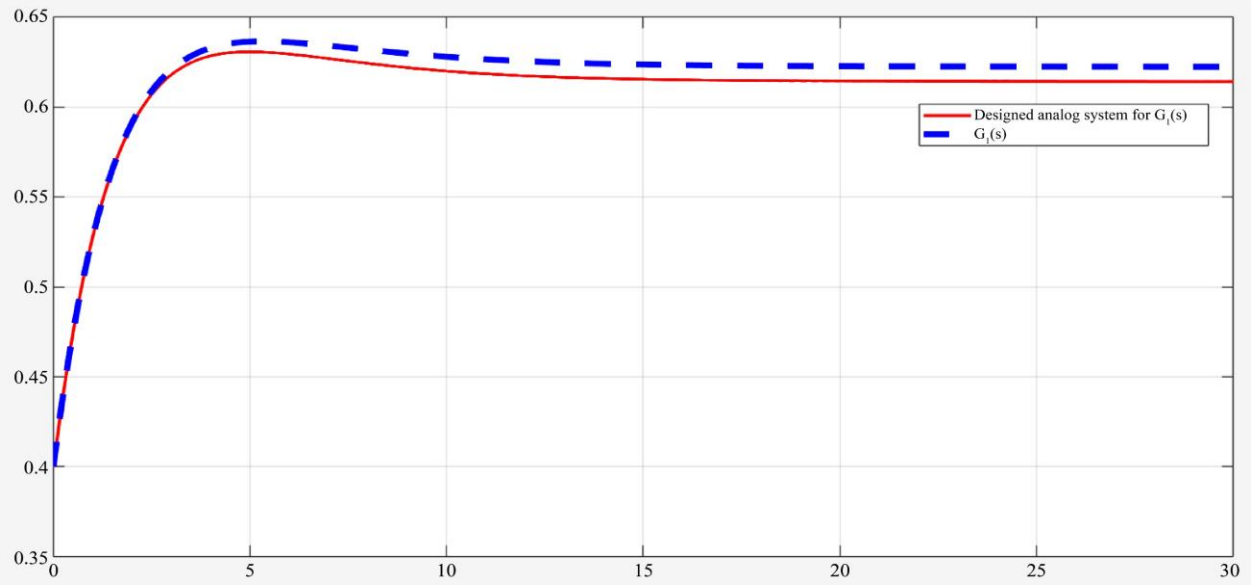

Fig. 5 Step Response for $G_1(s)$ and its designed analog system

The performance evaluation of the designed system is done by observing the Mean Squared Error (MSE) of the achieved time-domain response with that of the original one. Key performance indices considered in the analysis include rise time, peak overshoot, and settling time for all systems. The formula for calculating the MSE is shown in equation 20, and the values calculated for $G_1(s)$ are shown in Table 3.From the time domain response and frequency domain response, it is observed that the implemented analog system faithfully captures the dynamics of the original system.

The frequency response is recorded and presented below

Table 3. MSE calculation for a step response $G_1(s)$

Technology	$G_1(s)$(MSE)
180nm	1.41

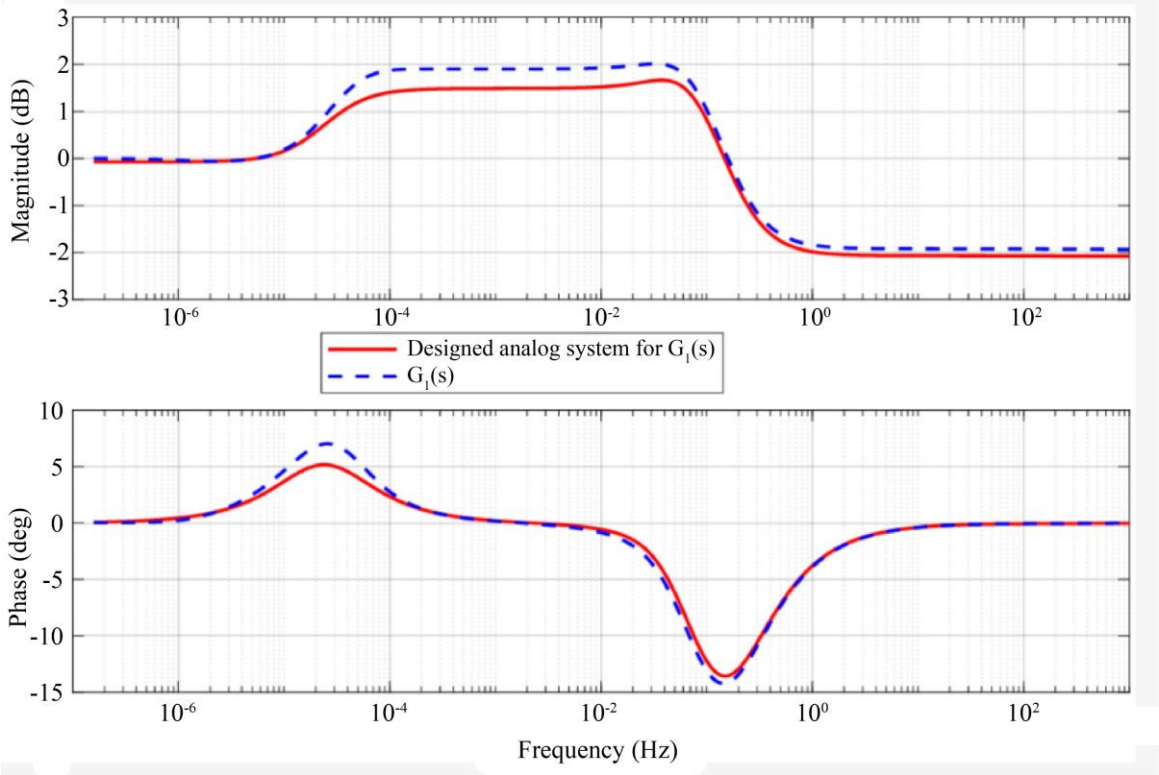

Fig. 6 Frequency domain validation for $G_1(s)$ and its analog system.

$$\text{MSE} = \frac{1}{n}\sum_{i=1}^{n}(y_s(i) - y_{as}(i))^2, \quad (20)$$

n = Number of samples
$y_s(i)$ = Output of the CL system at the i^{th} instant
$y_{as}(i)$ = Output of the analog CL system at the i^{th} instant

Table 4. Evaluation for time domain performance indices for $G_1(s)$

	$G_1(s)$	Analog System for $G_1(s)$
Rise Time	1.4136	1.3115
Settling Time	6.618	7.1923
Overshoot	2.28	2.699
Peak	0.6365	0.6307

5.2. Design and Implementation of System 2: -G2(s)

As explained in Section 3, the system $G_2(s)$ is designed using 180nm technology. The partial fraction expansion of $G_2(s)$. By using the ORA approximation, the above expression reduces to,

$$G_2(s) = \frac{\begin{array}{c}0.2987s^{12} + 1009s^{11} + 1.137\times10^{6}s^{10} + 4.3\times10^{8}s^{9} \\ +2.399\times10^{9}s^{8} + 2.598\times10^{9}s^{7} + 5.794\times10^{8}s^{6} \\ +9.242\times10^{5}s^{5} + 510.4s^{4} \\ +0.1188s^{3} + 1.118\times10^{-5}s^{2} \\ +3.078\times10^{-10}s + 1.823\times10^{-15}\end{array}}{\begin{array}{c}s^{12} + 3372s^{11} + 3.793\times10^{6}s^{10} + 1.427\times10^{9}s^{9} \\ +4.176\times10^{9}s^{8} + 2.702\times10^{9}s^{7} + 4.68\times10^{8}s^{6} \\ +7.564\times10^{5}s^{5} + 430.8s^{4} \\ +0.1063s^{3} + 1.084\times10^{-5}s^{2} \\ +3.078\times10^{-10}s + 1.823\times10^{-15}\end{array}}, \quad (20)$$

The above equation reduces to the following form after partial-fraction expansion:

$$G_2(s) = 0.298 + \frac{1.22}{s+1112} + \frac{0.4365}{s+2.11} + \frac{0.3450}{s+0.538} + \frac{0.0270}{s+0.287} - \frac{0.0229}{s+1128} - \frac{0.735}{s+1127} - \frac{0.000000176}{s+0.000270}, \quad (21)$$

By Foster 1 analysis, the component values are calculated, and the circuit is designed for $G_2(s)$ as shown in the figure.

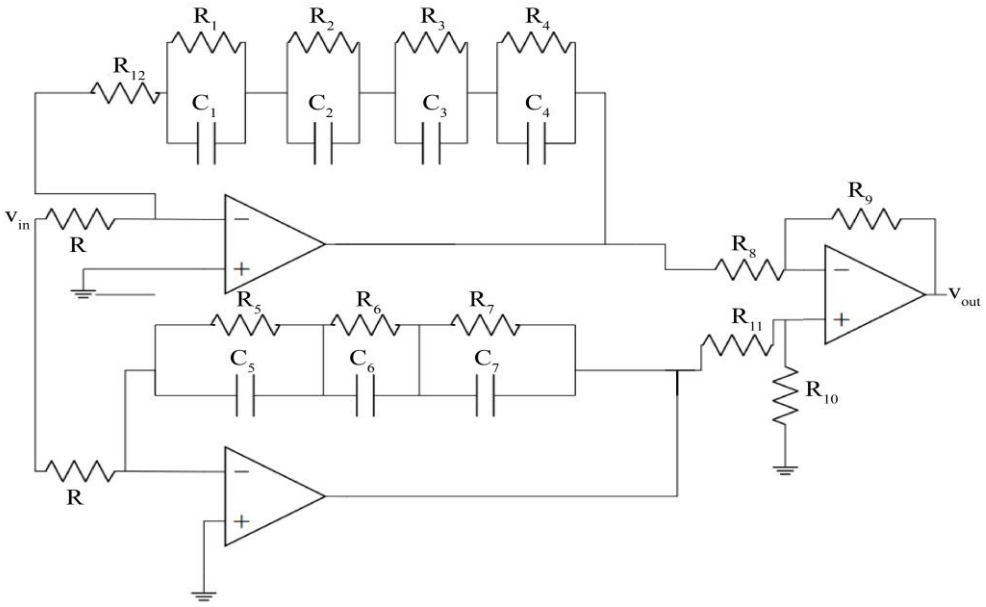

Fig. 7 Analog System design for $G_2(s)$.

Figure 7 represents the circuit diagram designed for $G_2(s)$, and Table 5 shows the required component values for the design of $G_2(s)$.

Table 5. Component values for $G_2(s)$.

Component	Values for $G_1(s)$
R_1 to R12	1.1k, 206k, 641k, 94k, 20, 652, 649, 10k, 10k, 10k, 10k, 298k
C_1 to C_7	0.8µ, 2.29 µ, 2.89 µ, 37µ, 43 µ, 1.36µ, 5.67
R	1MΩ

The system is implemented for $G_2(s)$ as shown in Figure 8.

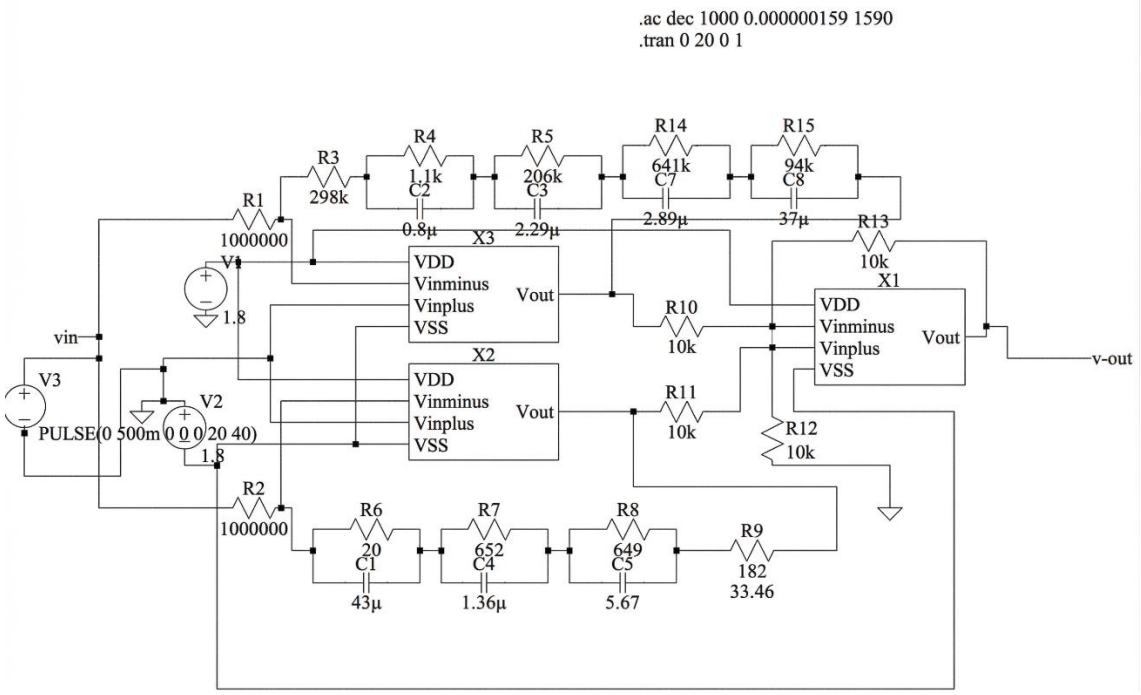

Fig. 8 Implemented system for $G_2(s)$.

The implemented system is applied with an input excitation of 0.5 V. The unit step response shows the behavior of a system in time when subjected to a sudden change. It reflects the dynamic behavior of the system.

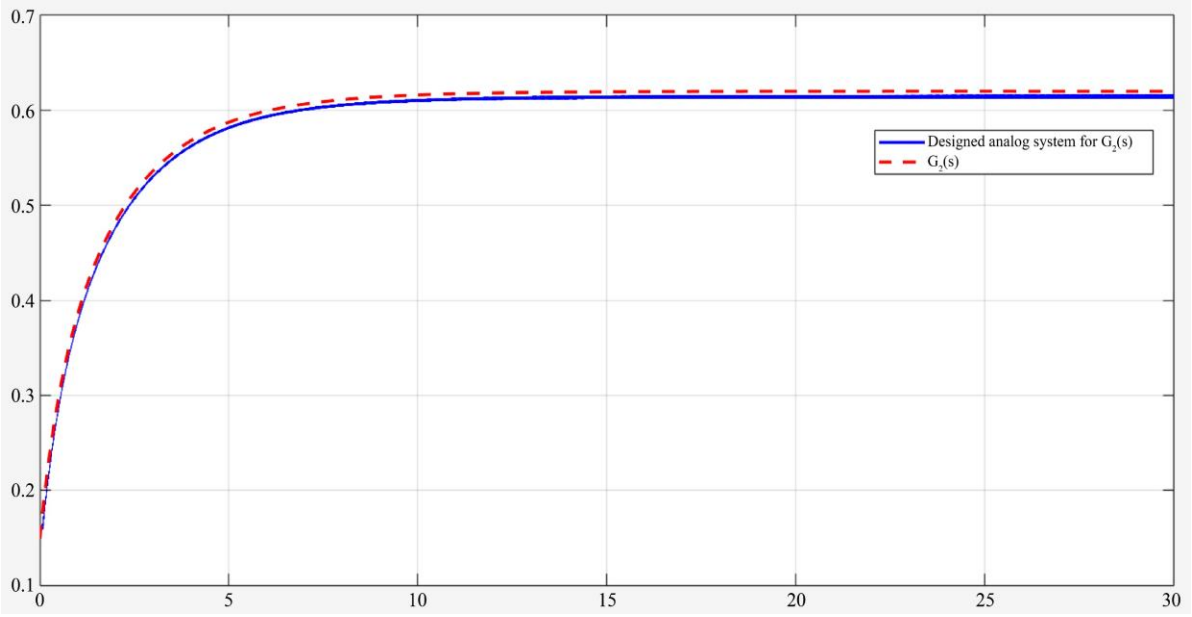

Fig. 9 Step Response for $G_2(s)$ and its designed analog system.

Table 6. MSE calculation for a step response $G_2(s)$

Technology	G2(s)(MSE)
180nm	1.06

Table 7. Evaluation for time domain performance indices for $G_1(s)$.

	$G_2(s)$	Analog System for $G_2(s)$
Rise Time	1.6194	1.67
Settling Time	5.1732	5.39
Overshoot	0 .0076	0.0001
Peak	0.6199	0.6159

The frequency domain validation for the system $G_2(s)$ is observed at the frequency range from 10^{-4} to 10^{3}

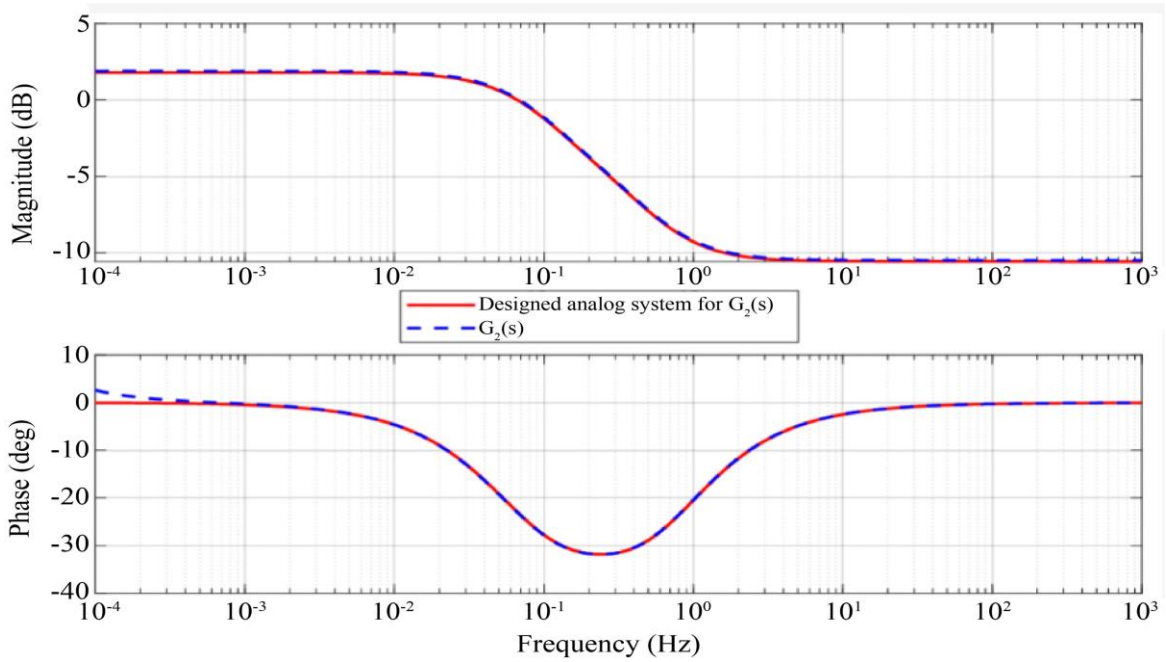

Fig. 10 Frequency domain validation for $G_2(s)$ and its designed analog system.

5.3. Design and implementation of System 3: - $G_3(s)$

The nonminimum phase system with FDE, which has α and β as fractional derivative operators, is stated below.

$$G_3(s) = \frac{\left(\frac{s^{0.2}}{0.8s^{0.2}+0.2}-1\right)}{\left(\frac{s^{0.8}}{0.2s^{0.2}+0.8}+1\right)}, \qquad (22)$$

The circuit is implemented for the components mentioned in Figure 10 and a designed op-amp. The above expression is simplified using ORA,

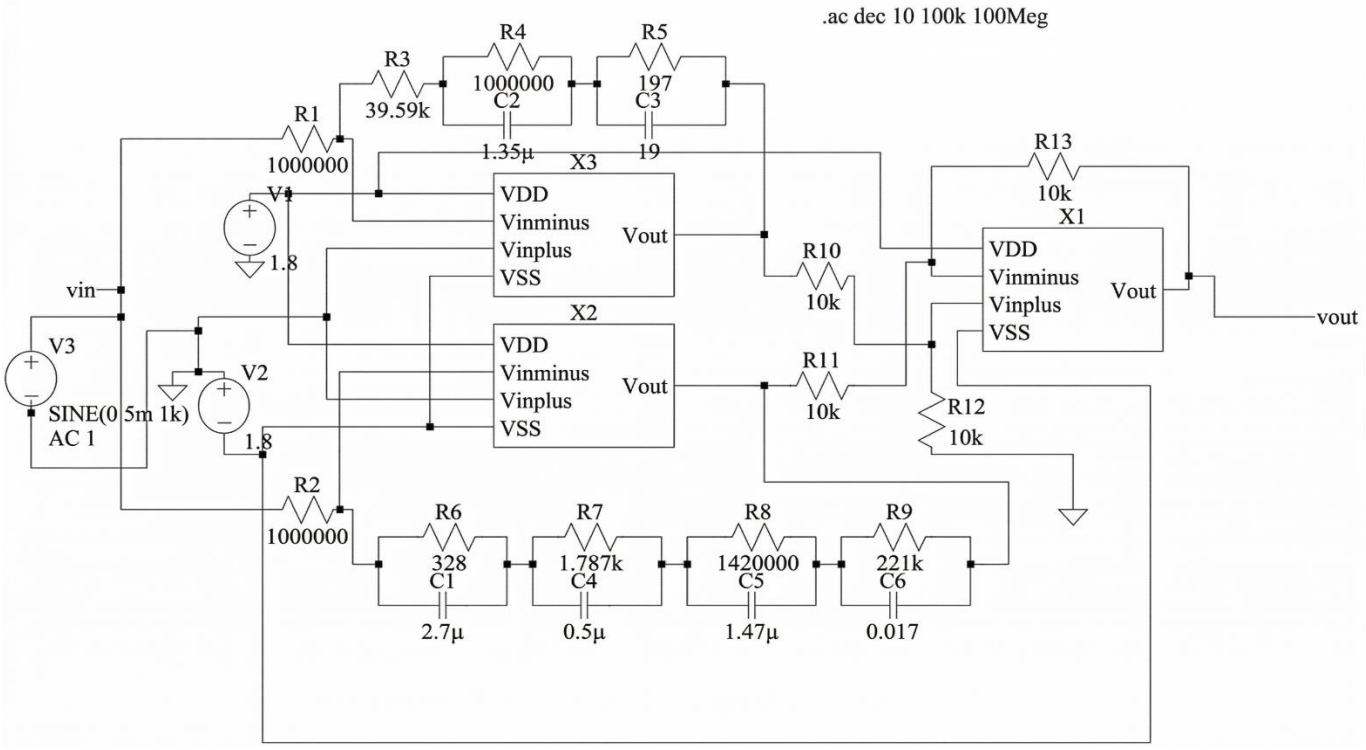

Fig. 11 Analog system implemented for $G_3(s)$

By calculating component values using Foster's 1 form, the circuit diagram is as follows: the component values are shown in Figure 10.

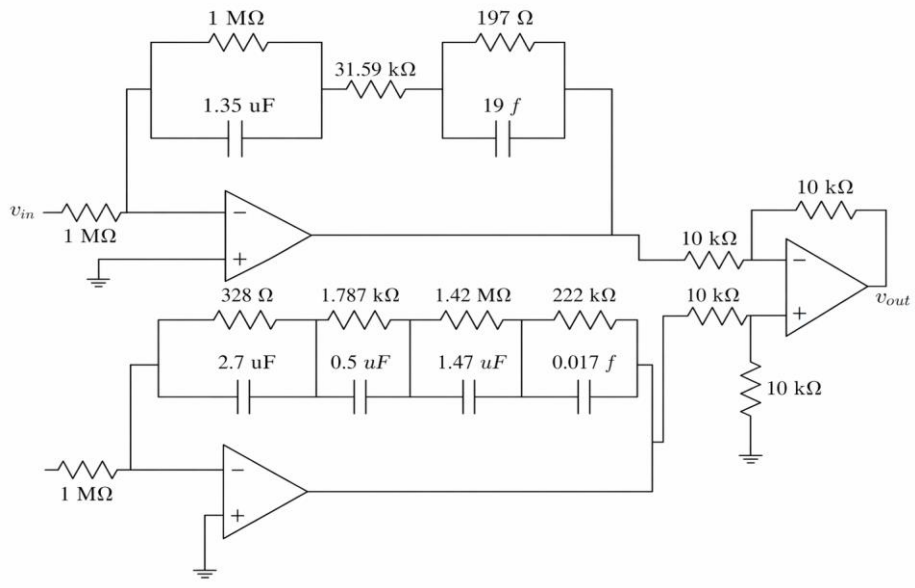

Fig. 12 Analog Design for $G_3(s)$

The response of the above system is taken by applying an excitation voltage of 0.5 V.

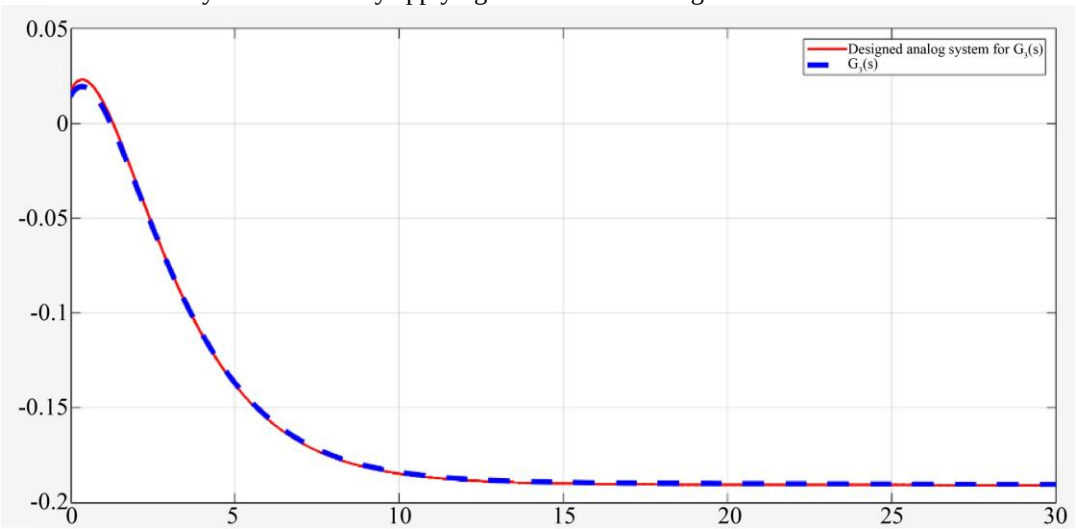

Fig. 13 Step Response for $G_3(s)$ and its designed analog system

Table 8. MSE calculation for a step response $G_3(s)$

Technology	$G_3(s)$(MSE)
180nm	0.003

Table 9. Evaluation for time domain performance indices for $G_3(s)$

	$G_3(s)$	Analog System for $G_3(s)$
Rise Time	5.76	5.65
SettlingTime	11.2296	11.10
Overshoot	0	4.9278e-05
Peak	0.1902	0.1908

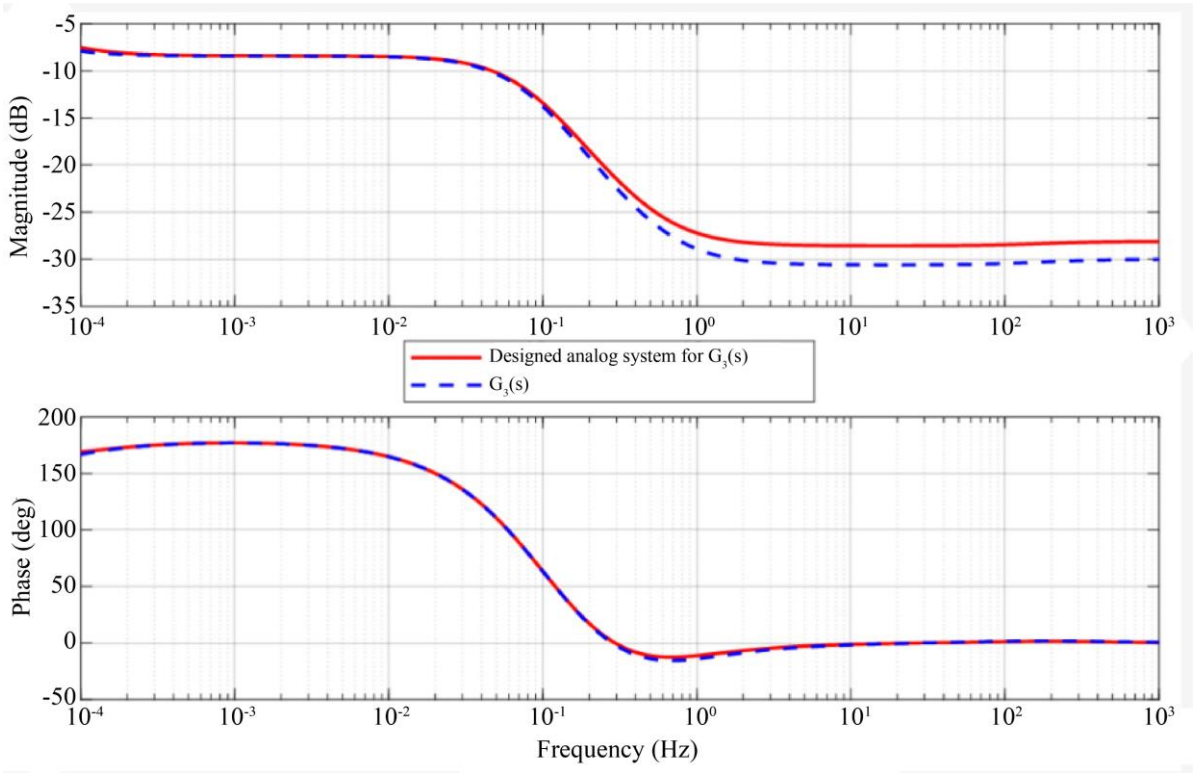

Fig. 14 Frequency domain validation for $G_3(s)$

6. Conclusion

This work has presented a systematic methodology and practical realization using analog circuits of fractional-order (FO) systems using Atangana–Baleanu fractional derivative. By integrating Foster and Cauer network synthesis techniques with the Oustaloup recursive approximation, accurate analog implementations of FO dynamics were achieved over a prescribed frequency range. The proposed circuits were designed and validated in the LTspice environment using a standard 180-nm CMOS technology, offering a favourable compromise between performance, design complexity, and implementation feasibility. Time-domain and frequency-domain analyses confirm that the proposed analog systems faithfully reproduce the dynamics of the corresponding theoretical fractional-order models, with close agreement observed in key performance metrics such as rise time, settling time, peak overshoot, and mean square error. The proposed methodology provides a flexible and scalable platform for the practical realization of fractional-order systems and can be readily extended in several directions. Future work may focus on the experimental fabrication and measurement of the proposed circuits to further validate their practical applicability. The design approach can also be extended to other fractional derivatives and approximation techniques, as well as to lower-geometry CMOS technologies for improved area and power efficiency. Additionally, the integration of the proposed fractional-order circuits into closed-loop control systems, signal processing architectures, and adaptive or reconfigurable analog platforms represents a promising direction for further research.

Conflicts of Interest

The authors clarify that they do not have conflicts of interest in relation to the publication of this work.

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