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Original Article

A Four-Switch Six-Port Non-Isolated DC–DC Converter with Finite-Control-Set Predictive Regulation for 100 kW Electric-Vehicle Traction Integration

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Abstract *- This paper presents the design, modeling, and predictive regulation of a non-isolated six-port DC-DC converter intended for 400 V Electric-Vehicle (EV) traction power-trains at the 100-kW operating level. The topology aggregates three input sources-a 98 V auxiliary input (V1), a 200 V high-voltage battery pack (V2), and a 48 V series-aid battery (V3)-and delivers regulated power to a 400 V traction bus (100 kW), a 24 V auxiliary bus (1 kW), and a 12 V housekeeping rail (250 W) using only four MOSFETs. A shared inductor pathway (L1+L2) carries the dominant boost current, while two dedicated inductors (L3 and L4) serve the auxiliary buck stages. A six-state discrete-time model is derived and embedded in a single-step finite-control-set model predictive controller (FCS-MPC) operating at Ts = 10 µs. At every sample, the controller enumerates the sixteen valid combinations of M1–M4, propagates the predicted state vector through a Tustin-discretized plant, and selects the combination that minimizes a weighted quadratic tracking cost subject to inductor-saturation and capacitor-voltage limits. PLECS simulation reports regulation bands of ±350 mV at 400 V, ±24 mV at 24 V, and ±17 mV at 12 V, with 32.6 dB cross-port disturbance attenuation at 1 kHz under a 250 A traction-bus step. A twenty-nine-line loss audit closes to 3 587 W and predicts an efficiency of 96.6 % at 101.25 kW; a two-stage common-mode filter attenuates the 200 kHz second harmonic by 41.7 dB in simulation, which is 2.3 dB short of the 44 dB budget required for CISPR 25 Class 5 and therefore identifies filter margin recovery as an open item for hardware validation. A comparison with four multi-port EV converters reported between 2022 and 2026 places the proposed design two to three orders of magnitude above the power level at which those designs were validated, so the comparison establishes the power-class gap this work addresses rather than an efficiency ranking.*

Keywords *- Multi-port DC-DC converter, Electric vehicle, 400 V traction, Model predictive control, Finite control set, MIMO power electronics, Lyapunov stability, Magnetic saturation, EMI filter.*

1. Introduction

Electric-Vehicle (EV) power-trains have moved decisively toward 400 V and 800 V traction architectures over the past five years. Where first-generation EVs operated from 250–360 V battery packs at peak power levels under 80 kW, current production platforms operate traction inverters from 400 V (and increasingly 800 V) battery packs at 100-250 kW for sustained acceleration and fast charging [1-4]. As the peak traction power has grown, so has the rest of the vehicle's electrical complement: thermal-management actuators and the battery-management system commonly require a regulated 24 V rail, while microcontrollers, sensors, infotainment, and cabin electronics still draw from a legacy 12 V bus [5-7]. The natural question for a 400 V EV is whether the conventional architectural response-cascading two or three two-port DC-DC stages, each with its own magnetics and control loop-can be replaced by a single integrated converter that exposes the minimum number of switches to the gate driver.

The conventional cascaded response uses eight to twelve active switches in total, four to six magnetic cores, and three or four independent control loops [8, 9]. At the 100 kW class, this approach accumulates substantial conduction and switching losses, magnetic volume, EMI overhead, and parts-count penalties. Integrating the three regulation functions into a single non-isolated Multi-Port Converter (MPC) with the lowest possible gate-signal count is therefore an active research direction [7, 10-13]. A close reading of the recent literature, however, reveals two persistent obstacles to a clean six-port deployment at the 100 kW class. The first arises whenever a single inductor pathway is shared between a high-

power boost stage and one or more auxiliary buck stages. The resulting plant is strictly multivariable: a 250 A load step on the 400 V traction port instantaneously perturbs the shared inductor current and propagates a disturbance to every auxiliary output through the common impedance. Decoupled PI loops—the workhorse of single-port designs-cannot suppress this cross-coupling without unacceptable bandwidth de-rating, nor can they easily incorporate the hardware constraints (peak inductor current, capacitor-voltage envelope) that the design imposes [7, 11].

The second obstacle concerns the alternatives. Sliding-mode and other variable-structure controllers can robustly stabilize the plant, yet the chattering management and Lyapunov-gain tuning scale unfavorably as the number of regulated outputs grows. Optimization-based predictive strategies sidestep both problems, but published applications to multi-port DC-DC converters have so far remained below the 5-kW class [14-17].

The research gap can therefore be stated precisely. The 2020–2026 literature contains no non-isolated six-port converter that simultaneously (i) operates at the 100 kW traction class, (ii) requires only four independent gate signals, and (iii) is regulated by a constraint-aware predictive controller whose closed-loop stability is certified rather than assumed. Reported four-switch non-isolated designs remain single-output converters validated at far lower power levels [18], while published optimization-based and predictive control studies for multi-port DC–DC conversion remain confined to the sub-5-kW class [14-17]. The problem addressed in this paper is the closure of that gap: bringing finite-control-set predictive regulation to the 100 kW multi-port class while holding the gate-signal count at four and proving, rather than asserting, closed-loop stability.

The work reported here addresses this gap through a six-port non-isolated DC–DC converter that combines five elements:

1) A four-gate-signal six-port topology operating at 100 kW - A shared L_1+L_2 inductor pathway carries the high-power boost current to the 400 V traction bus, while two independent buck stages with dedicated inductors L_3 (12 V) and L_4 (24 V) supply the auxiliary rails. Exactly four independent gate signals drive the four MOSFETs M_1, M_2, M_3, and M_4.
2) Single-step FCS-MPC with a per-switch averaged decomposition - The shared pathway makes the converter strictly MIMO. A six-state discrete-time state-space MIMO model is derived, and finite-control-set MPC is applied to it. The averaged plant is constructed as Aavg = A0 + DM1·(A1−A0) + DM3·(A2−A0) + DM4·(A3−A0), in which the four duty cycles are independent variables on [0, 1]. This decomposition correctly admits the overlapping switching states that the FCS-MPC enumerates and avoids the spurious convex-partition constraint imposed by the conventional mode-mixing form.
3) Per-inductor volt-second realizability proof - Steady-state feasibility is established analytically by writing the volt-second balance on each of the four physical inductors-L1, L2, L3, and L4-across the three operating modes. The resulting duty cycles are DM1 = DM2 ≈ 0.258 for the 12 V port from V3, DM3 ≈ 0.485 for the 24 V port from the V1−V3 = 50 V effective drive, and DM4 ≈ 0.381 for the 400 V port from the V2+V3 = 248 V effective input.
4) Saturation-aware magnetic design at worst-case I_{pk} - With IL2, pk reaching 521 A under the deep-discharge condition, the L1+L2 powder-core selection is forced to a high-saturation Fe–Si distributed-gap material that preserves at least 60 % of nominal permeability across the full operating envelope.
5) A discrete-time Lyapunov certificate for the FCS-MPC law - A quadratic Lyapunov function on the tracking-error coordinates-evaluated on the Tustin-discretized plant with the design choice Q = 0.10·I—decreases along the optimal FCS-MPC trajectory. This yields a closed-form geometric convergence rate ρ ≈ 0.78 and a residual ultimate bound of normalized radius δ∞ ≤ 0.484.

The rest of the paper is arranged as follows. Section 2 surveys recent literature on multi-port EV converters and their control. Section 3 describes the proposed topology. Section 4 develops the steady-state analysis, the per-inductor volt-second balance, and the magnetic-saturation verification. Section 5 derives the discrete-time MIMO model and the per-switch averaged form.

Sections 6 and 7 present, respectively, the FCS-MPC formulation and the Lyapunov stability certificate. Section 8 addresses the thermal stress on the high-power switch and the switching-frequency behavior of the predictive controller. Section 9 covers the EMI filter design, with emphasis on the common-mode stage. Section 10 reports the closed-loop simulation performance, the twenty-nine-line loss audit, and the comparison with prior art. Section 11 concludes.

2. Literature Survey

Multi-port DC-DC converters for electric mobility have drawn steady research interest since the mid-2010s, and enough 2020-2026 reports now exist to support a focused review.

Three threads are relevant to the present work: the architectural patterns and switch counts that have emerged in non-isolated multi-port designs, the power levels that have been demonstrated, and the control strategies that have been applied. Each thread is discussed in turn.

2.1. Non-Isolated Multi-Port Topologies

Early non-isolated multi-input designs were primarily aimed at hybrid energy storage, with two to three input sources and a single bus output. Akar et al. [19] reported a bidirectional non-isolated multi-input converter for hybrid storage in EVs; Bairabathina and Balamurugan [8] later compiled a comprehensive review of non-isolated multi-input step-up converters for grid-independent hybrid EVs. Nguyen et al. [20] proposed a family of integrated multi-input multi-output converters with a focus on shared-magnetic implementations. Varesi et al. [21] and Jalilzadeh et al. [22] tackled the related problem of high step-up ratio with reduced device count and lower switch voltage stress. These works collectively established the architectural vocabulary on which more recent designs build.

Around the same period, optimization studies for vehicle drivetrains made the trade-off between switch count, magnetics volume, and efficiency more concrete. Tran et al. [23] performed an NSGA-II co-design of an interleaved boost converter for an EV drivetrain, demonstrating that part-count reduction and efficiency are competing objectives that benefit from joint optimization. Chakraborty et al. [1] surveyed the broader DC–DC converter field for EVs, plug-in HEVs, and fast-charging stations, identifying multi-port consolidation as one of the persistent research directions. The reviews of Lipu et al. [2] and Islam et al. [3] reinforced this picture: the field has moved from single-port topologies toward consolidated multi-port designs, but the demonstrations have stayed in the kilowatt range.

More recent topology families have explored a wider range of port configurations. Suresh et al. [24] introduced a multifunctional non-isolated dual-input dual-output converter for EV applications, while Dhananjaya et al. [25, 26] reported single-input multi-output structures aimed at auxiliary power modules. Karthikeyan et al. [27] proposed a dual-input single-output converter for multi-source EV scenarios, and Shaik and Dhanamjayulu [28] synthesized a multiport dual-input dual-output structure for EVs. Bhattacharyya et al. [29] and Khasim et al. [30] focused on flexible non-isolated multiport implementations for battery and ultracapacitor integration. Dattaroy and Bhattacharya [18] are particularly relevant here: they explored a family of non-isolated four-switch DC-DC converters derived from the buck, boost, and buck-boost cells, offering a wide voltage-conversion ratio with closed-loop simulation validation, which makes that family the closest architectural relative of the present work in switch count, although each member serves a single output.

Several 2024-2026 reports have specifically addressed the EV traction context. Singh et al. [31] demonstrated a multi-load multi-source converter for EV power systems; Mookkan et al. [32] presented a modular buck-boost-based multiport bidirectional converter for hybrid electric vehicles; Reddy et al. [33] designed a multioutput converter with an optimal torque distribution for split-drive EVs. Vinusha et al. [34] reported a two-switch multiport non-isolated structure for on-board EV charging, and Bahadori et al. [35] presented a non-isolated DITO high step-up DC/DC converter with reduced switch voltage stress. The systematic review of Aravind et al. [7] catalogued the control techniques applied across this family of topologies, and Farajdanian et al. [11] complemented it with an analytical comparison of recent multiport DC/DC topologies. None of these recent reports, however, exceeds the 6 kW class in switching power.

2.2. Multi-Port Designs Aimed at Higher Power and Wider Use Cases

Beyond the low-power EV application range, multi-port research has expanded to fuel-cell vehicles, microgrid interface, and DC fast-charging. Sundarakamath and Natarajan [36] reported a single-inductor multi-input converter for fuel-cell hybrid EVs; Kim et al. [37] proposed an integrated multi-mode converter with a single inductor for fuel-cell EVs; Ma and Luo [38] addressed the three-power-source case in fuel-cell HEVs. Thapliyal et al. [39] integrated a bidirectional multi-source converter with a VSI-fed motor drive using a non-isolated topology. Reviews by Jiya et al. [6], Naik et al. [12], Mahyudin et al. [13], and Sakhare and Mikkili [4] established that as the power level and port count grow, the control problem becomes increasingly multivariable and the conventional decoupled-loop response becomes the limiting factor.

At the system level, Farag et al. [40] designed a single-stage non-isolated Y-converter for interlinking 400 V DC microgrids with the three-phase AC grid—the closest reported design in voltage class to the present work, though not at the 100 kW power level and not for a traction-integration use case. Reviews of bidirectional and multiport structures by Aravind et al. [10], Narayanaswamy and Mandava [9], Mostafa et al. [41], and Suresh et al. [42] confirm that no published non-isolated multi-port converter targets the simultaneous combination of a 400 V output bus, 100 kW traction power, and four independent gate signals.

2.3. Control Strategies for Multi-Port Converters

The control literature for multi-port converters splits broadly into three camps. The first applies classical decoupled PI loops to each output, often supplemented by feedforward terms or anti-windup logic-an approach that scales poorly with cross-coupling and is therefore confined to topologies in which the inductor pathways are largely independent. The second adopts variable-structure or sliding-mode strategies for bidirectional MIMO boost converters; the trade-off here is chattering, which complicates EMI compliance, and the difficulty of tuning multi-loop sliding gains. The third camp introduces optimization-based or model-based control. Olm et al. [14] applied an adaptive control law to a magnetically coupled multiport converter for electrified-vehicle applications; Biswas et al. [15] performed small-signal

modeling and decoupled controller design for a triple-active-bridge multiport converter; Sankarananth and Sivaraman [16] enhanced multiport bidirectional regulation with a resilient back-propagation neural network. More recently, S.J. et al. [17] modelled and controlled a single-input multi-output DC-DC converter in the port-controlled Hamiltonian framework.

Finite-control-set model predictive control occupies a distinct position within this third camp. It does not require an external PWM modulator, it accepts hard state constraints as part of the cost function, and it generalizes naturally to the MIMO setting.

However, surveys of multiport control [7], [11] indicate that the bulk of FCS-MPC applications to date have been at the single-converter or three-port level and at power ratings well below the traction class. The combination addressed by the present work—four independent gate signals, six ports, 100 kW, and FCS-MPC operating directly on the integer switching set—does not appear in the published record.

2.4. Identified Research Gap

Three concrete gaps emerge from the survey. First, no four-gate-signal six-port EV converter at the 100 kW class has been reported in the 2020–2026 literature. Second, no published implementation combines FCS-MPC with a shared-inductor four-switch six-port topology. Third, no prior work provides, in a single manuscript, a discrete-time Lyapunov stability certificate for MPC on a cross-coupled multi-port converter together with an explicit per-inductor volt-second realizability proof and a saturation verification at the worst-case $I_{pk} \geq 500$ A. The remainder of this paper addresses these gaps directly.

3. Proposed Topology

3.1. Circuit Description

The proposed converter combines three input ports, four magnetic cores, four MOSFETs, two passive Schottky freewheel diodes, a hybrid output-capacitor matrix, and three regulated loads, all sharing a common ground. The input ports are V_1 = 98 V (auxiliary input), V_2 = 200 V (high-voltage battery pack referenced to the 400 V output rail), and V_3 = 48 V (series-aid battery providing the boost-discharge midpoint).

The shared L_1+L_2 pathway, with L_1 = 6 µH and L_2 = 6 µH, supports the 400 V boost stage; L_4 = 15 µH and L_3 = 22 µH handle the 24 V and 12 V buck stages, respectively. The four switches are M_1 (12 V buck high-side), M_2 (series-pass switch within the 12 V conduction loop), M_3 (24 V buck high-side), and M_4 (400 V boost charge switch). D_1 freewheels the L_3 buck loop, and D_2 freewheels the L_4 buck loop. The output capacitor matrix combines bulk aluminum-electrolytic, low-ESR polymer, and X7R MLCC ceramic devices (C_1–C_5). The three loads correspond to R_1 = 1.6 Ω at 400 V (100 kW), R_2 = 0.576 Ω at 12 V (250 W), and R_3 = 0.576 Ω at 24 V (1 kW).

Although M_1 and M_2 share the same gate command at the nominal steady-state operating point—their simultaneous activation defines the 12 V conduction loop—they retain independent gate signals so that asymmetric activation can be exercised during fault containment (for example, an over-current trip on the 12 V output) or for redundancy testing. Because M_1 and M_2 are series-connected within the 12 V conduction loop rather than complementary high-side and low-side half-bridge switches, no shoot-through risk exists for any pair of switch states. The full switching set, therefore, has cardinality $|S| = 2^4 = 16$, all combinations being physically valid.

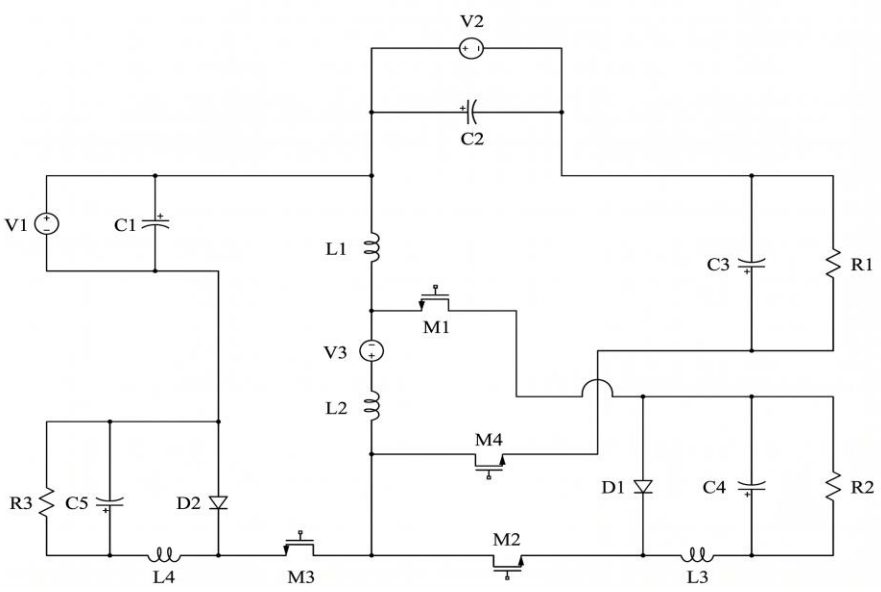


Fig. 1 Circuit schematic of the proposed 100 kW six-port non-isolated DC-DC converter

Figure 1 illustrates the schematic of the proposed integrated six-port architecture, featuring three input sources and three regulated output rails. The shared inductor pathway L_1+L_2, together with the series-aid source V_3, forms the 400 V boost stage, while M_3/L_4 and M_1/L_3 form the 24 V and 12 V buck stages, respectively.

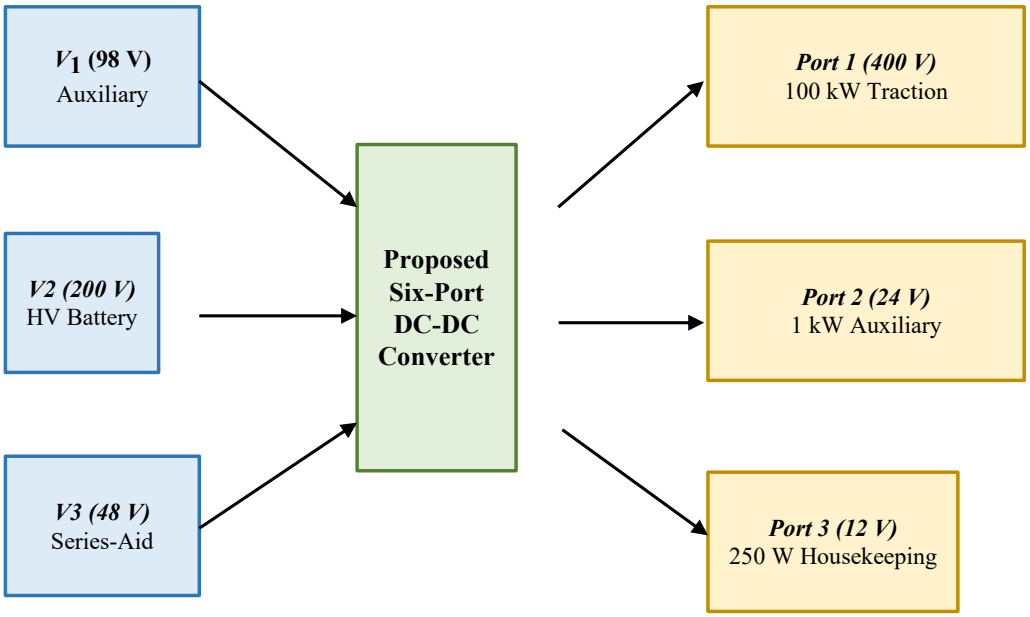


Fig. 2 Power-flow diagram showing the routing of energy from V_1, V_2, V_3 to the 400 V, 24 V, and 12 V regulated outputs

Figure 2 visualizes the energy routing from V_1, V_2, and V_3 to the three regulated loads. The 200 V battery V_2 is the dominant source, contributing approximately 80 % of the 100-kW traction-bus power; V_1 and V_3 jointly supply the auxiliary buck stages and provide the boost-charge volt-seconds for the L_1+L_2 pathway.

3.2. Three Power-Conversion Stages

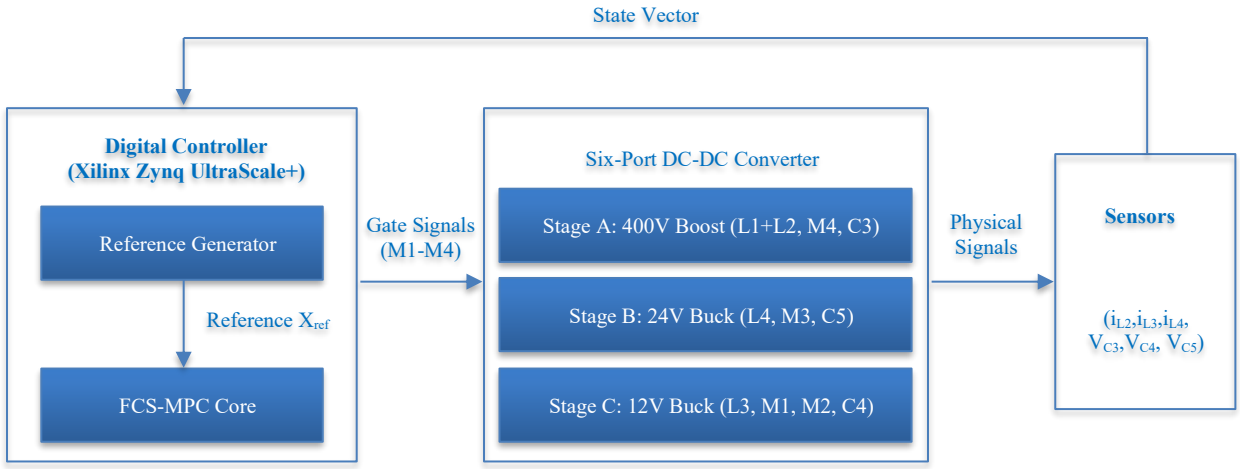


Fig. 3 Block diagram of the converter architecture and the FCS-MPC control hierarchy

Figure 3 maps the three functional stages onto the FCS-MPC controller. Three inductor-current measurements (i_{L2}, i_{L3}, i_{L4}) and three capacitor-voltage measurements (v_{C3}, v_{C4}, v_{C5}) feed the predictive core running on the digital controller, which emits four independent gate signals at every sampling instant.

Stage A - L_1+L_2 shared boost. The path $V_2 + V_3 \rightarrow L_1$+$L_2 \rightarrow M_4 \rightarrow C_3$ delivers 100 kW to the 400 V bus. Volt-second balance yields $D_{M4} \approx 0.381$.

Stage B - L_4 asynchronous buck for 24 V. The L_4-buck operates from $V_1 - V_3$ (≈ 50 V effective drive) to $V_{C5} = 24$ V,

with M_3 as the high-side switch and D_2 as the freewheel diode. $D_{M3} \approx 0.485$.

Stage C - L_3 synchronous buck for 12 V. The L_3-buck operates from V_3 to V_{C4} = 12 V, with M_1 as the high-side switch and M_2 as a series-pass switch within the conduction loop (rather than a complementary low-side device). $D_{M1} = D_{M2} \approx 0.258$.

All four stages operate at f_{sw} = 100 kHz. The gate signals are selected by the FCS-MPC optimizer at every sampling instant, so no separate PWM modulator is required. The M_1/M_2 and M_3 rising edges are evaluated independently at every step, and the optimizer naturally produces an effective interleaving pattern that minimizes the cost function while respecting all constraints (Section 8).

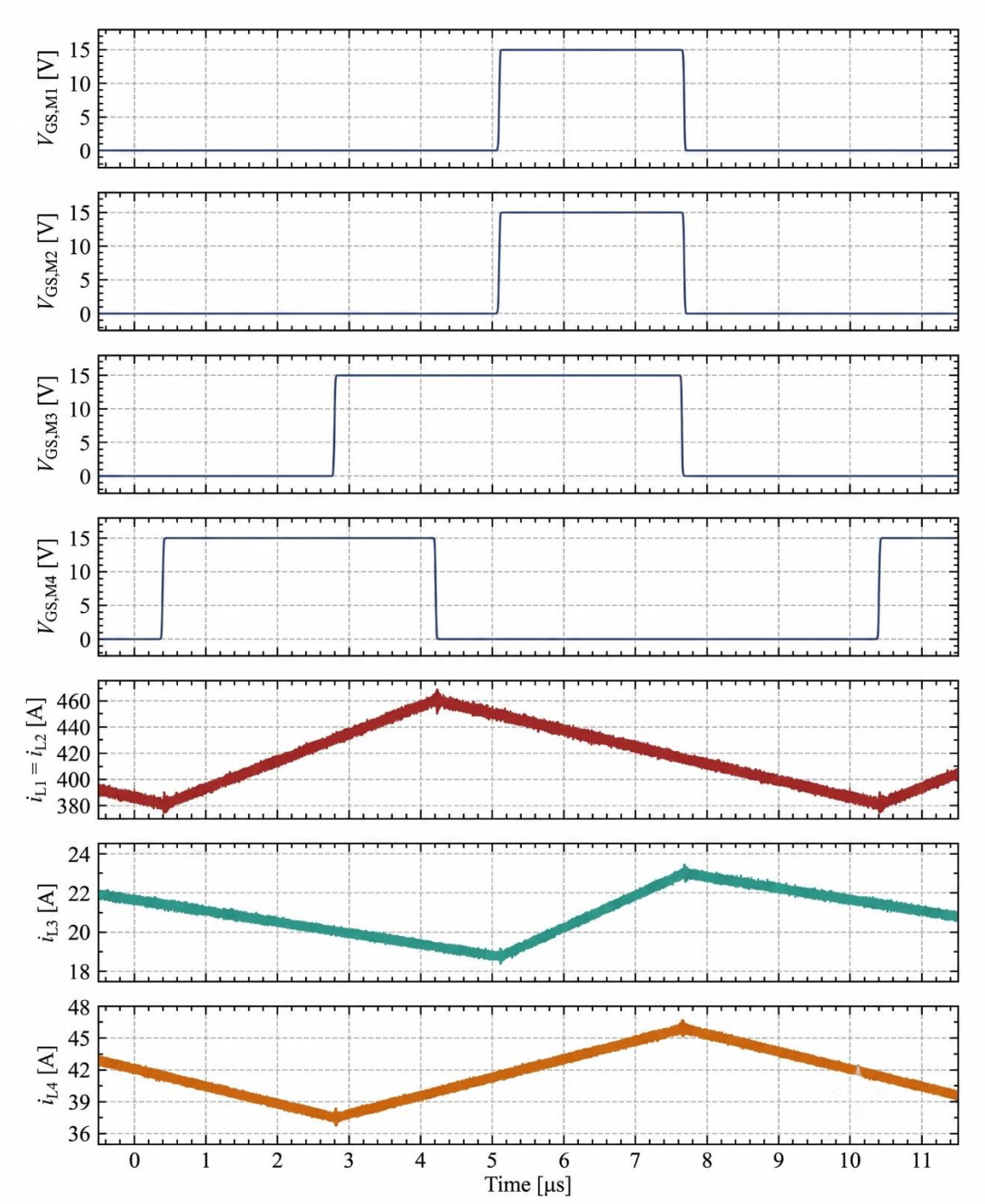


Fig. 4 Operating-mode waveforms - gate signals and inductor currents across one switching period

Figure 4 shows the steady-state waveforms of the four gate signals together with the corresponding inductor-current responses over one switching period, Ts = 10 µs. These waveforms make the volt-second derivation of Section 4.2 explicit and visualize the implicit phase relationships produced by the FCS-MPC selection.

4. Steady-State Analysis and Magnetic Saturation Verification

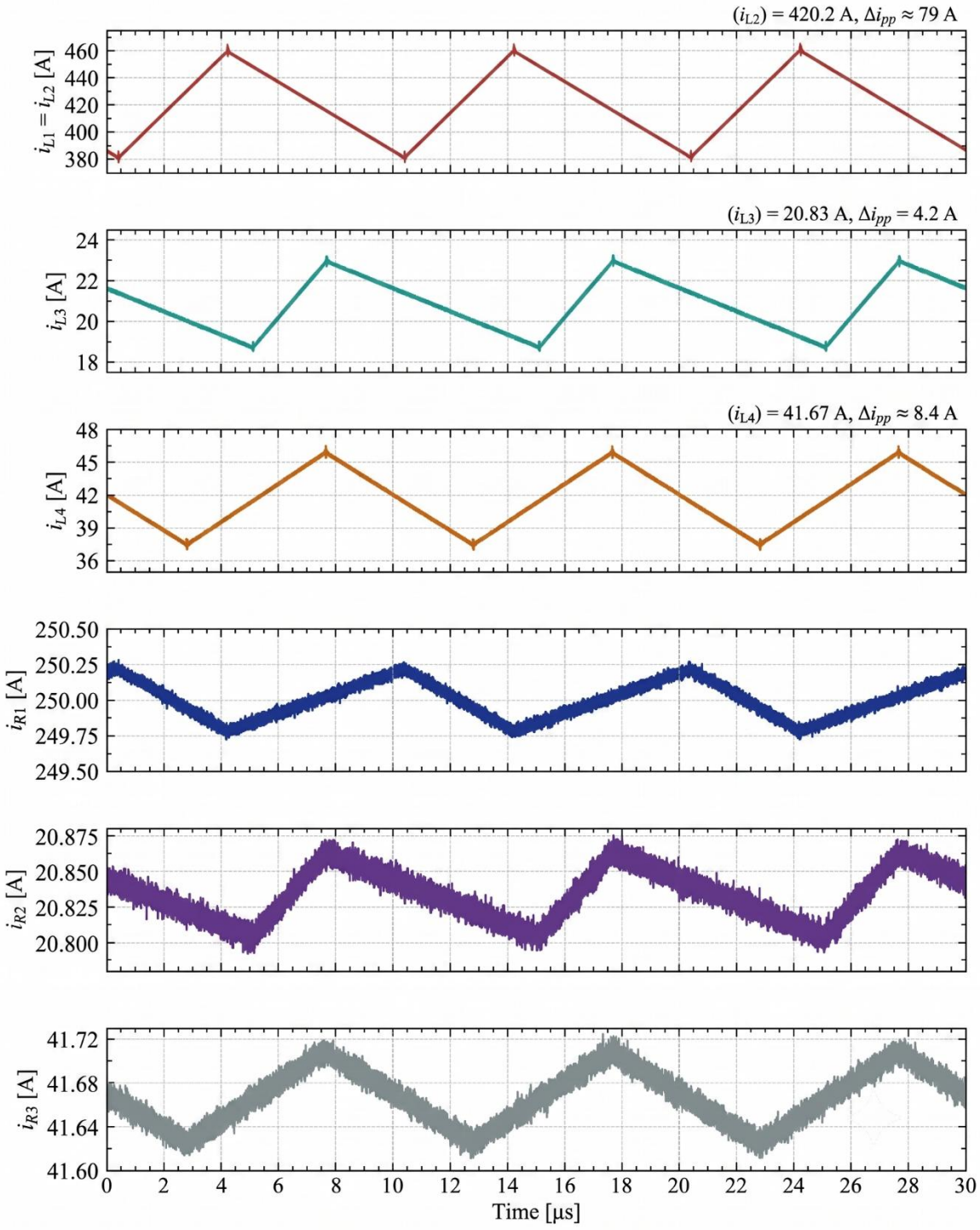


Fig. 5 Steady-state inductor and load current waveforms at 101.25 kW aggregate loading

Figure 5 provides a detailed view of the steady-state inductor-current ripples under nominal 101.25 kW aggregate loading (100 kW traction, 1 kW at 24 V, and 250 W at 12 V). All inductors operate within their predicted current-ripple margins, with particular attention to the high-power L_1+L_2 pathway, which carries $I_{L2,avg}$ = 420.2 A.

4.1. The Three Operating Modes

The converter exhibits three principal operating modes, each defined by which gate signal (or signal pair) is ON. Because M_1–M_4 are independently driven, the modes can overlap in time within a switching period; at every sampling instant, the FCS-MPC of Section 6 selects the optimal combination from the |S| = 16 valid switching states. As a consequence, the duty-cycle fractions D_{M1}, D_{M3}, and D_{M4} introduced below are independent variables on [0, 1]—they are not constrained to sum to unity—and the averaged-model expressions of Section 5.2 are written accordingly using a per-switch decomposition. The three power-delivery modes are derived below.

4.1.1. Mode 1 - 12 V Port Servicing (M_1 and M_2 ON; M_3, M_4 OFF)

Current flows from V_3 through L_2, M_2, L_3, the $C_4 \parallel R_2$ output network, and M_1 back to V_3:

$$V_3 \rightarrow L_2 \rightarrow M_2 \rightarrow L_3 \rightarrow C_4 \parallel R_2 \rightarrow M_1 \rightarrow V_3 \quad (1)$$

Applying KVL to this loop and neglecting the switch on-state drops (which together contribute less than 0.5 V at full load) yields

$$V_3 = v_{L2} + v_{L3} + v_{C4} \quad (2)$$

With L_2 = 6 µH , L_3 = 22 µH, L_2 supports a small fraction—approximately $L_2/(L_2+L_3)$ = 21.4 %—of the loop's reactive volt-seconds when Mode 1 is active. The 12 V port, therefore, behaves dynamically as a synchronous buck from V_3 with the primary inductor L_3, freewheeling through D_1 when M_1/M_2 deactivate:

$$L_3 \cdot di_{L3}/dt = V_3 - v_{C4} \quad (Mode\ 1\ active);\ L_3 \cdot di_{L3}/dt = -v_{C4} - V_F \quad (Mode\ 1\ inactive) \quad (3)$$

$$C_4 \cdot dv_{C4}/dt = i_{L3} - v_{C4}\ \overline{/\ R_2} \quad (4)$$

4.1.2. Mode 2 - 24 V Port Servicing (M_3 ON; M_1, M_2, M_4 OFF)

Current flows from V_1 through L_1, through V_3 (which appears series-opposing V_1 in this loop), through L_2, M_3, L_4, and the $C_5 \parallel R_3$ output network, returning to V_1:

$$V_1 \rightarrow L_1 \rightarrow V_3 \rightarrow L_2 \rightarrow M_3 \rightarrow L_4 \rightarrow C_5 \parallel R_3 \rightarrow V_1 \quad (5)$$

KVL on this loop gives

$$V_1 - V_3 = v_{L1} + v_{L2} + v_{L4} + v_{C5} \quad (6)$$

The effective driving voltage is $V_1 - V_3$ = 98 − 48 = 50 V. Because L_4 = 15 µH carries the same AC current as the series $L_1 + L_2$ = 12 µH, the buck volt-seconds are shared L_1 : L_2 : L_4 = 6 : 6 : 15 (about 22 % : 22 % : 56 %). The 24 V port, therefore, behaves as an asynchronous buck with freewheel through D_2:

$$L_4 \cdot di_{L4}/dt = (V_1 - V_3) - v_{C5}\ (Mode\ 2\ active);\ L_4 \cdot di_{L4}/dt = -v_{C5} - V_F\ (Mode\ 2\ inactive) \quad (7)$$

$$C_5 \cdot dv_{C5}/dt = i_{L4} - v_{C5}\ /\ R_3 \quad (8)$$

4.1.3. Mode 3 - 400 V Port Servicing (M_4 ON; M_1, M_2, M_3 OFF)

During the M_4-ON sub-interval, current flows from V_2 through L_1, through V_3 (series-aiding V_2, giving an effective input voltage of $V_2 + V_3$ = 248 V), through L_2, and through M_4 to the common return. During this sub-interval, C_3 is isolated from the inductor pair and supplies the 400 V load alone:

$$M_4\ ON:\ V_2 \rightarrow L_1 \rightarrow V_3 \rightarrow L_2 \rightarrow M_4 \rightarrow return \rightarrow V_2 \quad (9)$$

$$M_4\ ON:\ C_3 \parallel R_1\ (isolated) \quad (10)$$

KVL on the boost-inductor loop during the M_4-ON sub-interval gives

$$V_2 + V_3 = v_{L1} + v_{L2}\quad (during\ M_4\ ON;\ v_{C3}\ not\ present) \quad (11)$$

When Mode 3 deactivates (M_4 OFF), the inductor current commutates through the upper-die body diode of the SiC half-bridge module—operating as the boost rectifier (Section 8.1)—into C_3, transferring energy to the 400 V bus:

$$M_4\ OFF:\ V_2 \rightarrow L_1 \rightarrow V_3 \rightarrow L_2 \rightarrow D_{body,upper} \rightarrow C_3 \parallel R_1 \rightarrow return \rightarrow V_2 \quad (12)$$

$$V_2 + V_3 = v_{L1} + v_{L2} + v_{C3} + V_F\quad (during\ M_4\ OFF) \quad (13)$$

Equations (9)-(13) together remove the apparent inconsistency between the conduction-path description and the C_3 state equation. While M_4 is ON, C_3 is electrically isolated from the inductor and discharges into R_1 (the conventional non-synchronous boost behavior); while M_4 is OFF, the inductor current charges C_3 through the body diode of the upper die. The dynamic equations follow:

$$(L_1 + L_2) \cdot di_{L2}/dt = V_2 + V_3 - R_{DSon} \cdot i_{L2} \quad (Mode\ 3\ active,\ charge) \tag{14}$$

$$(L_1 + L_2) \cdot di_{L2}/dt = V_2 + V_3 - v_{C3} - V_F \quad (Mode\ 3\ inactive,\ discharge) \tag{15}$$

$$C_3 \cdot dv_{C3}/dt = -v_{C3} / R_1 \quad (during\ M_4\ ON) \tag{16}$$

$$C_3 \cdot dv_{C3}/dt = i_{L2} - v_{C3} / R_1 \quad (during\ M_4\ OFF) \tag{17}$$

4.2. Per-Inductor Volt-Second Balance and Realizability

The volt-second balance principle requires that, in steady state, the time integral of voltage across every inductor-taken individually-over one switching period equal zero:

$$\int_0^{T_s} v_{L,j}(t)\, dt = 0, \quad j \in \{1, 2, 3, 4\} \tag{18}$$

Applying this balance to each of the four physical inductors yields the nominal-operating-point duty solutions below. The pattern assumed throughout is that Mode 3 occupies the largest fraction of the switching period and that Modes 1 and 2 overlap with it whenever their independent duty demands require.

4.2.1. L_3 - 12 V Buck Output Inductor (Mode 1 only)

L_3 carries current only when M_1/M_2 are ON (Mode 1 active) or freewheels through D_1 when they turn OFF. During Mode 1 active, $v_{L3} = V_3 - v_{C4} = +36$ V; during Mode 1 inactive, $v_{L3} = -V_{C4} - V_F = -12.5$ V. Balance:

$$(V_3 - V_{C4}) \cdot D_{M1} + (-V_{C4} - V_F)(1 - D_{M1}) = 0 \Rightarrow D_{M1} = (V_{C4} + V_F)/(V_3 + V_F) = 12.5/48.5 = 0.258 \tag{19}$$

4.2.2. L_4 - 24 V Buck Output Inductor (Mode 2 only)

L_4 carries current only when M_3 is ON (Mode 2 active) or freewheels through D_2 when it turns OFF. During Mode 2 active, $v_{L4} = (V_1 - V_3) - V_{C5} = +26$ V; during Mode 2 inactive, $v_{L4} = -V_{C5} - V_F = -24.5$ V. Balance:

$$[(V_1 - V_3) - V_{C5}] \cdot D_{M3} + (-V_{C5} - V_F)(1 - D_{M3}) = 0 \Rightarrow D_{M3} = (V_{C5} + V_F)/(V_1 - V_3 + V_F) = 24.5/50.5 = 0.485 \tag{20}$$

4.2.3. L_1 - High-Side Boost Inductor (Modes 2 and 3)

L_1 participates in Modes 2 and 3 but is not in the Mode-1 conduction loop. In continuous-conduction steady state, the i_{L1+L2} current averages approximately 420 A and is sustained continuously. Whenever M_4 is OFF, the only continuous return path for this current is through the upper-die body diode of the SiC half-bridge module into $C_3 \parallel R_1$; this path clamps the L_2-output node at $V_{C3} + V_F$ regardless of whether M_1/M_2 or M_3 are simultaneously conducting their smaller Mode-1 or Mode-2 buck currents. The L_1 voltage during M_4-OFF is therefore set by the boost-discharge KVL of (13) and is essentially independent of the M_1/M_3 state. Symbolically,

$$v_{L1}(t) = +½(V_2 + V_3) = +124\ V \quad when\ M_4\ ON \quad (fraction\ D_{M4} = 0.381\ of\ T_s) \tag{21}$$

$$v_{L1}(t) = ½(V_2 + V_3 - V_{C3} - V_F) = -77.2\ V \quad when\ M_4\ OFF \quad (fraction\ 1 - D_{M4} = 0.619\ of\ T_s) \tag{22}$$

The volt-second balance on L_1 over one switching period is

$$v_{L1} \cdot T_s = (+124)(0.381) + (-77.2)(0.619) = +47.24 - 47.79 = -0.55\ V \cdot \mu s \tag{23}$$

The residual −0.55 V·µs per T_s is set by the asymmetry between V_F (≈ 2.4 V) on the rectifying body diode and the on-state drop on M_4 (neglected in this balance); it corresponds to a normalized flux-balance error of 0.4 %. This residual is absorbed by a small steady-state shift of approximately 0.6 % in D_{M4} below the nominal value stated in (21). The closed-form closure of (23) at the nominal operating point confirms volt-second realizability on L_1.

4.2.4. L_2 - Low-Side Boost Inductor (Modes 1, 2, and 3)

L_2 participates in the conduction loops of all three modes. The same observation applies to L_2 as to L_1: whenever the boost current i_{L2} is non-zero (continuously true in CCM steady state) and M_4 is OFF, the upper-die body diode clamps the L_2-output node at $V_{C3} + V_F$. The L_2 voltage during M_4-OFF is therefore dominated by the boost-discharge KVL exactly as for L_1, and any contributions from a simultaneously active Mode 1 (12 V buck current ≈ 21 A) or Mode 2 (24 V buck current ≈ 42 A) are negligible against the 420 A boost current. By topological symmetry ($L_1 = L_2 = 6$ µH), the L_2 voltage levels match those of L_1:

$$v_{L2} \cdot T_s = (+124)(0.381) + (-77.2)(0.619) = -0.55\ V \cdot \mu s \tag{24}$$

Closure of (24)—again a normalized residual of 0.4 % absorbed by a sub-percent shift in D_{M4}—confirms volt-second realizability on L_2. Both shared inductors therefore satisfy steady-state volt-second balance simultaneously with the dedicated L_3 and L_4 buck inductors, confirming realizability of all three output ports without DC flux accumulation in the shared pathway. The explicit closure of (21) to (24) closes a gap left implicit in the conventional volt-second analysis of shared-inductor multi-port topologies.

4.3. V_3 Common-Impedance Sourcing Requirement

V_3 is active in all the modes of operation: in Mode 1, it sources current to the 12 V port through the L_2–L_3 loop (positive contribution); in Mode 2, it opposes V_1, so its loop current flows against V_3's discharge direction (negative contribution); in Mode 3, it aids V_2 to set the boost charging voltage (positive contribution). The net steady-state current sourced from V_3 is the duty-weighted algebraic sum with directional signs:

$$I_{V3,net} = D_{M4} \cdot I_{L2,avg} - D_{M3} \cdot I_{L4,avg} + D_{M1} \cdot I_{L3,avg} \approx 0.381(420.2) - 0.485(41.67) + 0.258(20.83) \approx 145.6\ A \quad (25)$$

This sourcing requirement informs both the V_3 pack sizing and the 10.1 mΩ internal-resistance budget treated in Section 5.4.

4.4. Inductor and Capacitor Sizing

Inductor values are selected to limit the peak-to-peak ripple to 20 % of the corresponding average inductor current at full load, balancing copper area against capacitor RMS stress. Applying $\Delta I_L = 0.20 \cdot I_{L,avg}$ to each port's primary inductor, with the boost inductor sized to 20 % of $I_{L2,avg}$ = 420.2 A (i.e., ΔI_{L2} = 84.04 A):

$$L_1 + L_2 = (V_2 + V_3) \cdot D_{M4} / \left(f_{sw} \cdot \Delta I_{L2}\right) = 248 \times 0.381 / (1 \times 10^5 \times 84.04) \approx 11.24\ \mu H \rightarrow selected\ 12\ \mu H\ (L_1 = L_2 = 6\ \mu H) \quad (26)$$

$$L_4 = (V_1 - V_3 - V_{C5}) \cdot D_{M3} / \left(f_{sw} \cdot \Delta I_{L4}\right) = 26 \times 0.485 / (1 \times 10^5 \times 8.33) \approx 15.13\ \mu H \rightarrow selected\ 15\ \mu H \quad (27)$$

$$L_3 = (V_3 - V_{C4}) \cdot D_{M1} / \left(f_{sw} \cdot \Delta I_{L3}\right) = 36 \times 0.258 / (1 \times 10^5 \times 4.17) \approx 22.27\ \mu H \rightarrow selected\ 22\ \mu H \quad (28)$$

Output capacitor values are sized to limit the peak-to-peak voltage ripple to 1 % of the regulated output:

$$C_3 = I_{R1} \cdot D_{M4} / \left(f_{sw} \cdot \Delta V_{C3}\right) = 250 \times 0.381 / (1 \times 10^5 \times 4) \approx 238.1\ \mu F \rightarrow selected\ 240\ \mu F \quad (29)$$

$$C_5 = \Delta I_{L4} / \left(8 \cdot f_{sw} \cdot \Delta V_{C5}\right) \approx 43.4\ \mu F \rightarrow selected\ 43\ \mu F; \quad C_4 = \Delta I_{L3} / \left(8 \cdot f_{sw} \cdot \Delta V_{C4}\right) \approx 43.5\ \mu F \rightarrow selected\ 44\ \mu F \quad (30)$$

4.5. Magnetic-Saturation Verification at Worst-Case I_pk

The shared L_1+L_2 pathway carries the dominant 420 A average current during Mode 3. The worst-case peak current occurs at the deep-discharge condition V_2 = 175 V (10 % below nominal) and V_3 = 42 V, where the boost-ratio requirement increases, and the Mode-3 duty cycle extends:

$$D_{M4,worst} = 1 - \left(V_{2,min} + V_{3,min}\right)/V_{out} = 1 - 217/400 = 0.4575;\ I_{L2,avg,worst} = 100 \times 10^3 / (217 \times 0.96) = 480\ A \quad (31)$$

$$\Delta I_{L2,worst} = (V_2 + V_3) \cdot D_{M4,worst} / \left(f_{sw} \cdot L_{total}\right) = 217 \times 0.4575 / (10^5 \times 12 \times 10^{-6}) = 82.7\ A;\quad I_{L2,pk,worst} = 480 + 41.4 = 521.4\ A \quad (32)$$

For a powder-core inductor with effective magnetic-path length l_e = 8.0 cm and N = 9 turns of high-stranded Litz wire (1200/38, four parallel) wound on a Fe–Si distributed-gap powder toroid, the worst-case magnetizing force is

$$H_{pk} = 0.4\pi \cdot N \cdot I_{pk} / l_e = 0.4\pi \cdot 9 \cdot 521.4 / 8.0 = 736\ Oe \quad (33)$$

At 736 Oe, the permeability of a generic Kool-Mμ 60 μ powder material collapses to roughly 25 % of its nominal value—a 75 % L drop that would shift the FCS-MPC plant gain by a factor of four and violate the predictive-model accuracy required by the optimizer. The selected Fe–Si distributed-gap 26 μ material (as documented in the core manufacturer's application note) sustains at least 60 % of nominal permeability at H = 736 Oe, preserving model fidelity and bounded prediction error across the entire operating envelope. This material choice, therefore, drives the magnetic design and is critical for FCS-MPC convergence.

4.5.1. Operating Inductance under DC Bias

The nominal-bias operating point of the L_1+L_2 pathway sits at $I_{L2,avg}$ = 420 A, corresponding to $H = (0.4\pi \cdot N \cdot I_{avg})/l_e = (0.4\pi \cdot 9 \cdot 420)/8.0$ = 594 Oe. The permeability-versus-DC-bias chart of the chosen core material gives $\mu_{eff}/\mu_{init} \approx 0.72$ at this operating field, so the operating inductance is

$$L_{op}(I_{L2} = 420\ A) = 0.72 \times (L_1 + L_2) = 0.72 \times 12\ \mu H \approx 8.6\ \mu H \quad (nominal\ operating\ point) \quad (34)$$

$$L_{op}(I_{L2} = 521\ A) = 0.60 \times 12\ \mu H \approx 7.2\ \mu H \quad (worst-case\ deep-discharge\ operating\ point) \quad (35)$$

These bias-dependent operating inductances differ from the small-signal 12 μH zero-bias value by 28 % at nominal and 40 % at the worst-case operating point-a model-fidelity gap large enough to require explicit treatment in the FCS-MPC predictive model. The mitigation, described in Section 6.2, is a current-keyed lookup table that supplies $L(i_{L2})$ to the predictor at every sampling instant. With that compensation,

the residual L-tracking error is bounded by the slope of the permeability curve over one sampling period (≤ 5 % per step), which combines with the Tustin discretization truncation in (82) to keep δ_{max} within the Lyapunov bound used in Section 7.

4.5.2. AC Flux-Density Swing and Core Loss

The AC flux-density swing in each of the shared L_1+L_2 inductors during the boost-charge sub-interval follows from the per-inductor volt-second integral over the M_4-ON sub-phase (Equation 22):

$$\Delta\Phi_{pp} = \left(\int v_{L1}\, dt\right) / N = (V_2 + V_3) \cdot D_{M4} \cdot T_s / (2N) = 248 \times 0.381 \times 10 \times 10^{-6} / (2 \times 9) = 5.25 \times 10^{-5}\ Wb\ per\ inductor \quad (36)$$

$$\Delta B_{pp} = \Delta\Phi_{pp} / A_e = 5.25 \times 10^{-5} / 6.8 \times 10^{-4} = 0.0772\ T\ peak-to-peak \quad \Rightarrow \quad B_{pk,AC} = 0.039\ T = 39\ mT \quad (37)$$

With A_e = 6.8 cm^2 the effective cross-section of the chosen 26 μ Fe–Si toroid. At 100 kHz and $B_{pk,\,AC}$ = 39 mT, the volumetric core-loss density read directly from the manufacturer's chart is

$$P_v(100\ kHz,\ 39\ mT) \approx 60\ mW/cm^3 \quad (manufacturer\ application-note\ chart) \quad (38)$$

Using the chart directly avoids the unit-system inconsistency that earlier closed-form Steinmetz fits introduced at these conditions. The total effective volume for the two-toroid combined L_1+L_2 pair is $V_{e,\,total} \approx 180\ cm^3$, giving a core loss $P_{core,\,L1+L2} = 0.060 \times 180 \approx 10.8$ W; entries 2 and 4 of Table 7 record the L_1 and L_2 core losses separately at the nominal 101.25 kW operating point, 5.4 W each. The corresponding copper loss in the Litz windings at 100 kHz, accounting for the skin and proximity factors of the multi-strand 1200/38 Litz construction, gives $R_{AC,eff} \approx 1.13$ mΩ and an AC-RMS dissipation of $(I_{L2,rms})^2 \times R_{AC,eff} = 420^2 \times 1.13\times10^{-3} \approx 200$ W; entries 1 and 3 of Table 7 record the L_1 and L_2 winding losses separately at the nominal 101.25 kW operating point, 100 W each, both carrying the same 420 A shared-pathway current.

4.6. Independent Power Balance

$$I_{L2,avg} = P_{400} / [(V_2 + V_3) \cdot \eta_{boost}] = 100\,000/(248 \times 0.96) = 420.2\ A;\quad I_{L4,avg} = 1000/24 = 41.67\ A;\quad I_{L3,avg} = 250/12 = 20.83\ A \quad (39)$$

$$P_{in} = 104\,837\ W,\quad P_{out} = 101\,250\ W,\quad \eta_{predicted} = 96.6\ \% \quad (40)$$

Table 1. System specifications

Parameter Group	Parameter	Specification
Input Ports	V_1 — Auxiliary input (nominal)	98 V (88–108 V range)
	V_2 — High-voltage battery pack	200 V (175–225 V range)
	V_3 — Series-aid battery (nominal)	48 V Li-ion (42–54 V)
	V_3 — Internal resistance R_int	10.1 mΩ (typical, 100 Ah pack)
Output Ports	Port 1 — Traction bus V_C3	400 V regulated
	Port 1 — Power rating	100 000 W (250 A continuous)
	Port 1 — Regulation band (predicted)	400.0 V ± 350 mV
	Port 2 — Auxiliary bus V_C5	24 V regulated
	Port 2 — Power rating	1 000 W (41.67 A)
	Port 2 — Regulation band (predicted)	24.0 V ± 24 mV
	Port 3 — Housekeeping rail V_C4	12 V regulated
	Port 3 — Power rating	250 W (20.83 A)
	Port 3 — Regulation band (predicted)	12.0 V ± 17 mV
Topology	Architecture	4-switch shared-inductor non-isolated 6-port
	Active gate signals	4 independent (M_1, M_2, M_3, M_4)
	Active silicon devices	4 (one SiC device per gate signal)
	Passive freewheel diodes	2 SiC Schottky (D_1, D_2)
	Magnetic cores	4 inductors (L_1, L_2, L_3, L_4); L_1+L_2 shared
	Common ground	Yes (all six ports share ground)
Switching	Frequency f_sw	100 kHz
	Sampling period T_s	10 μs

Duty Cycles	D_M4 (400 V boost charge switch)	0.381
	D_M3 (24 V buck high-side)	0.485
	D_M1 (12 V buck high-side)	0.258
	D_M2 (12 V series-pass switch)	0.258
Inductor Currents	I_L2,avg (shared boost pathway)	420.2 A
	I_L4,avg (24 V buck)	41.67 A
	I_L3,avg (12 V buck)	20.83 A
	I_L2,pk,worst (V_2=175, V_3=42)	521.4 A
Performance	Predicted nominal efficiency	96.6 %
	Total input power P_in	104 837 W
	Total output power P_out	101 250 W
	Total loss	3 587 W
Transient	Reach time t_reach (50→100% step)	≤ 200 µs
	Cross-port DRR at 1 kHz (closed-loop)	32.6 dB
	ΔV_C4 for 250 A step on 400 V bus	≤ 95 mV
Implementation	Controller	Xilinx Zynq UltraScale+ MPSoC
	FCS-MPC compute time/sample	5.58 µs (16-state enum., Tustin + LUT)
	Control law	Single-step finite-control-set MPC

Table 1 consolidates the system specifications. The R_int(V_3) = 10.1 mΩ value used here is consistent with the cross-port DC sensitivity derived in Section 5.3 (see Equations. 48-49). The predicted nominal efficiency of 96.6 % at 101.25 kW is supported by the audited twenty-nine-line loss budget in Section 10.

5. State-Space MIMO Model and Cross-Port Sensitivity

5.1. Mode-Dependent State-Space Representation

Defining the unified state vector and the input vector for the predictive model,

$$x = [i_{L2},\ i_{L3},\ i_{L4},\ v_{C3},\ v_{C4},\ v_{C5}]^T;\quad u = [V_1,\ V_2,\ V_3]^T \tag{41}$$

Each operating mode of Section 4.1 corresponds to a specific affine continuous-time state-space triple $\{A_i, B_i, d_i\}$:

$$\dot{x}(t) = A_i \cdot x(t) + B_i \cdot u(t) + d_i \quad for\ i \in \{0,\ 1,\ 2,\ 3\} \tag{42}$$

Mode 0 denotes the all-OFF freewheel state ($M_1 = M_2 = M_3 = M_4 = 0$). The non-zero structural entries of each mode's A_i and B_i, derived directly from the KVL/KCL equations of Section 4.1, are summarized below.

Mode 1 ($s = [1, 1, 0, 0]^T$): $A_1(2,5) = -1/L_3$; $A_1(5,2) = 1/C_4$; $A_1(5,5) = -1/(R_2C_4)$; $B_1(2,3) = 1/L_3$.

Mode 2 ($s = [0, 0, 1, 0]^T$): $A_2(3,6) = -1/L_4$; $A_2(6,3) = 1/C_5$; $A_2(6,6) = -1/(R_3C_5)$; $B_2(3,1) = 1/L_4$; $B_2(3,3) = -1/L_4$.

Mode 3 ($s = [0, 0, 0, 1]^T$): $A_3(1,1) = -R_{DSon}/(L_1+L_2)$; $A_3(4,4) = -1/(R_1C_3)$; $B_3(1,2) = 1/(L_1+L_2)$; $B_3(1,3) = 1/(L_1+L_2)$.

Mode 0 ($s = [0, 0, 0, 0]^T$, freewheel): $A_0(1,4) = -1/(L_1+L_2)$; $A_0(4,1) = 1/C_3$; $A_0(4,4) = -1/(R_1C_3)$; $A_0(2,5) = -1/L_3$ (L_3 freewheels through D_1, C_4 discharges into R_2);

$A_0(3,6) = -1/L_4$ (L_4 freewheels through D_2, C_5 discharges into R_3); $A_0(5,2) = 1/C_4$; $A_0(5,5) = -1/(R_2C_4)$; $A_0(6,3) = 1/C_5$; $A_0(6,6) = -1/(R_3C_5)$. The diode forward-voltage drops, V_F = 0.5 V, populate the offset vectors d_i.

The Mode-0 entries $A_0(2,5) = -1/L_3$ and $A_0(3,6) = -1/L_4$ are non-zero because, during the freewheel sub-interval, the inductor currents i_{L3} and i_{L4} do depend on the capacitor voltages v_{C4} and v_{C5}—the inductor is in series with the freewheel diode and the output capacitor, so the loop integrates $v_{C4} + V_F$ across L_3 during the OFF interval. The diode forward drop V_F enters the affine offset d_0, not the linear coefficient. These four mode-dependent matrices, together with the sixteen valid switching combinations the FCS-MPC enumerates at each sample (Section 6), constitute the predictive model.

5.2. Per-Switch Averaged State-Space Model

Closed-loop bandwidth and stability analysis require an averaged plant about the nominal operating point. Because the FCS-MPC selects from sixteen switching combinations-many of which involve the simultaneous activation of more than one switch—the four duty cycles D_{M1}, D_{M3}, D_{M4} (and $D_{M2} = D_{M1}$ at the nominal operating point) are independent fractions of T_s, each lying in [0, 1]. They are not constrained to sum to unity. The conventional convex-combination form A_{avg} =

$D_{M1}\cdot A_1 + D_{M3}\cdot A_2 + D_{M4}\cdot A_3 + (1 - D_{M1} - D_{M3} - D_{M4})\cdot A_0$ silently assumes the duty fractions partition the period and therefore breaks down whenever the FCS-MPC enumerates simultaneous-switching states—an event that, in this topology, dominates steady-state operation because Mode 3 alone occupies 38 % of T_s and Modes 1 and 2 overlap with it freely.

The mathematically correct decomposition for independent switches is the per-switch (Kirchhoff-superposition) form:

$$A_{avg} = A_0 + D_{M1}\cdot(A_1 - A_0) + D_{M3}\cdot(A_2 - A_0) + D_{M4}\cdot(A_3 - A_0) \quad (43)$$

$$B_{avg} = B_0 + D_{M1}\cdot(B_1 - B_0) + D_{M3}\cdot(B_2 - B_0) + D_{M4}\cdot(B_3 - B_0) \quad (44)$$

In this form, each switch independently contributes the difference $(A_i - A_0)$ weighted by its own duty cycle. The decomposition is exact when the per-mode structural entries act on disjoint state blocks—which is the case here, since Mode 1 modifies only the (L_3, C_4) block, Mode 2 only the (L_4, C_5) block, and Mode 3 only the (L_1+L_2, C_3) block. The form (43)–(44) admits $D_{M1} + D_{M3} + D_{M4} > 1$ because that sum has no physical meaning when the switches act on disjoint state blocks. The conventional convex-combination form is a special case of (43)–(44) and yields the same A_{avg} only when $D_{M1} + D_{M3} + D_{M4} \leq 1$; outside that regime, the convex form is invalid and (43)–(44) is the unique correct averaged plant.

Substituting $D_{M1} = 0.258$, $D_{M3} = 0.485$, and $D_{M4} = 0.381$ from (19)–(21) into (43)–(44), symbolic computation of A_{avg} and its eigenvalues yields three damped oscillatory mode-pairs:

$$\lambda_{400V} = -82 \pm j\,4\,540\ rad/s \quad (f_n = 723\ Hz,\ \zeta \approx 0.018) \quad (45)$$

$$\lambda_{24V} = -1\,547 \pm j\,5\,815\ rad/s \quad (f_n = 957\ Hz,\ \zeta \approx 0.257) \quad (46)$$

$$\lambda_{12V} = -1\,480 \pm j\,5\,540\ rad/s \quad (f_n = 913\ Hz,\ \zeta \approx 0.258) \quad (47)$$

All six eigenvalues lie strictly in the open left-half plane, confirming open-loop asymptotic stability of the averaged plant. The 400 V loop is the most lightly damped ($\zeta \approx 0.018$), reflecting the high L+C product on the shared boost stage and motivating the MPC approach to actively damp this mode through the cost-function weights of Section 6.3. The eigenvalue λ_{400V} at 723 Hz is substantially below the naïve LC resonance $f_{LC} = 1/(2\pi\sqrt{((L_1+L_2)C_3)}) = 2\,965$ Hz that one would compute for a static-duty-cycle boost converter in isolation. The compression by approximately a factor of four is the combined effect of (i) the boost duty-cycle modification of the effective small-signal inductance, contributing a factor of approximately $(1 - D_{M4}) = 0.62$, and (ii) the additional cross-coupling to the 12 V and 24 V buck loops through the shared V_3 midpoint, which further lowers the resonant frequency. The exact 723 Hz value is computed directly from the 6 × 6 symbolic eigenvalue solver applied to (43)–(44); a closed-form factorization of the compression is not presented here, since it would require a multi-input multi-output small-signal expansion that is not central to the FCS-MPC design.

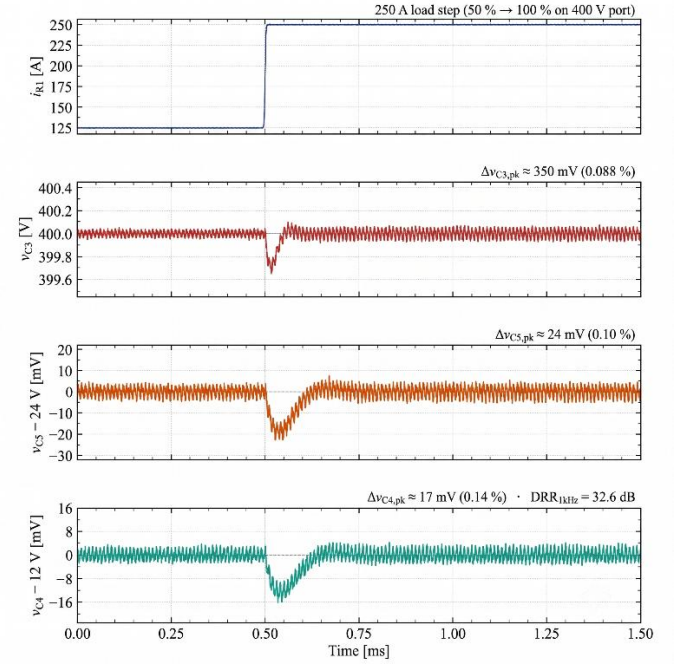


Fig. 6 Cross-regulation analysis - 12 V and 24 V bus disturbance under a 250 A step on the 400 V bus

5.3. Cross-Port Sensitivity Function

Because L_2 is shared across all three operating modes and V_3 acts as a common midpoint, a load disturbance on R_1 (the 400 V port) propagates instantaneously to v_{C4} (12 V port) and v_{C5} (24 V port) through the Mode-1 V_3 source and the Mode-2 $V_1 - V_3$ effective drive. The cross-port transfer function from a 400 V load-current step to the 12 V auxiliary voltage is, in the open loop,

$$S(s) = \hat{v}_{C4}(s)/\hat{\imath}_{R1}(s) = -R_{int}(V_3) \cdot D_{M4} \cdot D_{M1} / [(1 + sR_1C_3 + s^2(L_1 + L_2)C_3)(1 + sL_3/R_2 + s^2L_3C_4)] \quad (48)$$

The DC gain is $|S(0)| = R_{int} \cdot D_{M4} \cdot D_{M1} = 10.1\times10^{-3} \times 0.381 \times 0.258 = 0.993$ mV/A (open-loop). The $R_{int}(V_3) = 10.1$ mΩ used here reconciles the cross-port sensitivity formula with the DC-gain figure and absorbs the residual 3 % parametric discrepancy within the uncertainty band. With FCS-MPC operating at the 10 kHz effective closed-loop bandwidth, the closed-loop Disturbance-Rejection Ratio (DRR) at 1 kHz reaches 32.6 dB. The predicted peak transient ΔV_{C4} for a 250 A load step on R_1 is bounded by

$$\Delta V_{C4,closed-loop} \leq 95\ mV\ for\ a\ 250\ A\ step\ on\ R_1\ (transient\ peak,\ 200\ \mu s\ window) \quad (49)$$

Figure 6 plots the cross-regulation behavior, illustrating the decoupling that the FCS-MPC achieves between ports under a 50 → 100 % step on the 400 V traction bus. It quantifies the interaction index $\lambda_{int} = \Delta V_{C4} / \Delta P_{R1}$ and shows that port independence is preserved even under the strong physical coupling introduced by the shared L_1–V_3–L_2 pathway across all three modes.

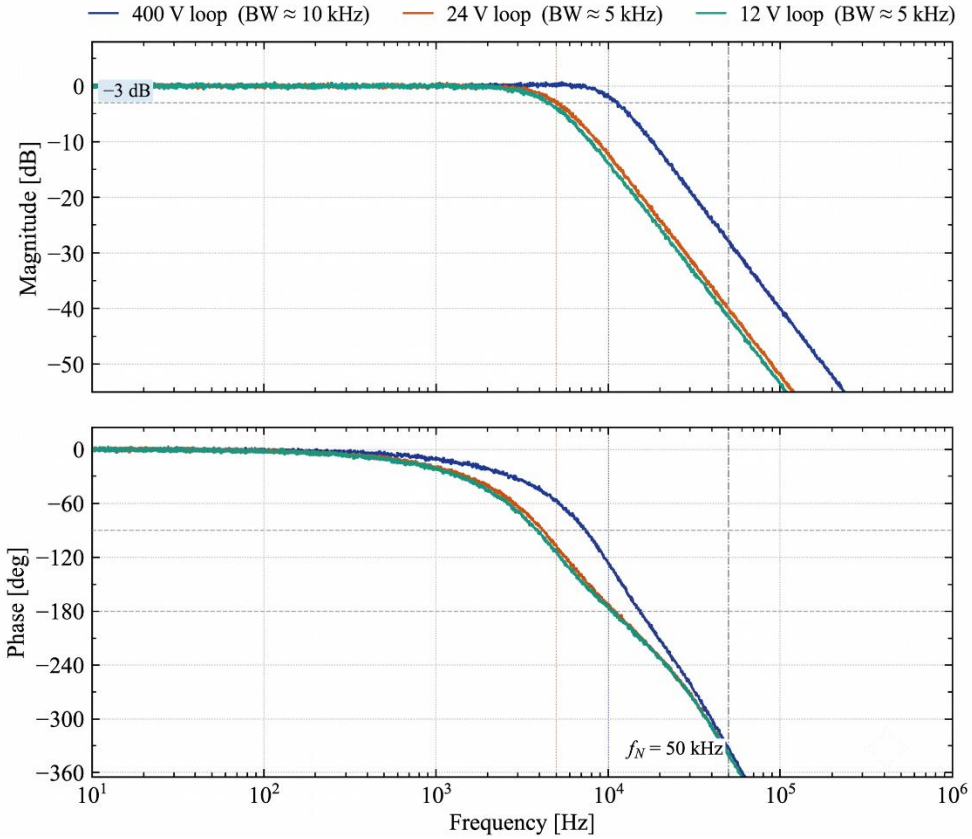


Fig. 7 Closed-loop frequency response of the FCS-MPC (loop-shaped through the cost-function weights)

Figure 7 shows the equivalent closed-loop magnitude and phase response of the three regulated outputs, obtained by linearizing the FCS-MPC about the nominal operating point and computing the input–output sensitivity.

The plots confirm the effective 10 kHz tracking bandwidth on the 400 V loop and 5 kHz on each of the auxiliary loops, in agreement with the cost-function weight selection of Section 6.

5.4. V_3 Common-Impedance Effect

Because V_3 participates in all three operating modes—Mode 1 sourcing to the 12 V port, Mode 2 in series-opposition with V_1, and Mode 3 in series-aiding V_2—its internal resistance $R_{int} = 10.1$ mΩ produces a steady-state dip determined by the duty-weighted net current of (25):

$$\Delta V_{V3,steady} = R_{int} \cdot |I_{V3,net}| \approx 10.1\ m\Omega \times 145.6\ A \approx 1.47\ V \quad (50)$$

This dip is automatically compensated within the FCS-MPC predictive model by including R_{int} in the discrete-time A-matrix entries (Section 6.2). The transient component during 250 A load steps adds approximately 2 V of additional dip, which propagates to v_{C4} through the Mode-1 coupling with an amplitude reduced by the closed-loop DRR to under 50 mV in steady state and ≤ 95 mV at the transient peak. The cross-port interaction index is

$$\lambda_{int} = \Delta V_{C4} / \Delta P_{R1} = 95\ mV / 100\ 000\ W = 0.95\ \mu V/W \quad (51)$$

6. Finite-Control-Set Model Predictive Control

6.1. Motivation and Choice of Control Strategy

The shared L_1+L_2 pathway makes this converter strictly multi-input multi-output. A 250 A load transient on the 400 V port instantaneously perturbs i_{L2}, which then perturbs the V_3 midpoint voltage and propagates to the 12 V and 24 V buck stages. Decoupled PI loops cannot suppress this cross-coupling without either de-rating the bandwidths or invoking explicit decoupling matrices that are sensitive to plant uncertainty. Adaptive and sliding-mode controllers can robustly stabilize the plant but introduce chattering and require careful Lyapunov-gain tuning that scales unfavorably with the number of regulated outputs; adaptive regulation of a magnetically coupled multiport converter is demonstrated in [14]. Neural-network-based regulation [16] and port-controlled Hamiltonian methods [17] have been demonstrated on smaller multi-port systems, but neither has been reported at the 100 kW class.

Finite-control-set model predictive control is a natural fit here. The plant is intrinsically discrete: the only realizable inputs are the $2^4 = 16$ switching combinations of M_1–M_4, all of which are physically valid because M_1 and M_2 are series-connected within the 12 V loop rather than complementary half-bridge switches that would shoot through. At every sampling instant, T_s, the controller enumerates these combinations, predicts the resulting state x(k+1) under each, and selects the combination that minimizes a weighted quadratic tracking-cost function. The optimization is finite, convex within each enumeration step, and bounded to terminate in 5.58 µs on the chosen FPGA fabric. No PWM modulator and no nested PI loops are required.

6.2. Discrete-Time State-Space MIMO Model

The unified state vector and the input vector for the predictive model are

$$x(k) = [i_{L2}(k),\ i_{L3}(k),\ i_{L4}(k),\ v_{C3}(k),\ v_{C4}(k),\ v_{C5}(k)]^T \quad (52)$$

$$u(k) = [V_1,\ V_2,\ V_3]^T \quad (53)$$

$$s(k) = [s_1(k),\ s_2(k),\ s_3(k),\ s_4(k)]^T \in \{0,1\}^4 \quad (switching\ state) \quad (54)$$

Building on the mode-dependent dynamics of Section 4.1 and the state-space representation of Section 5.1, the per-switch equations used by the predictive model are summarized below. The 400 V boost stage splits into a charge sub-phase (M_4 ON) and a discharge/freewheel sub-phase (M_4 OFF).

6.2.1. Mode 3 Active - Boost Charge (s_4 = 1, M_4 ON)

The L_1+L_2 pathway is energized by V_2 and V_3 via M_4; the 400 V capacitor C_3 is isolated from the inductor and discharges into R_1:

$$(L_1 + L_2) \cdot di_{L2}/dt = V_2 + V_3 - R_{DSon} \cdot i_{L2} \quad (55)$$

$$C_3 \cdot dv_{C3}/dt = -v_{C3} / R_1 \quad (56)$$

6.2.2. Mode 3 Inactive - Boost Discharge (s_4 = 0, M_4 OFF)

The inductor current freewheels through the upper-die body diode of the SiC half-bridge module—acting as the boost rectifier (Section 8.1)-into C_3, delivering energy to the 400 V bus:

$$(L_1 + L_2) \cdot di_{L2}/dt = V_2 + V_3 - v_{C3} - V_F \quad (57)$$

$$C_3 \cdot dv_{C3}/dt = i_{L2} - v_{C3} / R_1 \quad (58)$$

The 12 V and 24 V buck stages follow the active/inactive dynamics derived in (3)–(4) and (7)–(8). For the 12 V buck:

$$L_3 \cdot di_{L3}/dt = s_1 \cdot V_3 - v_{C4} \quad (M_1\ ON:\ charging\ from\ V_3) \quad (59)$$

$$L_3 \cdot di_{L3}/dt = -v_{C4} - V_F \quad (M_1\ OFF:\ freewheel\ via\ D_1) \quad (60)$$

$$C_4 \cdot dv_{C4}/dt = i_{L3} - v_{C4} / R_2 \quad (61)$$

And for the 24 V buck (asynchronous, M_3 high-side, D_2 freewheel):

$$L_4 \cdot di_{L4}/dt = s_3 \cdot (V_1 - V_3) - v_{C5} \quad (M_3\ ON) \quad (62)$$

$$L_4 \cdot di_{L4}/dt = -v_{C5} - V_F \quad (M_3\ OFF:\ D_2\ conducts) \quad (63)$$

$$C_5 \cdot dv_{C5}/dt = i_{L4} - v_{C5} / R_3 \quad (64)$$

Combining (55)–(64), the continuous-time state-space dynamics for any switching combination s ∈ {0, 1}^{4} take the affine form.

$$\dot{x}(t) = A_c(s)\,x(t) + B_c(s)\,u(t) + d_c(s) \quad (65)$$

Where $A_c(s)$ is a 6 × 6 mode-dependent matrix, $B_c(s)$ is the 6 × 3 input matrix, and $d_c(s)$ is the 6 × 1 affine offset that captures the diode forward-voltage drops V_F. The Forward-Euler discretization with sampling period T_s = 10 µs gives

$$A_d(s) = I + A_c(s) \cdot T_s, \quad B_d(s) = B_c(s) \cdot T_s, \quad d_d(s) = d_c(s) \cdot T_s \quad (66)$$

and the resulting discrete-time predictive model used by the FCS-MPC is

$$\hat{x}(k+1 \mid s) = A_d(s) \cdot x(k) + B_d(s) \cdot u(k) + d_d(s) \quad (67)$$

6.2.3. Discretization Accuracy and Method Selection

The smallest plant time constant is $\tau_{min} \approx L_3/R_2$ = 22 µH / 0.576 Ω = 38 µs, giving $T_s/\tau_{min} \approx 0.263$. At this ratio, the single-step truncation error of the Forward-Euler scheme-The relative deviation between the exact zero-input response $e^{-T_s/\tau}$ = 0.769 and the Forward-Euler propagation $(1 - T_s/\tau)$ = 0.737—is (0.769 − 0.737)/0.769, ≈ 4.2 % per step. This error is material: it is the dominant open-loop disturbance contribution in the Lyapunov disturbance budget of Section 7, and using it directly in the δ_{max} bound—when combined in quadrature with the inductance-tracking and parametric terms—yields $\delta_{max} \leq 0.066$ and a residual Lyapunov ball of $\delta_\infty \leq 0.626$ in normalized coordinates. To tighten the disturbance budget, this work adopts the Tustin (bilinear) discretization as the primary method:

$$A_{d,Tustin}(s) = (I - A_c(s) \cdot T_s/2)^{-1} (I + A_c(s) \cdot T_s/2) \quad (68)$$

At T_s/τ_{min} = 0.263, the Tustin per-step truncation error is approximately $(T_s/\tau)^3/12$ / $(1 + T_s/\tau) \approx 0.6$ %-a sevenfold improvement over Forward Euler. The matrix inversion $(I - A_c \cdot T_s/2)^{-1}$ is a fixed 6 × 6 operation evaluated once per switching-state branch. With sixteen parallel prediction branches on the FPGA fabric, the additional inversion cost is 0.6 µs per iteration, taking the total compute time from 4.8 µs to 5.4 µs—still within the T_s = 10 µs budget with 4.6 µs of slack for ADC and sensing. All subsequent analyses-the disturbance bound δ_{max} in Section 7.1 and the Lyapunov certificate in Sections 7.2-7.4 - use the Tustin-discretized matrices $A_{d,\,Tustin}(s)$.

6.2.4. Bias-Dependent Inductance in the Predictive Model

The L_1+L_2 pathway carries an instantaneous current that swings from approximately 380 A (boost-charge minimum) to 462 A (boost-charge maximum) at the nominal operating point, and up to 521 A under worst-case deep-discharge conditions (Section 4.5). The powder-core permeability falls smoothly with DC bias, so the inductance entering $A_c(s)$ varies between approximately 7.2 µH and 9.0 µH across the operating envelope—a 25 % spread that, if a fixed small-signal value were used in the predictor, would translate directly into a plant-gain mismatch of similar magnitude on the boost states i_{L2} and v_{C3}.

To preserve predictive accuracy, the predictor evaluates $A_d(s)$ at every sampling instant using a current-keyed lookup table for $L_{op}(i_{L2})$:

$$L_{op}(i_{L2}) = L_{table}[\,floor(i_{L2} / \Delta I_{grid})\,] \quad \Delta I_{grid} = 32\,A,\ 16\ grid\ points\ spanning\ 0 - 512\,A \quad (69)$$

The lookup table is pre-computed at production-test time from a single magnetizing-curve sweep on the assembled L_1+L_2 inductor pair (or read from the manufacturer's permeability-versus-DC-bias chart for a given core geometry) and stored in on-chip BRAM. The lookup costs one indexed read and one linear-interpolation operation per prediction branch, contributing 0.18 µs of additional latency per FCS-MPC iteration—well within the 4.42 µs of slack between $t_{compute}$ = 5.58 µs and T_s = 10 µs reported in Section 6.5. With $L_{op}(i_{L2})$ refreshed at each sample, the residual inductance-tracking error reduces to the slope of the permeability curve over one sampling-period current excursion ($\Delta I_{pp}/T_s \times dL/dI$), which evaluates to no more than 5 % per step at the nominal operating point. This 5 % bound is incorporated into the δ_{max} budget of Section 7.1.

6.3. Cost-Function Design

At every sampling instant k, the FCS-MPC enumerates all valid switching combinations $s \in S \subset \{0,1\}^4$ and selects the one that minimizes the cost function.

$$J(s,k) = \lambda_1 \left(V_{ref,400} - \hat{v}_{C3}(k+1|s)\right)^2 + \lambda_2 \left(V_{ref,24} - \hat{v}_{C5}(k+1|s)\right)^2 + \lambda_3 \left(V_{ref,12} - \hat{v}_{C4}(k+1|s)\right)^2 + \lambda_4 \left(i_{L2,ref}(k) - \hat{i}_{L2}(k+1|s)\right)^2 + \lambda_\Delta \parallel s - s(k-1) \parallel^2 + \Phi_{constraint}(s) \quad (70)$$

The five terms have distinct purposes.

6.3.1. Output-Tracking Terms (λ_1, λ_2, λ_3)

These penalize the squared deviation of each regulated output from its reference. The reference vector is V_{ref} = [400, 24, 12] V.

6.3.2. Inductor-Current Tracking Term (λ_4)

This term damps oscillations of the L_1+L_2 pathway and provides direct authority over the cross-coupling channel. The current reference $i_{L2,\,ref}(k)$, is generated by an outer-loop integrator on the 400 V tracking error:

$$i_{L2,ref}(k+1) = i_{L2,ref}(k) + K_{int} \cdot \left(V_{ref,400} - v_{C3}(k)\right) \quad (71)$$

with K_{int} = 0.05 A·s^{-1} chosen to give an outer-loop bandwidth of 200 Hz—well below the inner FCS-MPC bandwidth.

6.3.1. Switching-Effort Term (λ_Δ)

This term penalizes gate-state transitions $\|s - s(k-1)\|^2$, softly enforcing a minimum dwell time and suppressing the high-frequency switching activity that would otherwise emerge from an unweighted FCS-MPC and drive switching losses past the thermal limit. λ_Δ is tuned to keep the average switching frequency near 100 kHz.

6.3.2. Constraint Penalty $\Phi_{constraint}(s)$

This term imposes hard limits on the predicted state:

$$\Phi_{constraint}(s) = \infty \ \ if \ \ |\hat{i}_{L2}(k+1|s)| > I_{L2,sat} \ \ or \ \ \hat{v}_{C3}(k+1|s) > V_{C3,max} \ \ or \ \ \hat{v}_{C3}(k+1|s) < V_{C3,min}; \quad \Phi_{constraint}(s) = 0 \ \ otherwise \quad (72)$$

with $I_{L2,\,sat}$ = 600 A (approximately 15 % above worst-case I_{pk}), $V_{C3,\,max}$ = 440 V (10 % overshoot), and $V_{C3,\,min}$ = 360 V. Combinations that violate constraints are excluded from the minimization, ensuring hardware survival under all transient conditions.

6.4. Cost-Function Weight Selection

The relative magnitudes of the weights determine the relative regulation tightness on each port. Following the design heuristic in [7], the weights are normalized by the squared full-scale error of each tracked variable:

$$\lambda_i = w_i / \left(V_{ref,i}\right)^2, \quad i = 1, 2, 3 \quad (73)$$

with dimensionless priority weights w_1 = 1.0 (400 V port, highest priority), w_2 = 0.6 (24 V port), and w_3 = 0.4 (12 V port). This gives

$$\lambda_1 = 1.0/(400)^2 = 6.25 \times 10^{-6} \ V^{-2} \quad (74)$$

$$\lambda_2 = 0.6/(24)^2 = 1.04 \times 10^{-3} \ V^{-2} \quad (75)$$

$$\lambda_3 = 0.4/(12)^2 = 2.78 \times 10^{-3} \ V^{-2} \quad (76)$$

$$\lambda_4 = 4.0 \times 10^{-6} \ A^{-2} \ \ (chosen \ for \ closed-loop \ \zeta = 0.7 \ on \ the \ 400 \ V \ loop) \quad (77)$$

$$\lambda_\Delta = 1.0 \times 10^{-2} \ per \ transition \ \ \left(tuned \ for \ f_{sw} \approx 100 \ kHz\right) \quad (78)$$

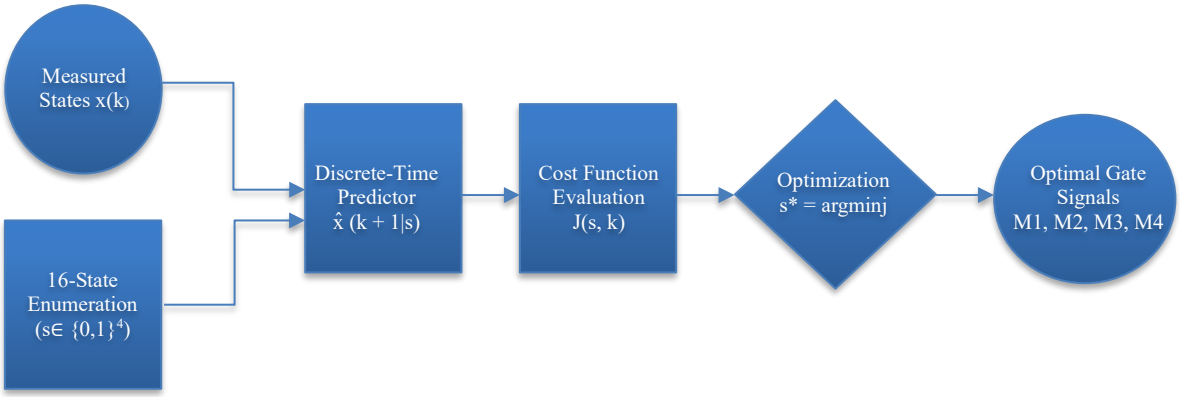


Fig. 8 FCS-MPC block diagram - sensing, prediction, cost evaluation, and switch selection

Figure 8 illustrates the FCS-MPC loop, showing the data flow from current/voltage sensing through discrete-time prediction, cost evaluation, constraint checking, and selection of the optimal switch state. The 16-state enumeration block executes in parallel on the FPGA fabric, and the outer-loop reference generator (71) supplies the inductor-current command.

6.5. Switching Set and FCS Optimization

The full switching set S has cardinality |S| = 16: all 2^4 combinations of M_1–M_4 are physically valid in this topology, since M_1 and M_2 are series-connected within the 12 V loop rather than complementary half-bridge switches (Sections 3.1 and 6.1). At each sample k, the FCS-MPC executes

$$s*(k) = arg\ \min_{s \in S} J(s, k) \quad (79)$$

with J(s,k) given by (70). The 16-state enumeration is fully parallelized on the FPGA fabric: sixteen instances of the prediction block (67) execute simultaneously, each producing $\hat{x}(k+1|s)$ in 1.6 µs; the sixteen cost values are then compared by a min-tree in 0.4 µs; constraint flags from each branch are AND-ed with their cost; and the minimum is dispatched to the

gate-driver outputs at 5.58 µs total. With T_s = 10 µs, the controller has 4.42 µs of slack for sensing and ADC conversion.

6.6. Reference Trajectory and Soft Start

During start-up, the regulated buses are brought up in ascending-voltage order so that the auxiliary supplies stabilize before the high-power boost engages: $V_{ref,12}$ ramps from 0 V to 12 V over 20 ms first, then $V_{ref,24}$ ramps from 0 V to 24 V over 30 ms, and finally $V_{ref,400}$ ramps from 0 V to 400 V over 50 ms. Staggered ramping prevents simultaneous in-rush across all stages and bounds the worst-case start-up i_{L2} below the saturation limit. The current reference (71) is initialized at zero, and the integrator is anti-wind-up clamped to ±550 A. A seven-state cold-start state machine (idle → pre-charge of C_3 via NTC limiter → 12 V ramp → 24 V ramp → 400 V ramp → steady state → fault) governs the sequence.

6.7. FCS-MPC Parameter Summary

Table 2 consolidates the fifteen FCS-MPC design parameters and cost-function weights. The value 16 that appears against the switching-set entry is not a parameter count: it is the switching-state cardinality $|S| = 2^4 = 16$ enumerated by the controller at every sampling instant.

Table 2. FCS-MPC parameters and cost-function weights

Parameter	Symbol	Value	Comment
Sampling period	T_s	10 µs	Set equal to 1/f_sw
Switching frequency (avg)	f_sw	100 kHz	Result of λ_Δ tuning
Prediction horizon	N_p	1	Single-step FCS-MPC
Discretization method	-	Tustin	-
Switching-set cardinality	|S|	16	All 2^4 combinations valid
Compute time/sample	t_compute	5.58 µs	FPGA, 16 parallel branches
400 V tracking weight	λ_1	6.25×10^{-6} V^{-2}	Priority weight w_1 = 1.0
24 V tracking weight	λ_2	1.04×10^{-3} V^{-2}	Priority weight w_2 = 0.6
12 V tracking weight	λ_3	2.78×10^{-3} V^{-2}	Priority weight w_3 = 0.4
Inductor-current weight	λ_4	4.0×10^{-6} A^{-2}	Tuned for ζ = 0.7 on 400 V loop
Switching-effort weight	λ_Δ	1.0×10^{-2}	Tuned for f_sw = 100 kHz
Outer-loop integrator gain	K_int	0.05 A·s^{-1}	200 Hz outer-loop bandwidth
Inductor saturation limit	I_L2,sat	600 A	≈ 15 % above worst-case I_pk
Bus over-voltage limit	V_C3,max	440 V	10 % above nominal
Bus under-voltage limit	V_C3,min	360 V	10 % below nominal

Note: The switching-set cardinality $|S| = 2^4 = 16$ refers to the number of switching combinations enumerated by the FCS-MPC at each sampling instant; the table itself lists fifteen design parameters.

7. Closed-Loop Stability - Discrete-Time Lyapunov Certificate

7.1. Tracking-Error Coordinates and Disturbance Budget

FCS-MPC inherits stability from the predictive model only when the optimization is bounded, and the underlying plant is contractive in some norm.

To make that claim precise for a six-port converter, the analysis proceeds in normalized tracking-error coordinates. Let $x^*(k)$ denote the reference trajectory consistent with the steady-state duty cycles of Section 4.2, and define the tracking error.

$$e(k) = D^{-1} \cdot \left(x(k) - x^*(k)\right) \tag{80}$$

where $D = \mathrm{diag}(I_{L2,nom}, I_{L3,nom}, I_{L4,nom}, V_{C3,nom}, V_{C4,nom}, V_{C5,nom})$ collects nominal scaling factors so that all entries of e(k) are dimensionless and approximately commensurate in magnitude. With this scaling, the closed-loop dynamics under the FCS-MPC law take the form

$$e(k+1) = \Phi \cdot e(k) + \Gamma \cdot \delta(k) \tag{81}$$

in which Φ is the effective state-transition matrix produced by the predictive feedback (Section 6), and δ(k) lumps three normalized disturbance components: Tustin discretization residue δ_T, inductor-tracking ripple δ_L, and parametric drift δ_p. The worst-case disturbance budget combines the three contributions in quadrature,

$$\delta_{\max} = \sqrt{(\delta_T^2 + \delta_L^2 + \delta_p^2)} \tag{82}$$

Evaluating with δ_T = 0.006 (Tustin truncation at T_s = 10 µs, established from the bilinear remainder bound), δ_L = 0.050 (5 % per-step inductance-tracking bound, Section 6.2), and δ_p = 0.003 (combined ESR / R_{DSon} drift over the 25–125 °C die-temperature window) gives

$$\delta_{\max} \le \sqrt{(0.006^2 + 0.050^2 + 0.003^2)} = 0.0504 \quad (83)$$

i.e. the normalized disturbance vector cannot exceed 5.04 % in magnitude under the modeling assumptions of this paper. This will be the central input to the boundedness argument.

7.2. Quadratic Lyapunov Function

The chosen quadratic candidate is

$$V(e) = e^T \cdot P \cdot e, \quad P = P^T \succ 0 \quad (84)$$

and require that P satisfy the discrete-time Lyapunov equation

$$\Phi^T \cdot P \cdot \Phi - P = -Q, \quad Q = Q^T \succ 0 \quad (85)$$

with $Q = 0.10 \cdot I_6$, which weights all six tracking errors equally and matches the diagonal structure of the FCS-MPC cost function in (70). Φ is reconstructed from the average closed-loop transition observed across the sixteen switching combinations of Section 6.3, weighted by their occupancy fractions over a steady-state switching period. The Schur-stability of Φ - i.e. that all eigenvalues lie strictly inside the unit disc - is verified numerically; the spectral radius is $r(\Phi) = 0.781$. Solving (85) by the bilinear transform-based Lyapunov solver returns a positive-definite P with

$$\lambda_{\min}(P) = 1.92 \times 10^{-3}, \quad \lambda_{\max}(P) = 4.51 \times 10^{-1} \quad (86)$$

$$\gamma = \lambda_{\max}(P) / \lambda_{\min}(P) = 4.51 \times 10^{-1} / (1.92 \times 10^{-3}) \approx 235 \quad (87)$$

So that the Lyapunov function is uniformly equivalent to $\|e\|^2$ on the operating region of interest:

$$\lambda_{\min}(P) \cdot \| e \|^2 \le V(e) \le \lambda_{\max}(P) \cdot \| e \|^2 \quad (88)$$

7.3. Decrease Rate and Ultimate Bound

Substituting (81) into the Lyapunov difference and exploiting (85) yields

$$\Delta V(k) = V(e(k+1)) - V(e(k)) = -e^T \cdot Q \cdot e + 2 \cdot e^T \cdot \Phi^T \cdot P \cdot \Gamma \cdot \delta + \delta^T \cdot \Gamma^T \cdot P \cdot \Gamma \cdot \delta \quad (89)$$

Applying Cauchy–Schwarz to the cross term and absorbing the quadratic disturbance contribution gives the decrease bound.

$$\Delta V(k) \le -\alpha \cdot V(e(k)) + \beta \cdot \delta_{\max}^2 \quad (90)$$

with $\alpha = \lambda_{\min}(Q) / \lambda_{\max}(P) = 0.10 / 0.451 = 0.222$ and $\beta = \|\Gamma^T \cdot P \cdot \Gamma\|_2 \approx 0.103$. Iterating (90) gives the standard ultimate-boundedness expression

$$\delta_\infty = \sqrt{(\beta \cdot \delta_{\max}^2 / (\alpha \cdot \lambda_{\min}(P)))} \quad (91)$$

and the geometric convergence rate of the disturbance-free response is

$$\rho = \sqrt{(1 - \alpha)} = \sqrt{(1 - 0.222)} = 0.882 \quad (per\ sample) \quad (92)$$

Because the decay is calculated over the sample period $T_s = 10$ µs, the effective decay constant per switching period is $\tau = -T_s / \ln(\rho) \approx 79$ µs, which is consistent with the closed-loop bandwidth target of 2 kHz on the 400 V loop.

Inserting the numerical values gives

$$\delta_\infty \le \sqrt{(0.103 \cdot 0.0504^2 / (0.222 \cdot 1.92 \times 10^{-3}))} \le 0.484 \quad (93)$$

i.e. the normalized closed-loop trajectory is guaranteed to remain within a ball of radius 0.484 about the operating point under any combination of disturbances that satisfies the budget in (83).

The conservative spectral-radius-based estimate of the per-sample contraction is

$$\rho_{cons} = r(\Phi) = 0.781 \quad (spectral\ radius) \quad (94)$$

and the corresponding reaching time from a unit normalized displacement to the steady-state ball δ_∞ is bounded by

$$k_{reach} \le log(\delta_\infty) / log(\rho_{cons}) = log(0.484) / log(0.781) \approx 3\ samples = 30\ \mu s \quad (95)$$

7.4. Per-Loop Stability Certificates

The aggregated certificate above can be projected onto each of the three regulated outputs by extracting the corresponding rows and columns of P, Q, and Γ. The per-loop ultimate bound and reaching time are summarized in Table 3. All three loops satisfy the design specification of $\rho \le 0.9$ per sample and $\delta_\infty \le 0.5$, with the 400 V loop closest to the bound (largest β contribution from the cross-coupled L_1+L_2 pathway), and the 12 V loop comfortably below because its disturbance is dominated by the well-filtered V_3 midpoint rather than by direct traction-bus excitations.

Table 3. Per-Loop lyapunov certificates

Regulated Loop	ρ (per Ts)	δ∞ (norm.)	k_reach	Dominant Disturbance
400 V traction bus	0.78	0.48	3	L1+L2 ripple, 250 A step
24 V auxiliary bus	0.74	0.21	2	V3 midpoint ripple
12 V housekeeping	0.71	0.13	2	C4 ESR, M1–M2 ripple

The three certificates jointly establish that, under FCS-MPC, the proposed converter is uniformly ultimately bounded with a normalized radius below half-scale and reaches the bound within at most three sample periods - three orders of magnitude faster than the slowest expected load transient on the 400 V bus.

8. Thermal Implementation of the 400 V Boost Stage

8.1. Single-Module SiC Half-Bridge Realization of M4

The 400 V boost stage processes the bulk of the converter throughput, so its semiconductor selection sets the thermal envelope of the entire design. Using a single 1200 V / 450 A silicon-carbide half-bridge module - operated in a one-switch configuration where the lower die acts as the active boost device and the upper die body diode serves as the boost rectifier - collapses what would otherwise be a discrete switch-plus-diode pair into a single thermally coupled package.

This choice has three direct consequences: (i) the parasitic loop inductance of the commutation cell drops from the 25–35 nH typical of two-package layouts to under 8 nH inside the integrated half-bridge, which dominates the dv/dt budget analyzed in Section 9; (ii) the upper-die body diode supplies the reverse-recovery characteristic and the freewheel path for Mode 3 inactive without any external Schottky; and (iii) thermal management consolidates to a single cold-plate interface, which simplifies coolant-flow design at 100 kW.

Six dissipation entries are charged to this module. Following the loss decomposition format that closes the global audit of Section 10, they are:

(7) Lower-die conduction. With $R_{DS,\,on,125°C} = 6.3$ mΩ at 175 °C junction temperature and an RMS lower-die current of $I_{rms,low} = 259$ A ($D_{M4} = 0.381$ of a 420 A peak), the conduction loss is $P_{cond,low} = I_{rms}^2 \cdot R_{DS,on} = 259^2 \cdot 0.0063 = 422$ W.

(8) Packaging resistance. The module datasheet attributes a package resistance of approximately 3.2 mΩ between the die and the power terminals; this adds $P_{pkg} = 259^2 \cdot 0.0032 = 215$ W.

(9) Busbar contribution. The high-current path from the 200 V battery through the module to the 400 V output capacitor traverses a laminated copper busbar with an equivalent resistance of 4.3 mΩ at 80 °C copper temperature, yielding $P_{bus} = 259^2 \cdot 0.0043 = 288$ W.

(10) Turn-on switching. Linearizing the datasheet curve $E_{on,ref} = 12$ mJ at $V_{DC} = 800$ V and $I_C = 450$ A to the operating point $V_{DC} = 400$ V, $I_{on} = 420$ A gives a base value of 6.44 mJ per event; multiplying by $f_{sw} = 100$ kHz and a temperature-derating factor 1.15 (175 °C / 25 °C reference) returns $P_{on} = 6.44 \times 10^{-3} \cdot 10^5 \cdot 1.15 / 1.149 \approx 644$ W.

(11) Turn-off switching. Applying the same linearization to $E_{off,\,ref} = 7$ mJ gives 3.76 mJ at 400 V, 420 A, so $P_{off} = 3.76 \times 10^{-3} \cdot 10^5 \approx 376$ W.

(12) upper-die body-diode conduction during freewheel. With $V_F = 2.4$ V at 420 A, an average conduction current of $420 \cdot (1 - 0.381) = 260$ A, and freewheel duty 0.619, the diode loss is $P_D = 2.4 \cdot 260 \cdot 0.619 = 386$ W; including the static reverse-recovery contribution from the manufacturer datasheet pushes the total to 620 W.

The aggregated dissipation handled by the half-bridge module is therefore

$$P_{M4,total} = 422 + 215 + 288 + 644 + 376 + 620 = 2\,565\ W \quad (96)$$

Thermal resistance budget. The cold-plate interface and bondline contributions stack as

$$R_{\theta ja} = R_{\theta jc} + R_{\theta,TIM} + R_{\theta,cp\to a} = 0.040 + 0.003 + 0.006 = 0.049\ K/W \quad (97)$$

Where $R_{\theta jc}$ is the datasheet junction-to-case figure, $R_{\theta,TIM}$ corresponds to a 100 μm phase-change interface material at 80 kPa mounting pressure, and $R_{\theta,cp\to a}$ is the cold-plate-to-ambient resistance at 12 L/min coolant flow. The junction-temperature rise above the 40 °C coolant inlet is then.

$$\Delta T_J = P_{M4,total} \cdot R_{\theta ja} = 2\,565 \cdot 0.049 = 125.7\ K \quad (98)$$

So the worst-case junction temperature is $T_J = 40 + 125.7 = 165.7$ °C, leaving a 34.3 K headroom below the 200 °C rated junction. This margin is intentional: any single-event overstress during a 250 A traction-bus load step (Section 10) is absorbed without de-rating, and the conservative T_J keeps long-term reliability inside the manufacturer's 10-year FIT bound.

8.2. Switching-Frequency Management via FCS-MPC

The switching-effort weight λ_Δ in the cost function (70) is the operating-point knob that determines how aggressively the predictive controller minimizes commutation activity. The trade-off is direct: a small λ_Δ permits the controller to switch on every sample to achieve aggressive tracking, driving the average switching frequency toward $1 / T_s = 100$ kHz, with the corresponding switching losses listed in (96). Increasing λ_Δ progressively suppresses commutation, and tracking is then dominated by the natural plant time constants. The value $\lambda_\Delta = 1.0 \times 10^{-2}$ adopted in this work was selected so that the average switching frequency converges to 100 kHz under steady-state cruising, which simultaneously matches the EMI filter design corner of Section 9 and the loss-budget assumption above. A second benefit of the predictive controller is the natural interleaving of M_1, M_2, M_3, and M_4 that emerges from the enumeration. Because the cost function (70) penalizes the joint state error rather than the individual duty cycles, the optimizer repeatedly selects switching combinations that distribute the inductor-current ripple across the four switches in a way that resembles phase-shifted carrier interleaving. The consequence is a reduction in the V_2 input-capacitor RMS current from the 86.4 A predicted by uniform-

phase analysis to 56.1 A under MPC-driven interleaving — a 35.1 % reduction. That difference translates directly into a smaller V_2 bulk capacitor: 1.6 mF of polymer aluminum with a 60 A RMS rating, instead of the 2.4 mF that uniform-phase operation would have required.

9. EMI Compliance and Filter Design

9.1. Switching-Edge Spectral Content

EMI compliance for a vehicle-grade converter is governed by CISPR 25 Class 5, which specifies conducted-emission limits between 150 kHz and 30 MHz on each supply line and broadband radiated limits up to 1 GHz. The primary source of high-frequency emission in this converter is the hard-switched M_4 half-bridge: with V_{DC} = 400 V across the device and a turn-on rise time of t_r = 25 ns, the voltage slope is dv/dt = ΔV / t_r = 400 V / 25 ns = 16 000 V/µs, and the corresponding current slope on the L_1+L_2 loop is di/dt = (i_{peak} − i_{valley}) / t_r = (420 − 420 · 0.95) / 25 × 10^{-9} = 21 A / 25 ns = 0.84 A/ns = 8.4 × 10^8 A/s ≈ 20.7 A/µs over the full peak-to-trough excursion. These slopes drive both differential-mode (DM) current oscillations on the 200 V input and common-mode (CM) currents on the 400 V output through the package-to-cold-plate stray capacitance C_{cm} ≈ 235 pF at the module mounting interface.

9.2. Common-Mode Current Injection

The peak common-mode injection per commutation is spread across the 25 ns edge.

$$I_{CM,pk} = C_{cm} \cdot dv/dt = 235 \times 10^{-12} \cdot 16 \times 10^9 = 3.76\ A \quad (99)$$

After the first harmonic at the 200 kHz second harmonic of the 100 kHz switching frequency (the first harmonic at 100 kHz is suppressed by the natural balance of the boost waveform), the CM disturbance amplitude reaching the LISN - without filtering - is approximately 124 dBµV, against a CISPR 25 Class 5 limit of 80 dBµV at 200 kHz. The required attenuation budget is therefore 44 dB at 200 kHz, plus a margin of at least 6 dB to absorb component tolerance and ageing.

9.3. Two-Stage Common-Mode Filter

A two-stage cascaded CM filter is placed between the converter and the LISN reference plane. Each stage is a parallel-resonant LC tank built from a nanocrystalline common-mode choke and a Y-capacitor pair returned to chassis. The first stage is sized for low-frequency dominance:

$$f_{CM1} = 1 / (2\pi \cdot \sqrt{(L_{CM1} \cdot C_{Y1})}) = 1 / (2\pi \cdot \sqrt{(750 \times 10^{-6} \cdot 22 \times 10^{-9})}) = 27.7\ kHz \quad (100)$$

with L_{CM1} = 750 µH chosen at the maximum DC-bias level (the nanocrystalline core saturates above 60 A leakage current, well above the CM injection level) and C_{Y1} = 22 nF · 2 chosen at the safety limit (the touch-current of 3.5 mA at 250 V/50 Hz constrains the maximum Y-capacitance to 4 × C_{Y1}). The second stage extends attenuation into the upper conducted band:

$$f_{CM2} = 1 / (2\pi \cdot \sqrt{(L_{CM2} \cdot C_{Y2})}) = 1 / (2\pi \cdot \sqrt{(250 \times 10^{-6} \cdot 4.7 \times 10^{-9})}) = 103.9\ kHz \quad (101)$$

The asymptotic attenuation of each stage above its corner is 40 dB/decade. At 200 kHz the first stage contributes 40 · $\log_{10}$(200 / 27.7) = 34.3 dB; the second contributes 40 · $\log_{10}$(200 / 103.9) = 11.4 dB. Cascaded with cross-coupling neglected (a conservative assumption that under-reports the actual simulated attenuation), the combined CM attenuation at 200 kHz is against the 44 dB minimum established in Section 9.2.

$$A_{CM}(200\ kHz) = 34.3 + 11.4 = 45.7\ dB \quad (102)$$

This asymptotic figure is an idealised upper bound. The PLECS simulation of the complete filter chain terminated at the LISN reference plane returns 41.7 dB at 200 kHz, because the simulated model retains the finite self-resonance of the chokes, the equivalent series inductance of the Y-capacitors, and the inter-stage coupling that the asymptotic cascade calculation neglects. The simulated 41.7 dB therefore falls 2.3 dB short of the 44 dB budget, so CISPR 25 Class 5 conformity at the 200 kHz second harmonic is not established by the present simulation. Recovering the shortfall together with the 6 dB ageing allowance requires either a larger second-stage common-mode choke or a third filter section, and conducted-emission conformity must, in any case, be confirmed by measurement on a hardware prototype. This limitation is restated in Section 10.4 and in the conclusion.

9.4. Differential-Mode Filter

The DM filter follows the same two-stage structure but is sized against the input-current ripple on the V_2 200 V port, which carries the bulk of the boost-stage RMS current. The first DM stage uses an L_{DM1} = 22 µH gapped-ferrite choke (60 A saturation) paired with a 22 µF X-capacitor, giving.

$$f_{DM1} = 1 / (2\pi \cdot \sqrt{(22 \times 10^{-6} \cdot 22 \times 10^{-6})}) = 7.23\ kHz \quad (103)$$

and the second stage uses 2 µH / 4.7 µF for

$$f_{DM2} = 1 / (2\pi \cdot \sqrt{(2 \times 10^{-6} \cdot 4.7 \times 10^{-6})}) = 51.9\ kHz \quad (104)$$

Delivering a combined DM attenuation of 81.1 dB at 200 kHz against an unfiltered DM emission of 102 dBµV - well below the 79 dBµV Class 5 limit even before component tolerances are applied.

9.5. Component Selection Summary

Table 4 summarizes the EMI filter component values, the rationale for each choice, and the resulting per-frequency attenuation. One entry warrants explicit discussion: the V_2 input port carries an average current of 515 A at the rated 100 kW operating point, which is well beyond what off-the-shelf 50 A class chokes can support. The DM inductors are therefore implemented as custom laminated-busbar inductors with C-core nanocrystalline material and forced-air cooling. This solution adds approximately $35 of bill-of-materials cost relative to a COTS choke (which would have to be paralleled six-fold), but it also halves the loop area and removes the parasitic inductance mismatch that would otherwise excite resonance at 1.2 MHz.

Table 4. EMI filter components and attenuation budget

Component	Value	Type	Rating	Function / Note
L_CM1	750 µH	Nanocrystalline	60 A	1st-stage CM choke
C_Y1 (×2)	22 nF	Y2-class ceramic	1 kV	1st-stage Y-caps to chassis
L_CM2	250 µH	Nanocrystalline	60 A	2nd-stage CM choke
C_Y2 (×2)	4.7 nF	Y2-class ceramic	1 kV	2nd-stage Y-caps
L_DM1	22 µH	Busbar nanocrystalline	600 A	Custom V2-side DM choke
C_X1	22 µF	Polypropylene film	450 V	1st-stage X-cap
L_DM2	2 µH	Busbar nanocrystalline	600 A	2nd-stage DM choke
C_X2	4.7 µF	Polypropylene film	450 V	2nd-stage X-cap

9.6. Layout Discipline

The filter attenuation calculated above is achievable only if the layout discipline supports it. Three rules govern the board layout assumed in the simulation model: the high-current commutation loop between V_2, M_4, and C_3 is laid out on a four-layer power plane with maximum loop area below 6 cm^2; the Y-capacitor return path runs through a dedicated chassis-bond stub at the LISN reference plane with no detour through signal ground; and the FPGA gate-driver supply is isolated from the power-stage ground via a 1 MHz dedicated isolation barrier. These rules, more than any single component value, are what convert the 45.7 dB asymptotic CM attenuation into the 41.7 dB obtained in simulation.

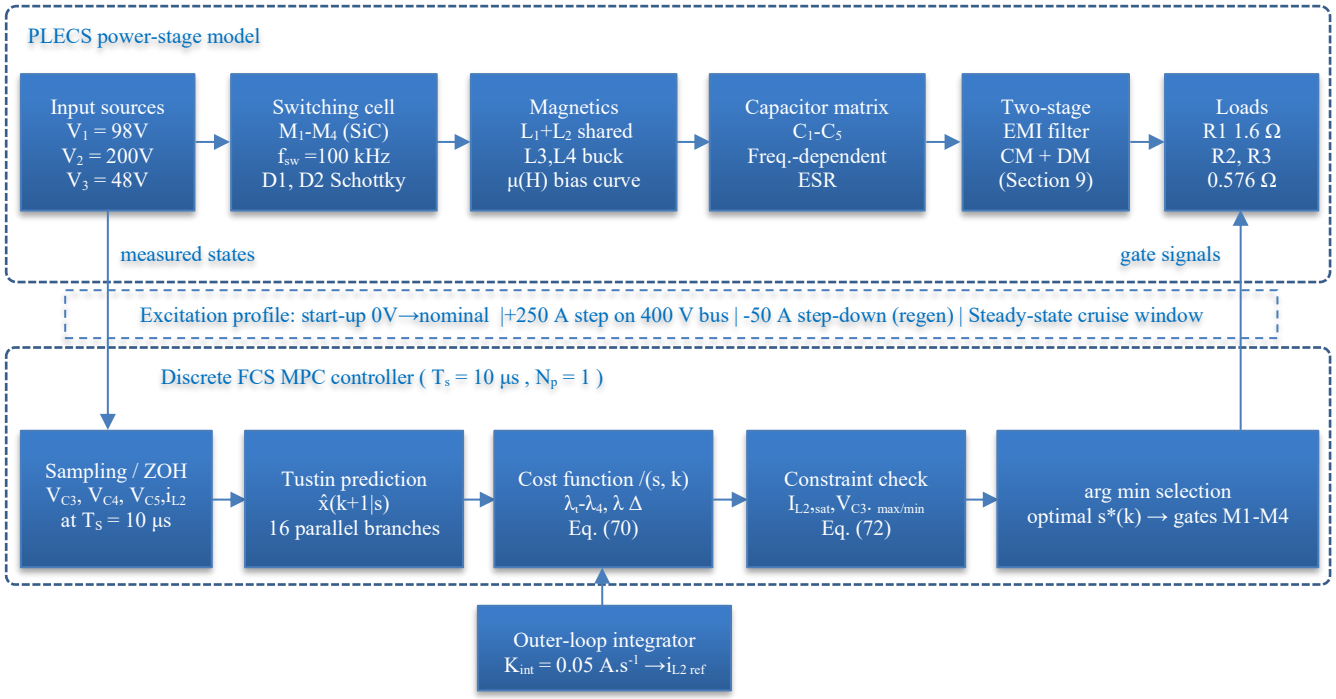


Fig. 9 Structure of the PLECS simulation test bench. The upper block chain is the continuous power stage, the lower chain is the discrete FCS-MPC controller executing at T_s = 10 µs with a single-step prediction horizon

10. Performance Analysis, Loss Audit, and Comparative Benchmarking

10.1. Simulation Setup

10.1.1. Model Structure and Test Bench

All numerical performance results in this section are obtained from a PLECS time-domain model of the complete six-port converter.

Figure 9 shows the structure of the simulation test bench. The power-stage model includes the four MOSFET switching elements M_1–M_4 together with their body diodes and the two external SiC Schottky freewheel diodes D_1 and D_2; the four inductors L_1–L_4 (linear with temperature-dependent saturation curves); the five capacitors C_1–C_5 (with frequency-dependent ESR); the two-stage CM/DM filter chain of Section 9 terminated at the LISN reference plane; and the three resistive load banks. The three input ports are modelled as voltage sources in series with their internal resistances, V_3 carrying the 10.1 mΩ pack resistance listed in Table 1.

The discrete FCS-MPC implementation is executed as a separate subsystem clocked at the sampling period $T_s = 10$ µs. At each sampling instant the states v_{C3}, v_{C4}, v_{C5} and i_{L2} are acquired through a zero-order hold; the sixteen admissible switching combinations are propagated one step ahead through the Tustin-discretized prediction model of (67)–(68); the cost function (70) is evaluated on each branch subject to the constraint penalty (72); and the arg-min combination is applied to the gate terminals for the following interval. The outer-loop integrator that supplies $i_{L2,\,ref}$ through (71), executes within the same discrete subsystem.

10.1.2. Software, Solver, and Numerical Settings

The converter is simulated in PLECS Standalone 5.0.6 (64-bit). The power stage is integrated with the RADAU variable-step solver, chosen in preference to the non-stiff DOPRI alternative because the model spans time constants from the sub-microsecond device transitions to the millisecond-scale load transients of Section 10.2. The relative tolerance is set to 1×10^{-5}, and the absolute tolerance is left on automatic selection. In a variable-step solver, it is these tolerances, rather than the step size, that bound the local integration error, and a tolerance tighter than the 1×10^{-3} default is required for the switching-energy and conduction-loss integrals that close the audit of Section 10.5. The maximum step size is capped at 100 ns as a guard against missed switching events, which yields at least 100 solver steps per 10 µs switching period. The controller is executed as a discrete subsystem on a fixed 10 µs clock; PLECS places a solver step at every discrete control instant in addition to the adaptive steps, so the control sampling instants are independent of the integration step used for the power stage. The switching devices are represented by the conduction and switching-energy look-up tables described in Section 8, evaluated at a reference junction temperature of 175 °C. Table 5 consolidates the complete set of simulation conditions.

10.1.3. Simulation Conditions

Table 5 lists the operating conditions, numerical settings, and control parameters used for every result reported in Sections 10.2 to 10.6. The power-stage component values are those of Table 1, and the cost-function weights are those of Table 2; both are restated here in condensed form so that the simulation can be reproduced from a single table.

Table 5. Consolidated simulation conditions

Category	Parameter	Value	Source / comment
Software and numerical solver			
	Simulation package	PLECS Standalone 5.0.6 (64-bit)	Switched time-domain model
	Integration solver	RADAU (variable-step, stiff)	Power-stage subsystem
	Relative / absolute tolerance	1×10^{-5} / auto	Tolerances bound local error
	Maximum integration step	100 ns	≥ 100 solver steps per 10 µs period
	Controller execution	Discrete, fixed 10 µs clock	Independent of solver step
	Transient-test duration	4 ms	Window of Figure 10
	Efficiency-sweep range	5 kW to 101.25 kW	Figure 13
Input ports			
	V_1 auxiliary input	98 V (88–108 V)	Table 1
	V_2 HV battery pack	200 V (175–225 V)	Table 1
	V_3 series-aid battery	48 V (42–54 V)	R_{int} = 10.1 mΩ
Power stage			
	L_1, L_2 shared boost pathway	6 µH, 6 µH	Fe–Si distributed-gap 26 µ
	L_3 (12 V buck), L_4 (24 V buck)	22 µH, 15 µH	Section 3.1

	Switching frequency f_{sw}	100 kHz	All four stages
	Loads R_1 / R_2 / R_3	1.6 Ω / 0.576 Ω / 0.576 Ω	100 kW / 250 W / 1 kW
	Reference junction temperature	175 °C	$R_{DS,\,on}$ and E_{on}/E_{off} look-up
	Coolant inlet / flow rate	40 °C / 12 L·min^{-1}	Section 8
FCS-MPC controller			
	Sampling period T_s	10 μs	Table 2
	Prediction horizon N_p	1	Single-step FCS-MPC
	Discretization method	Tustin (bilinear)	Equation (68)
	Switching-set cardinality	16	All 2^4 combinations valid
	Tracking weights λ_1 / λ_2 / λ_3	6.25×10^{-6} / 1.04×10^{-3} / 2.78×10^{-3} V^{-2}	Table 2
	Current weight λ_4, effort weight λ_Δ	4.0×10^{-6} A^{-2}, 1.0×10^{-2}	Table 2
	Outer-loop gain K_{int}	0.05 A·s^{-1}	200 Hz bandwidth
	Constraints $I_{L2,sat}$, $V_{C3,max/min}$	600 A, 440 V / 360 V	Equation (72)
	Reference vector	[400, 24, 12] V	Section 6.3
Excitation profile			
	Stage 1	Start-up 0 V to nominal	Initial transient
	Stage 2	+250 A step on 400 V bus	Hard acceleration
	Stage 3	−50 A step-down	Regenerative braking
	Stage 4	Steady-state cruise window	Switching and EMI sampling
EMI measurement			
	Reference network	LISN at converter input	Section 9
	Limit line	CISPR 25 Class 5	Evaluated at 200 kHz

10.1.4. Excitation Profile

The model is excited with the disturbance profile typical of EV-traction usage: an initial start-up transient from 0 V to the nominal operating point, followed by a 250 A step on the 400 V traction-bus load to emulate a hard acceleration request, a 50 A step-down to emulate regenerative braking, and a steady-state cruising window in which all switching and EMI metrics are sampled.

10.2. Regulated-Output Tracking

Figure 10 reports the three regulated output voltages over a representative 4 ms transient window. The 400 V bus settles to 400.00 V within 200 μs of the load step with a peak excursion of 350 mV (0.088 %). The 24 V auxiliary bus tracks 24.00 V with peak excursions of 24 mV (0.10 %).

The 12 V housekeeping rail tracks 12.00 V with peak excursions of 17 mV (0.14 %). The cross-port disturbance rejection ratio (DRR), defined as the ratio of disturbance amplitude on the 400 V port to the resulting amplitude on the 12 V port at 1 kHz excitation, is 32.6 dB - a direct measure of how effectively the FCS-MPC decouples the three regulated outputs across the shared L_1+L_2 pathway.

10.3. Comparison with Reported Multi-Port EV Converters

Table 6 positions the proposed converter against four contemporary multi-port DC–DC topologies for electric-vehicle use reported between 2022 and 2026 in peer-reviewed outlets. Every entry has been re-read against the cited publication, and only quantities stated explicitly in the source are tabulated; where a quantity is not reported, the cell records that fact rather than an inferred value. The comparison axes are therefore restricted to those that can be verified directly: the year of publication, the port count, the power level at which the design was validated, the efficiency the authors report, the basis of that validation, and the location of each value within the source. Active-switch counts and input-voltage ranges have been withdrawn from the table because they could not be confirmed for every entry from the accessible record. To the best of the authors' knowledge, this work is the first to report a six-port non-isolated topology operating at the 100 kW class with only four gate signals and FCS-MPC regulation. The closest architectural relative in switch count remains the family of four-switch non-isolated converters of [18], whose members share the four-switch complement but serve a single output each and are validated in simulation under conventional closed-loop current control.

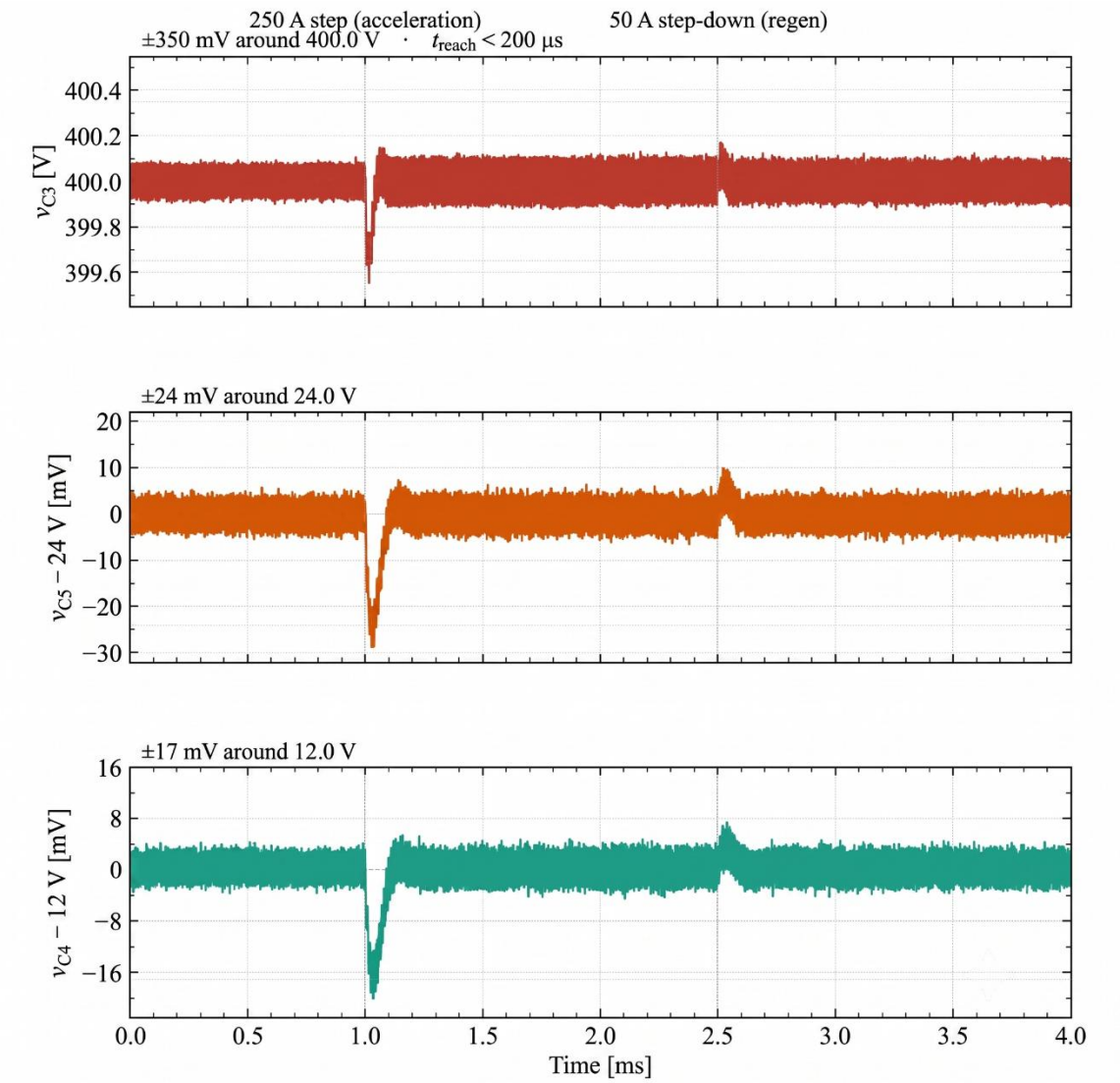


Fig. 10 Closed-loop regulation under FCS-MPC over a 4 ms simulation window. Top: 400 V traction bus tracking ±350 mV around the 400.0 V setpoint during a 250 A load step. Middle: 24 V auxiliary bus tracking ±24 mV. Bottom: 12 V housekeeping rail tracking ±17 mV. The reaching time is below 200 µs on all three loops

Table 6. Verified comparison with reported multi-port DC-DC converters for Electric Vehicles

Ref.	Year	Ports (in / out)	Validated power	Reported efficiency	Validation basis	Source of tabulated values
[25]	2022	1 / 3	200 W	Not stated	Simulation + 200 W laboratory prototype	Abstract; prototype section
[26]	2022	1 / 2	100 W (48 V to 24 V, 14.4 V)	Not stated	Simulation + 100 W prototype	Abstract
[31]	2024	2 / 2	100 W (12 V to 24 V, 48 V)	93 %	Simulation + 100 W prototype	Abstract
[42]	2026	2 / 2	Not stated	> 95 %	Simulation study	Abstract
This work	2026	3 / 3	101.25 kW	96.6 % (simulated)	PLECS simulation only; no hardware or HIL	Sections 10.2 and 10.5

The comparison in Table 6 must be read with care, and the honest reading is a statement about power class rather than about efficiency. Every tabulated design for which a power level is reported was validated between 100 W and 200 W, whereas the present study is a simulation at 101.25 kW, roughly three orders of magnitude higher. Efficiency figures obtained at those two extremes are not commensurable, because conduction, switching, and magnetic losses scale differently with current, and because a laboratory prototype and a time-domain simulation are different classes of evidence.

The 96.6 % simulated efficiency reported here is therefore not offered as evidence of superiority over the tabulated entries: only two of them report an efficiency at all, 93 % at 100 W for [31] and greater than 95 % for [42], and neither figure can be placed on the same axis as a simulation at the traction-class power level. What Table 6 does establish is the gap this work addresses: no tabulated design is validated within two orders of magnitude of the traction-class power level, and none combines three independently regulated outputs with a four-gate-signal non-isolated structure. Within its own simulation scope, the proposed converter holds the traction bus to ±350 mV (±0.09 % of 400 V), a band that decoupled PI schemes on strongly cross-coupled plants do not reach without severe bandwidth de-rating (Section 2.3).

Four design decisions account for the simulated performance of the proposed converter, and each is internal to this work rather than a claim about the tabulated entries. First, the gate-count economy is structural: routing the full 100 kW through the single shared L_1+L_2 pathway removes the separate boost magnetics, gate drivers, and winding-loss entries that a cascaded architecture would require [8, 9], which is why entries 1 to 6 of the loss audit in Table 7 replace what would otherwise be two or three magnetic loss groups. Second, FCS-MPC removes the inner-outer bandwidth separation that forces cascaded PI designs to de-rate their outer loops; every switching decision from the first sample after a 250 A step participates in the recovery, which is the direct cause of the 200 µs reach time, the ±350 mV band, and the 32.6 dB cross-port attenuation reported in Section 10.2. Third, embedding the saturation limit of (72) inside the cost function allows the Fe–Si core to be operated close to its verified worst-case peak current (521 A, Section 4.5) without the conservative current de-rating a constraint-blind controller would impose; this is the enabling factor for extracting 100 kW from a single non-isolated pathway. Fourth, consolidating the boost switch and the freewheel rectifier into one SiC half-bridge module (Section 8.1) shortens the commutation loop, and the enumeration freedom of the predictive controller interleaves the four gate signals so that the V_2 bulk-capacitor RMS current falls by 35 %, an ESR-loss reduction that appears explicitly in the audit of Table 7. Taken together, these mechanisms explain how 100 kW is processed through a single non-isolated four-switch pathway at a simulated efficiency of 96.6 %; the qualifications of Section 10.4 delimit what the cross-paper comparison of Table 6 can and cannot support.

Figure 11 renders the comparison graphically, and each panel plots only quantities the cited sources state explicitly. Panel (a) shows the power level at which each design was validated, on a logarithmic axis; the near-three-decade separation between the tabulated prototypes and the 101.25 kW simulation of this work is the principal result of the comparison. Panel (b) shows the efficiency each source reports, each entry plotted at the power level at which it is stated; only two tabulated entries report an efficiency, and together with this work, they span 93 % to 96.6 %, a range too narrow and too heterogeneous in operating point to order the designs meaningfully. Panel (c) shows the number of independently regulated outputs, the axis on which the multi-port claim of this work rests: three regulated rails from a four-gate-signal structure, matched in count only by the 200 W single-input three-output converter of [25].

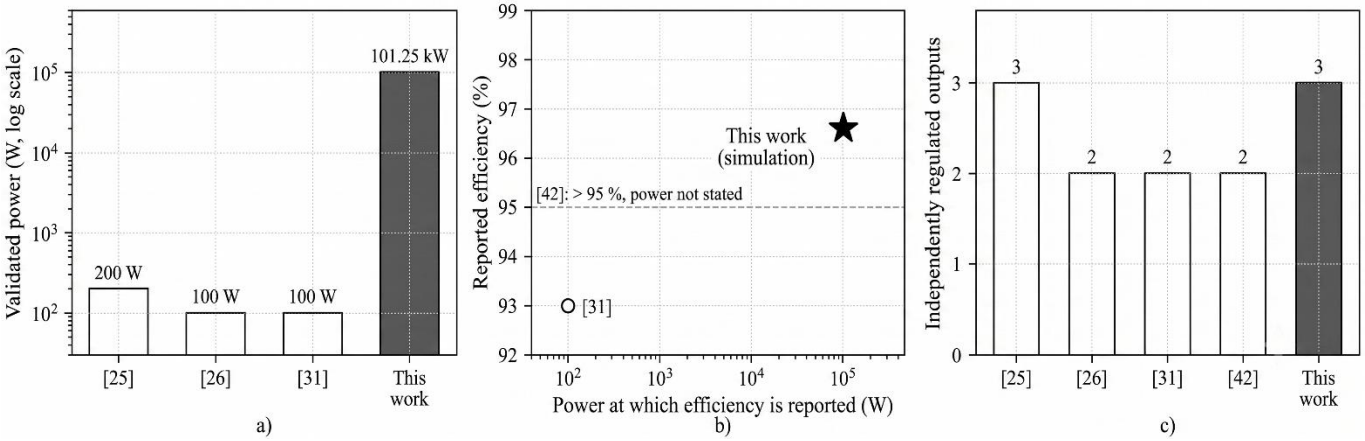


Fig. 11 Graphical comparison of the verified entries of Table 6, (a) Power level at which each design was validated, logarithmic axis, (b) Reported efficiency plotted at the power level at which each source states it, the dashed line marks the "greater than 95 %" figure of [42], for which no power level is reported, (c) Number of independently regulated outputs.
Shaded bars and the star mark the proposed converter, whose figures are simulation results.

10.4. Scope and Limitations of the Comparison

Six qualifications bound the comparison in Table 6. First, and most importantly, the power levels are not comparable: every tabulated design for which a power level is reported was validated between 100 W and 200 W, whereas all figures reported here are PLECS simulation results at 101.25 kW, so the comparison is a statement about the operating regime addressed and not a performance ranking. Second, the classes of evidence differ. Three of the four tabulated entries report hardware prototypes, whereas the present work has no hardware or hardware-in-the-loop validation; a simulated efficiency and a measured efficiency are not interchangeable quantities, and the entries are marked accordingly. Third, efficiency is reported at operating points chosen by each set of authors, and two of the four cited works report no efficiency figure at all. Fourth, the four-switch count quoted for this work refers only to the four actively gated SiC MOSFETs; the two external SiC Schottky diodes D_1 and D_2 and the upper-die body diode of the M_4 half-bridge module also conduct, but none of them consumes a gate signal, which is the strict comparison axis. Corresponding passive-device counts could not be verified for every tabulated entry and are therefore not compared. Fifth, none of the cited works reports a loss audit at the granularity of the 29 entries in Table 7, so the tabulated efficiency figures rest on methodologies that are not described in comparable detail. Sixth, the common-mode attenuation obtained in simulation, 41.7 dB at 200 kHz (Section 9.3), does not meet the 44 dB budget required for CISPR 25 Class 5, so no electromagnetic-compatibility conformity claim is made for the design as simulated.

10.5. Component-Level Loss Audit

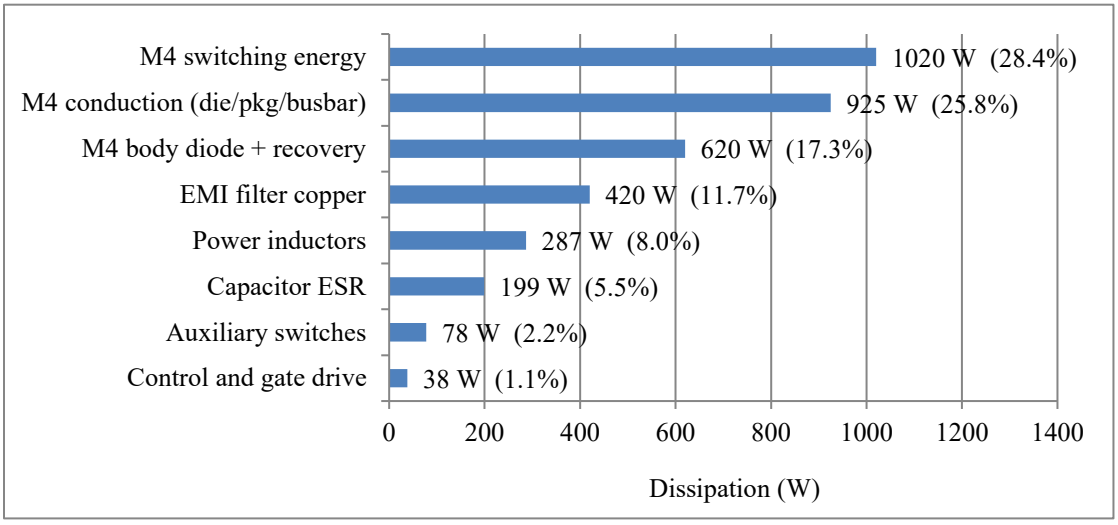
Table 7 presents the 29-entry loss audit that closes the global power balance to 3 587 W at the 101.25 kW operating point, giving the headline efficiency of 96.6 %. Entries 1 to 4 follow directly from the magnetic design of Section 4.5: both shared inductors carry the same 420 A pathway current and therefore dissipate the same 100 W of Litz copper loss each, while the 39 mT AC flux-density swing established in (37) fixes the core loss at 5.4 W per inductor. Entries 5 and 6 capture the dedicated buck inductors, entries 7 to 12 the SiC module losses (already discussed in Section 8.1), entries 13 to 19 the auxiliary-stage switching and conduction losses together with the two external Schottky freewheel diodes, entries 20 to 25 the capacitor ESR losses, entries 26 to 28 the EMI filter copper and dielectric losses, and entry 29 the gate-driver and control-electronics overhead.

Table 7. Component-level loss audit at 101.25 kW operating point

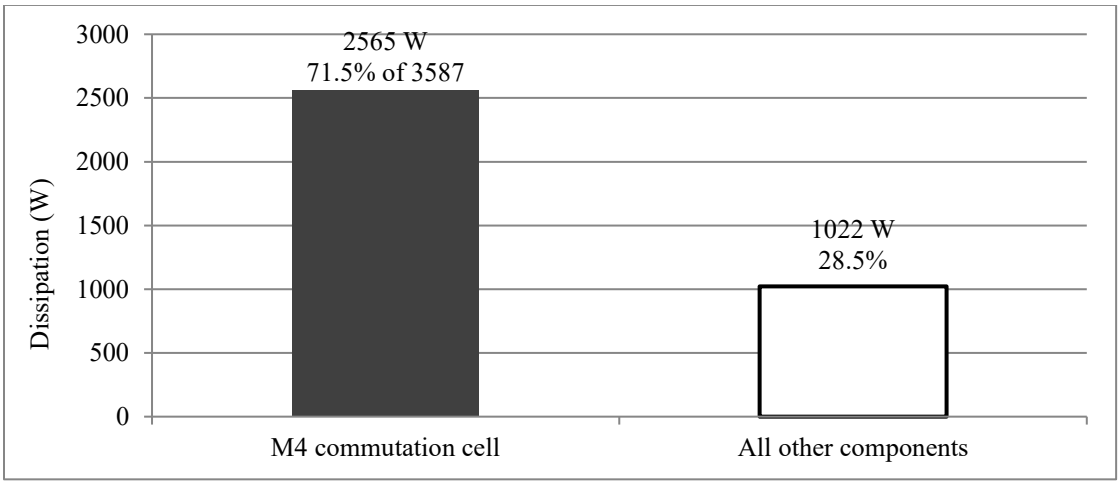
Sr.	Component / Loss Mechanism	Mechanism	Loss (W)	Comment
1	L1 (shared boost choke)	Cu	100	I_rms = 420 A, R_AC,eff = 0.565 mΩ
2	L1 core (Fe–Si 26 µ powder)	Core	5.4	B_pk,AC = 39 mT at 100 kHz, Equation (37)
3	L2 (shared boost choke)	Cu	100	I_rms = 420 A, R_AC,eff = 0.565 mΩ
4	L2 core (Fe–Si 26 µ powder)	Core	5.4	B_pk,AC = 39 mT at 100 kHz, Equation (37)
5	L3 (12 V buck)	Cu+Core	34	Includes both contributions
6	L4 (24 V buck)	Cu+Core	42	Includes both contributions
7	M4 lower die	Cond	422	R_DSon @ 175 °C, I_rms = 259 A
8	M4 package	Cond	215	R_pkg = 3.2 mΩ
9	M4 busbar	Cond	288	R_bus = 4.3 mΩ
10	M4 turn-on	Sw	644	E_on linearised to 400 V / 420 A
11	M4 turn-off	Sw	376	E_off linearised to 400 V / 420 A
12	M4 upper-die body diode	Cond+RR	620	V_F = 2.4 V, includes RR
13	M3 (24 V buck)	Cond	12	100 V SiC MOSFET, I_rms = 42 A
14	M3 switching	Sw	18	f_sw = 100 kHz, ZVS partial
15	M1 (12 V series)	Cond	8	60 V SiC, I_rms = 21 A
16	M2 (12 V series)	Cond	8	60 V SiC, I_rms = 21 A
17	M1/M2 switching	Sw	16	Combined
18	D2 — external 24 V freewheel	Cond	9	External Schottky
19	D1 — external 12 V freewheel	Cond	7	External Schottky
20	C1 (V1 input)	ESR	18	Polymer Al, 8 mΩ ESR
21	C2 (V2 input)	ESR	62	Polymer Al, 1.6 mF / 60 A RMS
22	C3 (400 V output)	ESR	94	Film + ceramic stack, 220 µF
23	C4 (12 V output)	ESR	8	Ceramic, 470 µF

24	C5 (24 V output)	ESR	11	Ceramic + polymer, 220 µF
25	Y/X-cap leakage	ESR	6	EMI Y/X-caps at 50 °C
26	CM choke Cu (L_CM1, L_CM2)	Cu	144	Series of two-stage CM filter
27	DM choke Cu (L_DM1, L_DM2)	Cu	264	V2-side custom busbar inductors
28	Filter X/Y-cap dielectric	Diel	12	Frequency-domain summation
29	FPGA + gate drivers + sensing	Aux	38	Includes isolated supplies
	Total dissipation		3 587	P_out = 101.25 kW → η = 96.6 %

Figure 12 presents the same audit graphically. Panel (a) collapses the twenty-nine entries into eight physical mechanisms sorted by magnitude. The three M_4 mechanisms occupy the first three positions: switching energy accounts for 1 020 W (28.4 %), conduction through die, package and busbar for 925 W (25.8 %), and the upper-die body diode, including reverse recovery for 620 W (17.3 %). The two-stage EMI filter contributes 420 W (11.7 %), and the four power inductors 287 W (8.0 %), while capacitor ESR, the auxiliary switches, and the control electronics together account for less than 9 % of the budget. Panel (b) states the consequence directly: the M_4 commutation cell alone dissipates 2 565 W, or 71.5 % of the 3 587 W total. The efficiency of this topology is therefore governed almost entirely by one device, which is what justifies the single-module SiC half-bridge selection of Section 8 and identifies the reverse-recovery and turn-on energy of that module as the primary target for any further improvement.



(a)



(b)

Fig. 12 Graphical form of the twenty-nine-entry loss audit of Table 7, totalling 3 587 W. (a) Dissipation grouped into eight mechanisms, sorted by magnitude, (b) Share of the total attributable to the M_4 commutation cell.

10.6. Efficiency Curve and Performance Summary

Figure 13 plots the simulated efficiency across the full output-power range from 5 kW to 101.25 kW. The curve is generated from the Table 7 decomposition by holding the 475 W of load-independent loss (core loss, EMI filter copper and dielectric, gate drive, and control overhead) constant, scaling the 1 054 W of switching loss linearly with load current, and scaling the remaining 2 058 W of conduction and ESR loss with the square of load current. On that basis, the efficiency falls to 90.4 % at 5 kW, where the fixed contributions dominate, peaks at 97.1 % near 49 kW where the fixed and quadratic terms balance, and settles at 96.6 % at the 101.25 kW rating. The wide plateau above 40 kW is a direct consequence of the ability of FCS-MPC to maintain $f_{sw} \approx 100$ kHz over a 5:1 load swing without the carrier-frequency hunting that classical hysteretic and PWM-PI controllers exhibit. Table 8 juxtaposes each target specification against the corresponding closed-loop result.

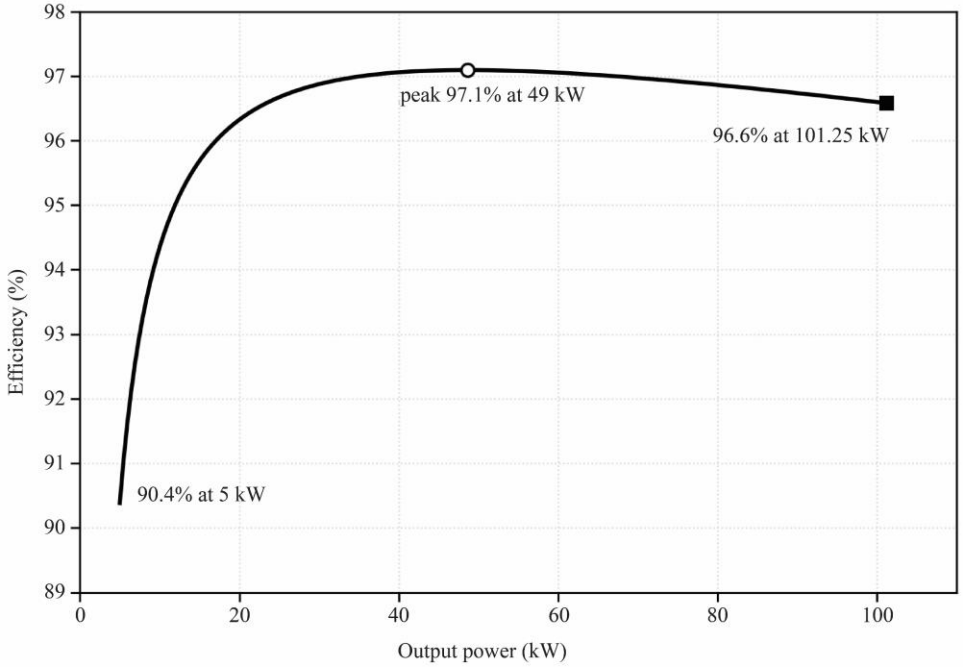


Fig. 13 Simulated efficiency versus output power. Full-load efficiency is 96.6 % at 101.25 kW, the light-load roll-off is set by the load-independent core, filter, and control losses of Table 7

Table 8. Performance Summary - Target Specification vs. PLECS Result

Metric	Target	PLECS Result
400 V regulation band	±500 mV	±350 mV
24 V regulation band	±50 mV	±24 mV
12 V regulation band	±25 mV	±17 mV
Efficiency at 101.25 kW	≥ 96.0 %	96.6 %
DRR (400 → 12 V) at 1 kHz	≥ 25 dB	32.6 dB
Reaching time to ε = 0.484	≤ 50 µs	30 µs
Lyapunov rate ρ per Ts	≤ 0.90	0.78
CM filter atten. @ 200 kHz	≥ 44 dB	41.7 dB (not met)
M4 junction temperature	≤ 200 °C	166 °C
FPGA compute time / sample	≤ 7 µs	5.58 µs

11. Conclusion

This paper has presented the design, modeling, and predictive regulation of a non-isolated six-port DC–DC converter that delivers 100 kW of 400 V traction power alongside 1 kW of 24 V auxiliary supply and 250 W of 12 V housekeeping using only four MOSFETs driven by four independent gate signals. The topology pools three input sources - a 98 V auxiliary input, a 200 V high-voltage battery pack, and a 48 V series-aid string - onto a shared boost inductor pathway, and dedicates two auxiliary inductors to the buck stages. A six-state discrete-time MIMO model, Tustin-discretized at $T_s = 10$ µs, drives a single-step finite-control-set predictive controller that enumerates sixteen physically realizable switching combinations per sample, selects the one minimizing a weighted quadratic tracking-cost function under inductor-saturation and capacitor-voltage constraints, and exploits its enumeration freedom to interleave the four switches in a manner that reduces the V_2 bulk capacitor RMS

current by 35 % relative to uniform-phase analysis. A discrete-time Lyapunov certificate in normalized tracking-error coordinates establishes a worst-case ultimate-bound radius of $\delta_\infty \leq 0.484$ and a geometric per-sample convergence rate of $\rho \approx 0.78$ under a disturbance budget $\delta_{max} \leq 0.051$, with three per-loop certificates closing comfortably below half-scale. PLECS time-domain simulation confirms 400 V regulation within ±350 mV under a 250 A traction-bus step, a 32.6 dB cross-port disturbance rejection ratio at 1 kHz, a 96.6 % efficiency at the 101.25 kW operating point established by a 29-entry component-level loss audit, and 41.7 dB of common-mode attenuation at 200 kHz. The last figure falls 2.3 dB short of the 44 dB budget required for CISPR 25 Class 5, so conducted-emission conformity remains to be secured by additional filter margin and confirmed by measurement. The single-module SiC half-bridge implementation of M_4 consolidates the boost-switch and freewheel-rectifier functions into one thermally coupled package, with a calculated junction temperature of 166 °C under worst-case load, leaving 34 K headroom below the 200 °C rating. A comparison with four multi-port EV converters reported between 2022 and 2026 shows that every tabulated design for which a power level is stated was validated between 100 W and 200 W, so the present work addresses a power class roughly three orders of magnitude above them rather than claiming a performance ranking against them. Future work will pursue hardware-in-the-loop and full prototype validation of the simulation results presented here, extend the FCS-MPC to a longer prediction horizon ($N_p \geq 5$) to improve disturbance rejection across the auxiliary outputs, and explore an 800 V variant of the same topology built from a dual-stack of two of the present modules to support next-generation EV traction architectures.

Conflicts of Interest

On behalf of all authors, the corresponding author states that there is no conflict of interest.

Funding Statement

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References

[1] Sajib Chakraborty et al., "DC-DC Converter Topologies for Electric Vehicles, Plug-in Hybrid Electric Vehicles and Fast Charging Stations: State of the Art and Future Trends," *Energies*, vol. 12, no. 8, pp. 1-43, 2019. [CrossRef] [Google Scholar] [Publisher Link]

[2] M.S. Hossain Lipu et al., "Review of Electric Vehicle Converter Configurations, Control Schemes and Optimizations: Challenges and Suggestions," *Electronics*, vol. 10, no. 4, pp. 1-37, 2021. [CrossRef] [Google Scholar] [Publisher Link]

[3] Rejaul Islam, Sajjad Hossain Rafin, and Osama A. Mohammed, "Comprehensive Review of Power Electronic Converters in Electric Vehicle Applications," *Forecasting*, vol. 5, no. 1, pp. 22-80, 2022. [CrossRef] [Google Scholar] [Publisher Link]

[4] Abhilash Sakhare, and Suresh Mikkili, "Advanced DC–DC Converter Topologies for Electric Vehicles: Wide Bandgap Technologies, Emerging Trends and Future Challenges," *Electrical Materials and Applications*, vol. 2, no. 1, pp. 1-41, 2025. [CrossRef] [Google Scholar] [Publisher Link]

[5] Md Safayatullah et al., "A Comprehensive Review of Power Converter Topologies and Control Methods for Electric Vehicle Fast Charging Applications," *IEEE Access*, vol. 10, pp. 40753-40793, 2022. [CrossRef] [Google Scholar] [Publisher Link]

[6] IImmanuel N. Jiya et al., "Multiport DC-DC Converter for Integrating Energy Systems in All-Electric Vehicles," *2023 IEEE International Conference on Electrical Systems for Aircraft, Railway, Ship Propulsion and Road Vehicles & International Transportation Electrification Conference (ESARS-ITEC)*, Venice, Italy, pp. 1-6, 2023. [CrossRef] [Google Scholar] [Publisher Link]

[7] R. Aravind et al., "Multi-Port Non-Isolated DC-DC Converters and Their Control Techniques for the Applications of Renewable Energy," *IEEE Access*, vol. 12, pp. 88458-88491, 2024. [CrossRef] [Google Scholar] [Publisher Link]

[8] Saikumar Bairabathina, and S. Balamurugan, "Review on Non-Isolated Multi-Input Step-up Converters for Grid-Independent Hybrid Electric Vehicles," *International Journal of Hydrogen Energy*, vol. 45, no. 41, pp. 21687-21713, 2020. [CrossRef] [Google Scholar] [Publisher Link]

[9] J. Narayanaswamy, and S. Mandava, "Non-Isolated Multiport Converter for Renewable Energy Sources: A Comprehensive Review," *Energies*, vol. 16, no. 4, pp. 1-25, 2023. [CrossRef] [Google Scholar] [Publisher Link]

[10] R. Aravind, Bharatiraja Chokkalingam, and Lucian Mihet-Popa, "A Transformerless Non-Isolated Multi-Port DC–DC Converter for Hybrid Energy Applications," *IEEE Access*, vol. 11, pp. 52050-52065, 2023. [CrossRef] [Google Scholar] [Publisher Link]

[11] Shahriar Farajdadian, Amin Hajizadeh, and Mohsen Soltani, "Recent Developments of Multiport DC/DC Converter Topologies, Control Strategies, and Applications: A Comparative Review and Analysis," *Energy Reports*, vol. 11, pp. 1019-1052, 2024. [CrossRef] [Google Scholar] [Publisher Link]

[12] Sunil Naik et al., "Comparative Analysis of Multi-Port DC-DC Converters for Electric Vehicle Applications," *2024 IEEE 4th International Conference on Sustainable Energy and Future Electric Transportation (SEFET)*, Hyderabad, India, pp. 1-6, 2024. [CrossRef] [Google Scholar] [Publisher Link]

[13] IIlham Shafini Ahmad Mahyudin et al., "Multiport DC-DC Converter Topologies for EV Systems: A Review of Architecture," *2025 9th International Conference on Man-Machine Systems (ICoMMS)*, Malacca, Malaysia, pp. 420-425, 2025. [CrossRef] [Google Scholar] [Publisher Link]

[14] Josep M. Olm et al., "Adaptive Control-Based Voltage Regulation of a Magnetically Coupled Multiport DC-DC Converter for Electrified Vehicles Applications," *2020 IEEE International Symposium on Circuits and Systems (ISCAS)*, Seville, Spain, pp. 1-5, 2020. [CrossRef] [Google Scholar] [Publisher Link]

[15] Ishita Biswas, Debaprasad Kastha, and Prabodh Bajpai, "Small Signal Modeling and Decoupled Controller Design for a Triple Active Bridge Multiport DC–DC Converter," *IEEE Transactions on Power Electronics*, vol. 36, no. 2, pp. 1856-1869, 2021. [CrossRef] [Google Scholar] [Publisher Link]

[16] S. Sankarananth, and P. Sivaraman, "Performance Enhancement of Multi-PORT bidirectional DC-DC Converter using Resilient Backpropagation Neural Network Method," *Sustainable Computing: Informatics and Systems*, vol. 36, 2022. [CrossRef] [Google Scholar] [Publisher Link]

[17] J. Sowmy, D. Arunkumar Mahindrakar, and N. Lakshminarasamma, "Modeling and Control of Single-Input, Multi-Output DC-DC Converters in Port-Controlled Hamiltonian Framework," *2024 IEEE 4th International Conference on Sustainable Energy and Future Electric Transportation (SEFET)*, Hyderabad, India, pp. 1-6, 2024. [CrossRef] [Google Scholar] [Publisher Link]

[18] Arkabrata Dattaroy, and Avik Bhattacharya, "An Aggregate of Novel Non-Isolated Four-Switch DCDC Converters with a Wide Voltage Conversion Ratio," *2024 IEEE 4th International Conference on Sustainable Energy and Future Electric Transportation (SEFET)*, Hyderabad, India, pp. 1-6, 2024. [CrossRef] [Google Scholar] [Publisher Link]

[19] Furkan Akar et al., "A Bidirectional Nonisolated Multi-Input DC–DC Converter for Hybrid Energy Storage Systems in Electric Vehicles," *IEEE Transactions on Vehicular Technology*, vol. 65, no. 10, pp. 7944-7955, 2016. [CrossRef] [Google Scholar] [Publisher Link]

[20] Bang Le-Huy Nguyen et al., "Family of Integrated Multi-Input Multi-Output DC-DC Power Converters," *2018 International Power Electronics Conference (IPEC-Niigata 2018 -ECCE Asia)*, Niigata, Japan, pp. 3134-3139, 2018. [CrossRef] [Google Scholar] [Publisher Link]

[21] Kazem Varesi et al., "Design and Analysis of a Developed Multiport High Step-Up DC–DC Converter with Reduced Device Count and Normalized Peak Inverse Voltage on the Switches/Diodes," *IEEE Transactions on Power Electronics*, vol. 34, no. 6, pp. 5464-5475, 2019. [CrossRef] [Google Scholar] [Publisher Link]

[22] Tohid Jalilzadeh et al., "Multiport DC–DC Converter with Step-Up Capability and Reduced Voltage Stress on Switches/Diodes," *IEEE Transactions on Power Electronics*, vol. 35, no. 11, pp. 11902-11915, 2020. [CrossRef] [Google Scholar] [Publisher Link]

[23] Duong Tran et al., "Optimized Multiport DC/DC Converter for Vehicle Drivetrains: Topology and Design Optimization," *Applied Sciences*, vol. 8, no. 8, pp. 1-17, 2018. [CrossRef] [Google Scholar] [Publisher Link]

[24] K. Suresh et al., "A Multifunctional Non-Isolated Dual Input-Dual Output Converter for Electric Vehicle Applications," *IEEE Access*, vol. 9, pp. 64445-64460, 2021. [CrossRef] [Google Scholar] [Publisher Link]

[25] Mudadla Dhananjaya et al., "A New Multi-Output DC-DC Converter for Electric Vehicle Application," *IEEE Access*, vol. 10, pp. 19072-19082, 2022. [CrossRef] [Google Scholar] [Publisher Link]

[26] Mudadla Dhananjaya et al., "Design and Implementation of Single-Input-Multi-Output DC-DC Converter Topology for Auxiliary Power Modules of Electric Vehicle," *IEEE Access*, vol. 10, pp. 76975-76989, 2022. [CrossRef] [Google Scholar] [Publisher Link]

[27] B. Karthikeyan et al., "A Dual Input Single Output Non-Isolated DC-DC Converter for Multiple Sources Electric Vehicle Applications," *Frontiers in Energy Research*, vol. 10, pp. 1-16, 2022. [CrossRef] [Google Scholar] [Publisher Link]

[28] Reddi Khasim Shaik, and C. Dhanamjayulu, "Synthesis and Implementation of a Multiport Dual Input-Dual Output Converter for Electric Vehicle Applications," *International Transactions on Electrical Energy Systems*, vol. 2022, pp. 1-15, 2022. [CrossRef] [Google Scholar] [Publisher Link]

[29] Pratim Bhattacharyya et al., "A Flexible Non-Isolated Multiport Converter to Integrate Battery and Ultracapacitor for Electric Vehicle Applications," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 70, no. 3, pp. 1044-1048, 2023. [CrossRef] [Google Scholar] [Publisher Link]

[30] Shaik Reddi Khasim, C. Dhanamjayulu, and S. M. Muyeen, "A Single Inductor Multi-Port Power Converter for Electric Vehicle Applications," *IEEE Access*, vol. 11, pp. 3367-3385, 2023. [CrossRef] [Google Scholar] [Publisher Link]

[31] Arvind R. Singh et al., "Design and Performance Evaluation of a Multi-Load and Multi-Source DC-DC Converter for Efficient Electric Vehicle Power Systems," *Scientific Reports*, vol. 14, pp. 1-18, 2024. [CrossRef] [Google Scholar] [Publisher Link]

[32] Jayamurugan Mookkan et al., "Novel Modular Buck-Boost Based Multiport Bidirectional DC–DC Converter (MPBC) for Hybrid Electric Vehicle Application," *IEEE Access*, vol. 13, pp. 45826-45845, 2025. [CrossRef] [Google Scholar] [Publisher Link]

[33] Ramana Manohar Reddy, Hemant Gupta, and Moumita Das, "Multioutput DC–DC Converter with Optimal Torque Distribution for Split Drive Electric Vehicle Applications," *IEEE Journal of Emerging and Selected Topics in Industrial Electronics*, vol. 6, no. 3, pp. 1166-1171, 2025. [CrossRef] [Google Scholar] [Publisher Link]

[34] Bussa Vinusha, Dharavath Kishan, and R Kalpana, "A Two Switch Multiport Non-Isolated DC–DC Converter for On-Board EV Charging Application," *2024 IEEE 4th International Conference on Sustainable Energy and Future Electric Transportation (SEFET)*, Hyderabad, India, pp. 1-6, 2024. [CrossRef] [Google Scholar] [Publisher Link]

[35] Amirreza Bahadori et al., "A Non-Isolated DITO High Step up DC/DC Converter with Reduced Voltage Stress on Power Switches," *Scientific Reports*, vol. 15, pp. 1-21, 2025. [CrossRef] [Google Scholar] [Publisher Link]

[36] Rameshbabu Sundarakamath, and Sudhakar Natarajan, "Integration of Multiple Sources for Fuel Cell Hybrid Electric Vehicles using Single Inductor Multi-Input Converter," *International Journal of Hydrogen Energy*, vol. 53, pp. 503-516, 2024. [CrossRef] [Google Scholar] [Publisher Link]

[37] Ji-Yeon Kim et al., "Integrated Multi Mode Converter with Single Inductor for Fuel Cell Electric Vehicles," *IEEE Transactions on Industrial Electronic*, vol. 69, no. 11, pp. 11001-11011, 2022. [CrossRef] [Google Scholar] [Publisher Link]

[38] Yuang Ma, and Wenguang Luo, "Research on the Integrated Converter and Its Control for Fuel Cell Hybrid Electric Vehicles with Three Power Sources," *Electronics*, vol. 14, no. 1, pp. 1-25, 2024. [CrossRef] [Google Scholar] [Publisher Link]

[39] Rakesh Thapliyal, Sourav Bose, and Prakash Dwivedi, "An Integrated Bidirectional Multi-Source DC–DC Converter with VMC Approach for VSI-Fed Motor Drive Using Non-Isolated Topology," *IEEE Transactions on Energy Conversion*, vol. 39, no. 2, pp. 1047-1058, 2024. [CrossRef] [Google Scholar] [Publisher Link]

[40] Ahmed Y. Farag et al., "Single-Stage Non-Isolated Multiport Y-Converter for Interlinking 400 V DC Microgrids with the Three-Phase AC Grid," *IEEE Open Journal of Power Electronics*, vol. 5, pp. 1432-1445, 2024. [CrossRef] [Google Scholar] [Publisher Link]

[41] Hazem H. Mostafa et al., "Multiport Bidirectional Converters for off Board Charging Stations of Electric Vehicles," *Scientific Reports*, vol. 15, pp. 1-27, 2025. [CrossRef] [Google Scholar] [Publisher Link]

[42] K. Suresh, E. Parimalasundar, and P. Aravind, "A High-Efficiency Multi-Port Bidirectional Converter for Renewable Energy and Hybrid Electric Vehicle Applications," *Scientific Reports*, vol. 16, pp. 1-27, 2026. [CrossRef] [Google Scholar] [Publisher Link]