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Original Article

Voltage-Booster for CMOS Wide-Band High-Precision Rectifier of Energy Harvesting for Implantable Medical Devices in Internet of Bodies (IOB) Telemedicine Embedded System

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Abstract *- This work proposes a new full-wave CMOS rectifier dedicated to wirelessly powered low voltage biomedical implants. It uses a diode Voltage Booster to Avoid Breakdown to maximize the higher wide-Band limit in the CMOS Rectifier for Energy Harvesting of Implantable Devices in a Telemedicine Embedded System. So, The rectifier topology now no longer requires a complicated circuit layout. It uses the best voltage to be had inside the circuit to force the gate of the chosen transistor, lowering present leakage day and lowering channel resistance even as showing excessive mutual conductance. The proposed rectifier at frequency 2.4 GHz has a two-stage structure with higher precision active diodes and diode voltage boosters in a typical 65nm CMOS process. The minimum working voltage is lower than in earlier publications, and the rectifier may be operated with input voltage amplitudes ranging from 0.2V to 4V before the Breakdown occurs. With this improvement, the rectifier can now function with various energy harvest systems such as vibrational energy harvest systems, electrostatic energy harvest systems, electromagnetic energy harvest systems, piezoelectric energy harvest systems, etc. The projected rectifier has a maximum voltage conversion efficiency (VCE) of more than 93.1 percent. A novel full-wave CMOS rectifier for low voltage wireless biomedical implants is described in this article.*

Keywords *– CMOS, Diode Voltage Booster, Breakdown Voltage, Wide-Band Rectifier, High Precision Rectifier, Energy Harvesting, Implantable Devices, Telemedicine, Internet of Bodies IOB, Embedded System.*

I. INTRODUCTION

A. Implantable Medical Devices & Telemedicine System

During surgery or other clinical procedures, implantable medical devices are put on the human body to accomplish specific activities. Artificial joints, breast implants, intrauterine devices (IUDs) for contraception, and bone, muscle, and joint fusion hardware are the most often utilized implanted medical devices. An implanted vascular access device is another form of implantable medical device commonly used by patients who have insufficient peripheral venous access or require regular venous access for treatment such as chemotherapy [1].

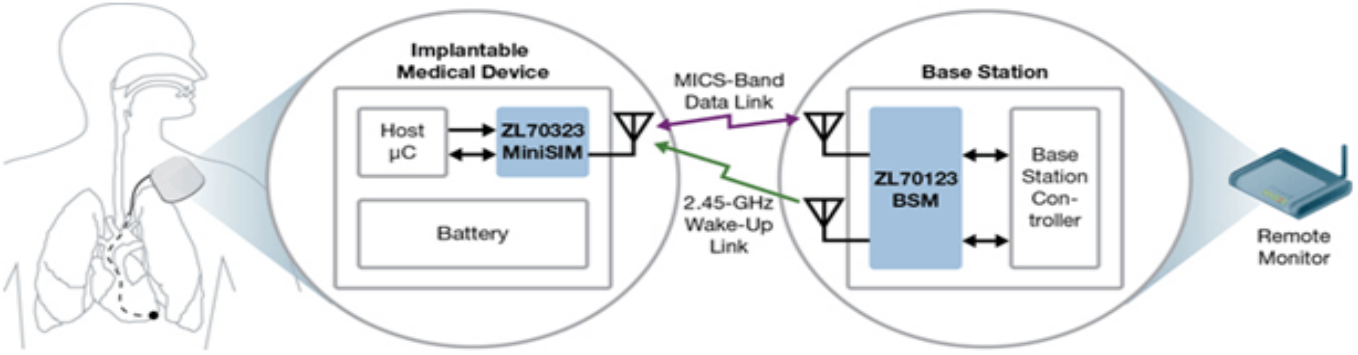

Fig. 1 Implantable medical devices & telemedicine system

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Active implanted medical devices, such as cardiac stimulators, are routinely used to treat heart problems. Patients with an implanted cardioverter-defibrillator (ICD), a battery-powered device put subcutaneously to measure heart rate, or a pacemaker, tiny battery-powered wireless, regular rhythm, have a pacemaker to manage their heart rhythm[2]. The implantable medical device that helps the heartbeat.

B. Internet of Bodies IOB

What is the body internet? And how can we change our lives? The Internet of Bodies (IoB) is an extension of the Internet of Things IoT that connects human frameworks to the community through devices that can be captured, embedded, or associated with frameworks in various ways. To do. Once the relationship is established, you can exchange records and remotely monitor and control frames and tools. The Internet of Bodies has three generations:

a) Body External

These are wearable devices made up of Apple Watch or Fitbits that can reveal our health.

b) Body Internal

This includes a pacemaker, cochlear implant, and virtual tablet. These are inserted into the body to detect or control various health factors.

c) Body Embedded

Internet of Bodies 0.33 technology is an embedded generation with a collective fusion of generations and the human body, with real-time connectivity to distant machines. Advances in WiFi connectivity, materials, and innovation expand implantable medical devices (IMDs) to run in many applications [3,4].

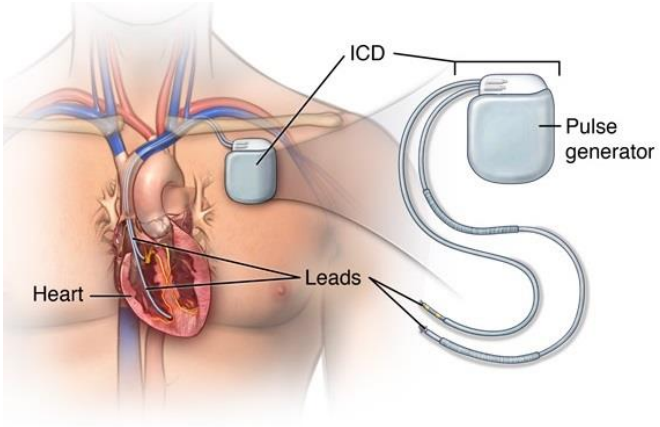


Fig. 2 Implantable cardioverter defibrillator ICD

A defibrillator or pacemaker is the most well-known example of the body's internet. This is a tiny device implanted in the abdomen or chest to assist patients with heart disease in controlling irregular cardiac rhythms by using electrical impulses, as shown in Figure 2. As shown in Figure 3, another IoB gadget is the "smart pill." These tablets have an edible electrical sensor as well as a computer chip. Once taken, these digital pills can gather data from our organs and transfer it to remote Internet-connected devices. Currently, the first digital chemotherapeutic agents are combined with healthcare providers (patients) equipped with chemotherapeutic agents and sensors to provide information on drug dosages and times and other rest and activity data. Collect, record and share. The security challenges facing the Internet of Things technology are similar to those that plague the Internet of Things. Still, with the involvement of IoT devices, they can have serious consequences.

In addition, IoB devices pose another cyber-security challenge that needs to be protected from hackers. Data protection is also of utmost importance. You must answer questions about who can access your data and why. A gadget that monitors health checks, for example, might also track unhealthy conduct. As the Internet of Bodies technology advances, regulatory and legal challenges must be addressed, and rules for responsible technology usage must be developed [4]. Figure 3 shows a “ Smart pill ” is another IoB device.

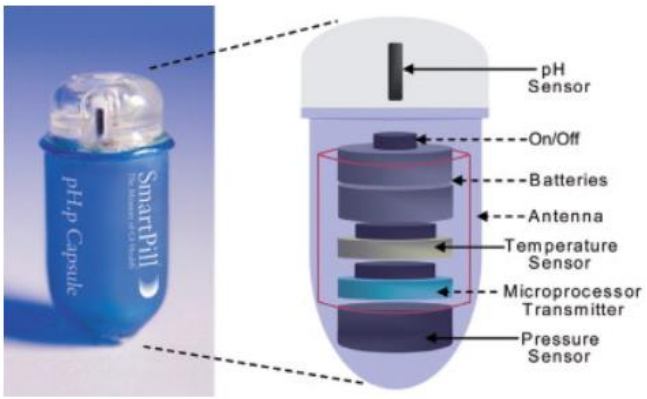


Fig.3. A “ smart pill ” is another iob device

C. Power Harvesting Challenges on Internet of Bodies IOB Implantable Medical Device

The Implantable Health Monitor continuously assesses multiple diseases and biomarkers and connects to the appropriate service providers and networks for real-time personal care may build. The following implantable monitors are most likely to be affected: glucose monitors, cardiac blood flow and composition monitors, human brown adipose tissue detection monitors, integrated photoelectric neuro-physiological probes, and selective biosensors (e.g.)[5-8].

The interface between the biomaterial and the sensor surface is important. For example, some prostheses are primarily bio-immobilized. Due to its biodegradability, operational and control functions are significantly reduced during the first two years. The stable fixation contacts a single nerve with minimal tissue damage, immune response, and signal noise. The ability to form microscale interfaces significantly reduces heterogeneous systems' variability, degradation, and functional degradation. If stability is not possible, the embedded nano-sensor can provide compensation over time. Other challenges include power generation, storage, and management, as shown in Figure 4. Maximizing the functionality of closed packaging and embedded subsystems, i.g. Sensing, signal processing, multiplexing, communication, and activation, as shown in Figure 5 [8-10].

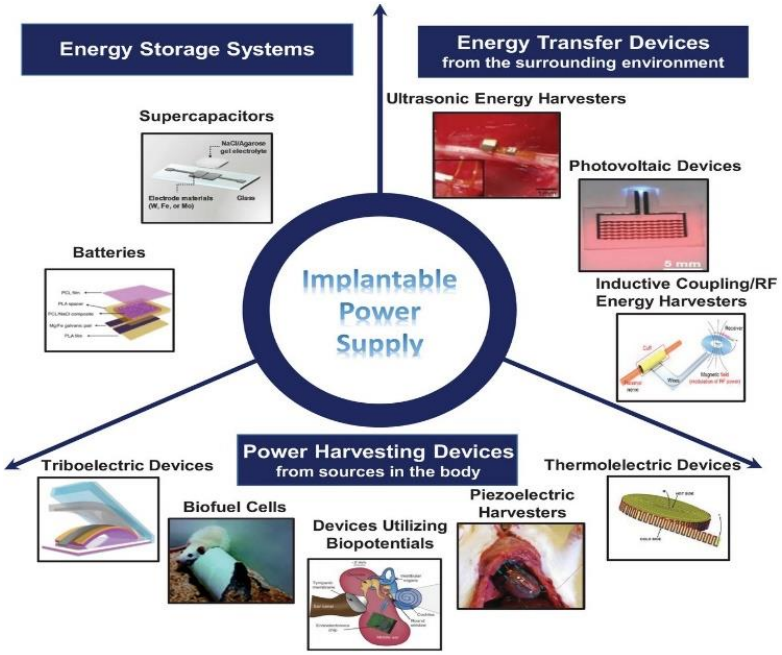


Fig. 4 Challenges of energy harvesting, storage, and management

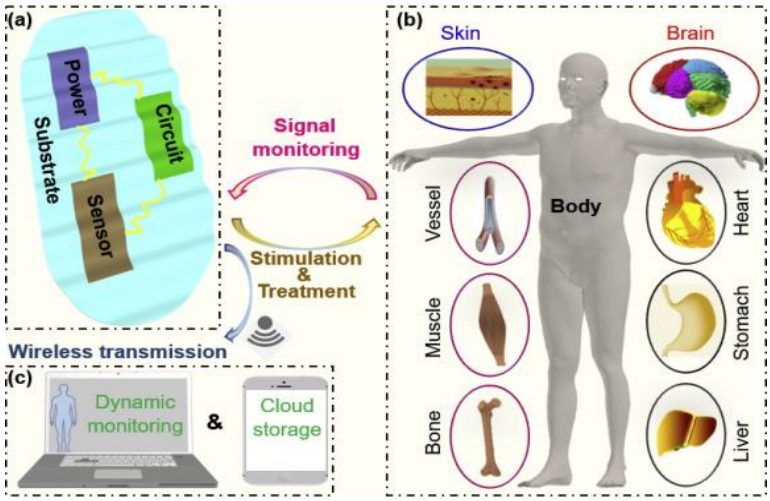


Fig. 5 Challenges of Sensing, signal processing, multiplexing, communication, and actuation

II. PRECISION CMOS WIDEBAND RECTIFIER FOR POWER GENERATION IN EMBEDDED MEDICAL DEVICES

The rectifier is intended to enhance power conversion efficiency PCE, focusing on input voltages less than 0.2V. A Schottky diode is used in this rectifier to convert the incoming AC signal to a DC voltage. Schottky diodes have been utilized to function across a wide frequency range [11]. In rectifier circuits, Schottky diodes produce high output voltage and efficiency. The forward voltage drop of Schottky diodes is smaller than that of pn junction diodes [12-14].

The most critical design difficulty in energy harvesting for embedded systems is creating an optimal CMOS rectifier circuit with moderate sensitivity and acceptable efficiency. Supply generation of WSN and RFID. Previous studies on CMOS rectifier analysis and efficiency improvement fall into four categories:

- Develop a mathematical model of the CMOS rectifier manufacturing procedure to utilize the model's insights to create an efficient harvesting system [13–17].
- Introduce various circuit strategies to ensure that the performance of traditional CMOS rectifiers is optimized, which is acknowledged as the basic core of CMOS rectifier circuits[18]; to give example, uses the Schottky diodes in the rectifier circuit to achieve low threshold voltage, while[19,20] uses native CMOS transistors with zero Vth to increase the sensitivity of total rectifiers; The fundamental disadvantage of these approaches is that they need a specific design procedure to produce Schottky diodes or native low Vth transistors, which boosts chip production costs because typical CMOS Fabrication processes do not incorporate Schottky Diode or native CMOS transistor; [21]describes an internal Vth cancellation (IVC) approach that uses the produced output voltage to increase the input impedance of rectifier circuit for connection to the matching network and compensation of diode threshold voltage; [22] compensates for the threshold voltage of the rectifier with an auxiliary battery and a battery voltage distributor in semi passive applications; on the other hand, it compensates for the threshold voltage of rectifier with an auxiliary rectifier chain; all these mentioned designs have been useful and could improve the performance of conventional rectifier circuits;
- In [23], the CMOS rectifier structure was introduced as a cross-coupled structure, and in [24], a self-suppression (SVC) approach was suggested. These structures can also enhance the manufacturing of rectifier circuits and the performance of existing rectifier circuits. It is worth mentioning that several researchers are now working on constructing these structures.
- The use of a structure with numerous transistors (3 to 15 transistors, for example) as a diode with almost optimal IV properties. The employment of these structures in half-wave and full-wave rectifiers increases rectifier circuit performance due to better IV characteristics [15, 16].

When implementing or constructing an optimal CMOS rectifier, it is critical to examine the structure and properties of the diode utilized in the rectifier. In other respects, the diode threshold voltage and forward bias current define rectifier performance, and the leak current in the reverse bias region is also essential for rectifier efficiency. Past research has attempted to create circuits that lower the rectifier diode's threshold voltage, minimize leakage current, and enhance forward current. [17,18]

The novel full-wave CMOS rectifier for low voltage wireless biomedical implants is described in this article. To tackle the difficulty of employing a cascade architecture where the voltage supply is restricted by the breakdown voltage of the common gate transistor, we suggest adopting self-bias technology as voltage-booster topology.

Due to self-bias technology for the common gate, the gate input voltage swing can increase the bias to more than 2Vdd. This means that you can increase the signal amplitude of the output before the CMOS device fails. The suggested rectifier was created with TSMC's standard 65nm CMOS technology. The total power efficiency may be enhanced by 11% when linked to a sine wave source with a peak amplitude of 3.3V, compared to the best results recently published in a gate cross-coupling-based structure.

IV. DIODE CONNECTED NMOS OR PMOS STRUCTURE

The rectifier circuit relies heavily on the diode-connected NMOS or PMOS transistor. Understanding the behavior of a diode-connected transistor can be aided by examining its IV characteristic. Before presenting the diode model, it is desirable to study the connection schematic of a standard diode-connected transistor, the IV curves, and the transistor's body influence on its leakage current and threshold voltage

Fig. 6(a) shows a typical diode connection of a MOS transistor. Also, Figure 6(b) shows that the IV curve is divided into four regions: collapse, posterior, subthreshold, and anterior [27]. The body effect can alter the threshold voltage of MOS transistors whose bulk is not linked to the source in the following ways:

$$Vth = Vtho + k1 * (\sqrt{\varphi s} + Vsb - \sqrt{\varphi s}) + k2 * Vsb \quad (1)$$

Where $k1$ and $k2$ are parameters that depend on channel doping. Vth is the threshold voltage of the transistor, $Vtho$ is the unique threshold voltage of the transistor, Vsb is the source bulk voltage of the transistor, and φs depends on CMOS technology.

The specifications required for a complete diode in a CMOS rectifier can be defined as follows: Suitable diodes for CMOS rectifiers require a low threshold voltage and a very low reverse leakage current. As a result, Figure 6 depicts the intended construction of a diode (diode-connected transistor) (a). The bulk is linked to the drain, not the source, as indicated in this diagram. Although CMOS technology does not differentiate between source and drain, we recommend attaching the ground to the terminal of the transistor that serves as the circuit's drain and shorting it to the diode's gate. When the proposed diode is forward biased, the transistor's source bulk voltage is negative, and the diode threshold is compared to a standard diode-connected MOS transistor in this area. The voltage will be negative. It will be low. This analysis is presented for transistors with diodes and can be extended to MIMO by inverting the voltage.

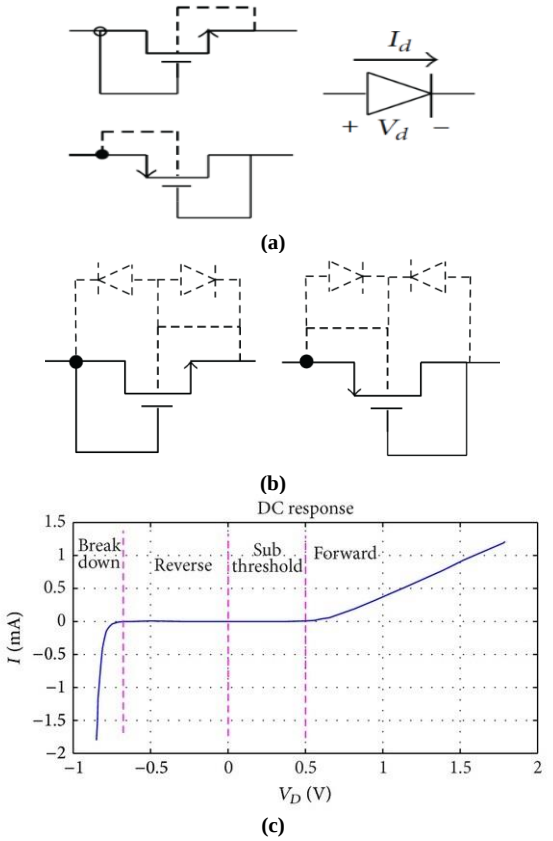


Fig. 6 A 65nm TSMC process specifications and standard IGMP transistor / L = 2 μm / 65nm. IV characteristic diodes showing the difference between (a) diode-connected MOS transistors, (b) unique PN junctions of MOS transistors, and (c) forward and reverse (leakage) currents between the proposed and conventional ones. Connection transistor [19-22].

The source bulk voltage is positive when the suggested diode is reverse biased; the diode reverses current is lowered compared to ordinary diodes. Fig. 6(b) depicts the unique PN junction between the MOS transistor's ground and drain/source. As seen in this image, when compared to the conventional diode in Fig. 6(c), the intrinsic forward bias of the PN diode increases the diode current where the PN diode is forward biased, reverse direction. A standard diode's PN junction, on the other hand, is forward-biased in this area.

As a result, in CMOS rectifier designs, the connections advised for most transistors can improve the performance of diode-connected MOS transistors. In conclusion, diode-connected MOS transistors are employed to enhance the IV properties of CMOS rectifier diodes. This diode works nicely in both forward and reverses directions. To lower leak currents and threshold voltages, use the unique bulk source or bulk drain PN junctions towards the preferred route. A single-stage conventional diode circuit rectifier is evaluated and compared to another conventional rectifier of the same kind. Optimal CMOS rectifier design, on the other hand, applies maximum efficiency optimization techniques. The rectifier is designed with TSMC 65nm CMOS technology using a cadence tool without additional masks.

The second suggested arrangement involves employing a diode-related MOSFET voltage-booster to raise entry voltage while preventing gate oxide breakdown. Improving the concept of voltage booster, we will imply resistive-diode voltage boosting that Fig.7 demonstrates. The wonderful swing of G2 may be made large compared to a poor swing. Wonderful voltage swing across deliver voltage is greater compared to poor swing. The circuit of Fig.7(a) is extra handy in this case, in which M1 and M2 have identical voltage swings on the gate-drain.

In conclusion, the Circuit works beneath neath output strength without inflicting overall performance degradation. By deciding on the fee of Rd and the scale of the diode-related transistor M3, we will specify the edge voltage at which the Rd-M3 begins off evolved undertaking and boosting the wonderful swing at G2. This greater step permits G2 to observe the upward push in D2 with a smaller attenuation than the autumn in D2. During this temporary response, the common fee saved on Cb will increase, inflicting Rd-M3 to behavior for a smaller percent of the obligation cycle. The common voltage at G2 will increase as much as the factor in which Rd-M3 does not conduct. Inconsistent state, the Rd-M3 course is off, and the wonderful and poor swings at G2 are equal. Fig.7(b) indicates the drain and gate voltages of transistor M2 as opposed to time for specific values of Rd. The voltage swing at D2 will now no longer be tormented by Rd, and the top-to-top swing of VG2 relies upon on Rd-Cb and now no longer Rb. Nevertheless, if the fee of Rd is reduced, the common voltage of VG2 will increase.

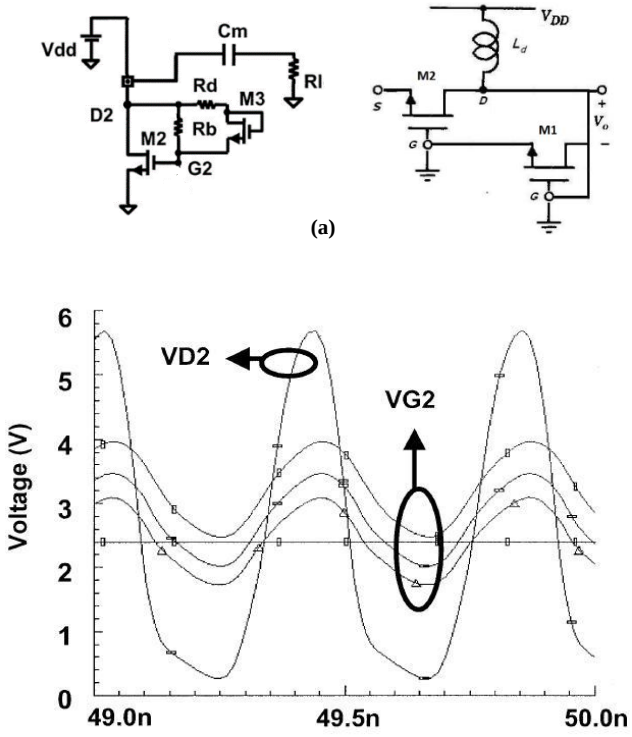


Fig. 7 (a) CMOS diode voltage (b) The voltage waveform VG2 is presented for three distinct source voltage levels.

The bootstrap cascode arrangement may be utilized in this scenario to achieve the same maximum voltage amplitude at the gate drains of M1 and M2. As a result, a greater supply voltage is used, and higher output power is generated.

V. PROPOSED WIDE-BAND RECTIFIER USING DIODE-VOLTAGE BOOSTER

Because of the need to increase the power conversion efficiency of the wideband rectifier using the proposed Diode Voltage Booster, for example, some WPT wireless power transfer systems operate in the ML frequency range[19-25]. When developing an optimal CMOS rectifier, it is critical to examine the structure and properties of the diode utilized in the rectifier. In other words, the diode threshold voltage and forward bias current are parameters that define rectifier performance, and the leak current in the reverse bias region is also essential in rectifier performance. All prior research attempted to create circuits that reduced the rectifier diode's threshold voltage and leakage current while increasing forward current [26-28].

A. Voltage Conversion Efficiency and Input Range

The suggested rectifier can operate across a wide range of input voltage amplitudes ranging from 0.45V to 1.95V, as shown in Fig.9. This is defined by the threshold voltage or breakdown voltage of the typical 65nm CMOS process. Fig.10 shows the confirmation of the breakdown voltage using the cadence tool. The wide input voltage range allows the rectifier to operate in different vibration energy harvesting systems.

As indicated in the equation, voltage efficiency is defined as the ratio of DC output voltage Vout to input voltage amplitude | Vin |. (2). Because the output voltage drop is significant, the rectifier's output voltage efficiency rises as the load resistance increases.

$$\eta_v = V_{out} / |V_{in}| \quad (2)$$

B. Power Efficiency of Rectifier is computed by

$$\eta_P = \frac{\int_{t_1}^{t_1+T} v_{out}(t) \cdot i_{out}(t)\, dt}{\int_{t_1}^{t_1+T} v_{in}(t) \cdot i_{in}(t)\, dt} 100\% \quad (3)$$

Here T is the input signal's period, and t1 is the start time. As R_Load increases, the current through the resistive load decreases and becomes less efficient as it approaches the current flowing through the comparator. A capacitance of 10uF and a load of 50k are employed since the load capacitor is adjusted to the applied frequency. The voltage efficiency at low frequencies is higher than at 1 kHz. Higher frequencies lead to comparator delays and increased reverse current. Nevertheless, this rectifier's working frequency range is enough for most applications at the frequencies of normal energy harvesting.

VI. DIFFERENTIAL CONTROL CMOS RECTIFIER WITH EXTERNAL BOOTSTRAP CIRCUIT

CMOS rectifier with external bootstrapping circuit During the input signal's amplitude, oxide breakdown occurred to MP2 (M5) when the amplitude was 4V.

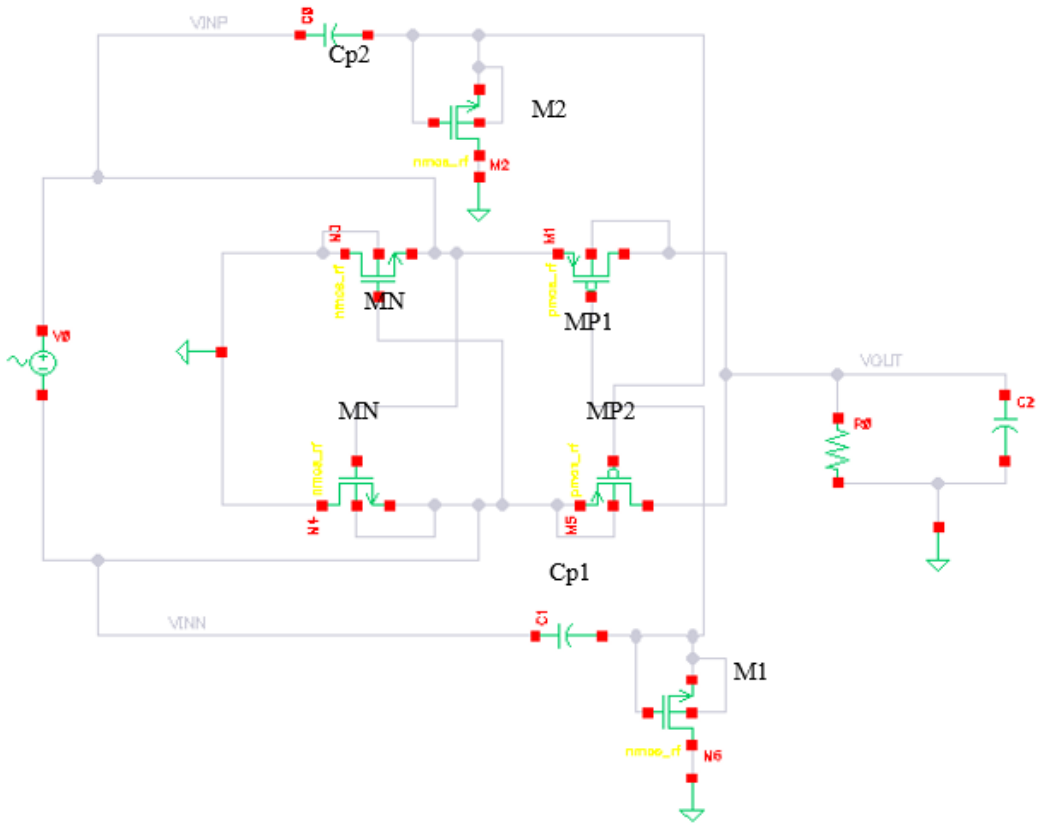


Fig. 9 Schematic View of Differential Drive

This is shown in Figure 10. The figure shows a warning message from cadence that there is a gate oxide breakdown to MP2 (M5).

```
Warning from spectre at time = 1.13487 ns during transient analysis `tran'.
    WARNING (CMI-2375): M5: Vgs has exceeded the oxide breakdown voltage of `vbox' = 6.6 V.
Notice from spectre at time = 1.16115 ns during transient analysis `tran'.
    M5: Device leaves the gate-source oxide breakdown region.
```

Fig. 10 Cadence warning message about gate oxide breakdown

Fig. 11 shows Simulation Results of breakdown voltage verification of standard CMOS process. From the warning message, we conclude that a gate oxide breakdown occurs at time = 1.13487 ns. Figure 3 shows the value of input voltage at this time, which is -3.946 V

The solution to the problem of gate oxide breakdown was to use a voltage booster sub-circuit which boosts the input to the transistor to avoid the Breakdown. The complete circuit is shown in Fig.12. The values of the resistances are both 1 kΩ, and the transistor size is 100 µm with a minimum channel length of 60 nm.

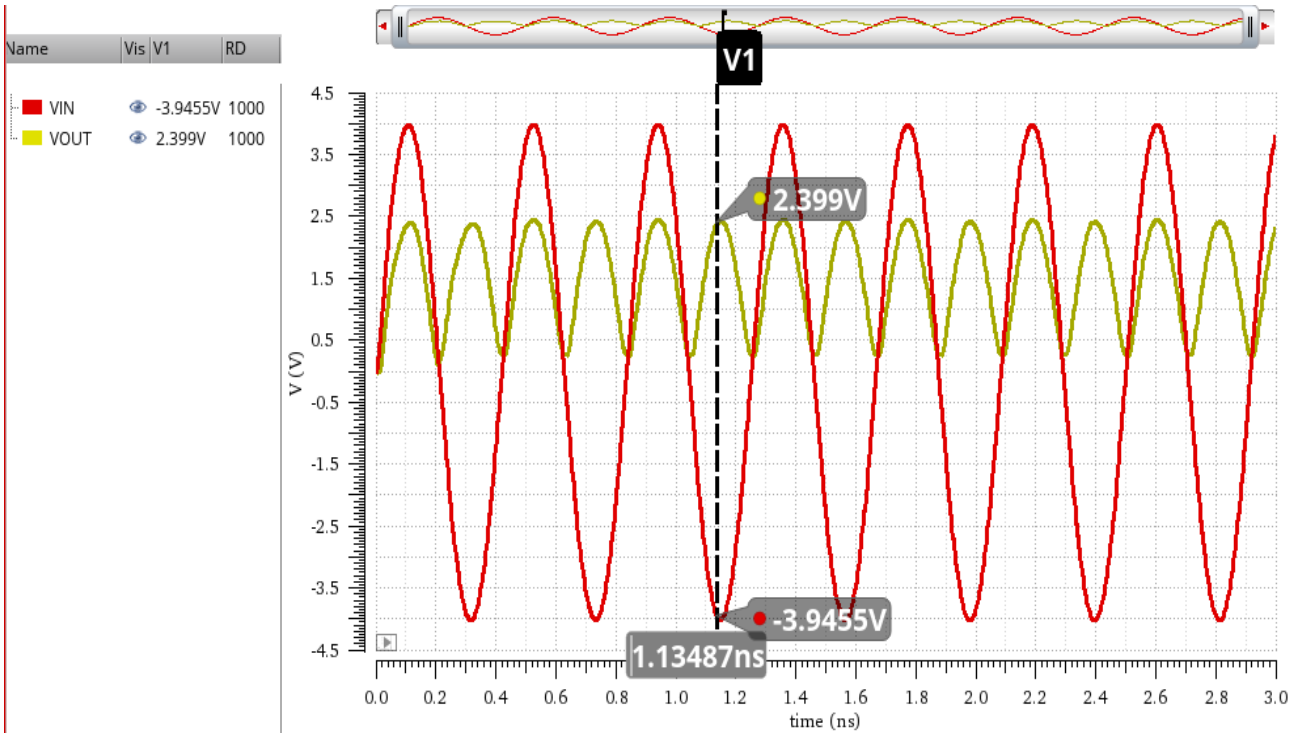


Fig. 11 The input voltage at which the gate oxide breakdown occurs

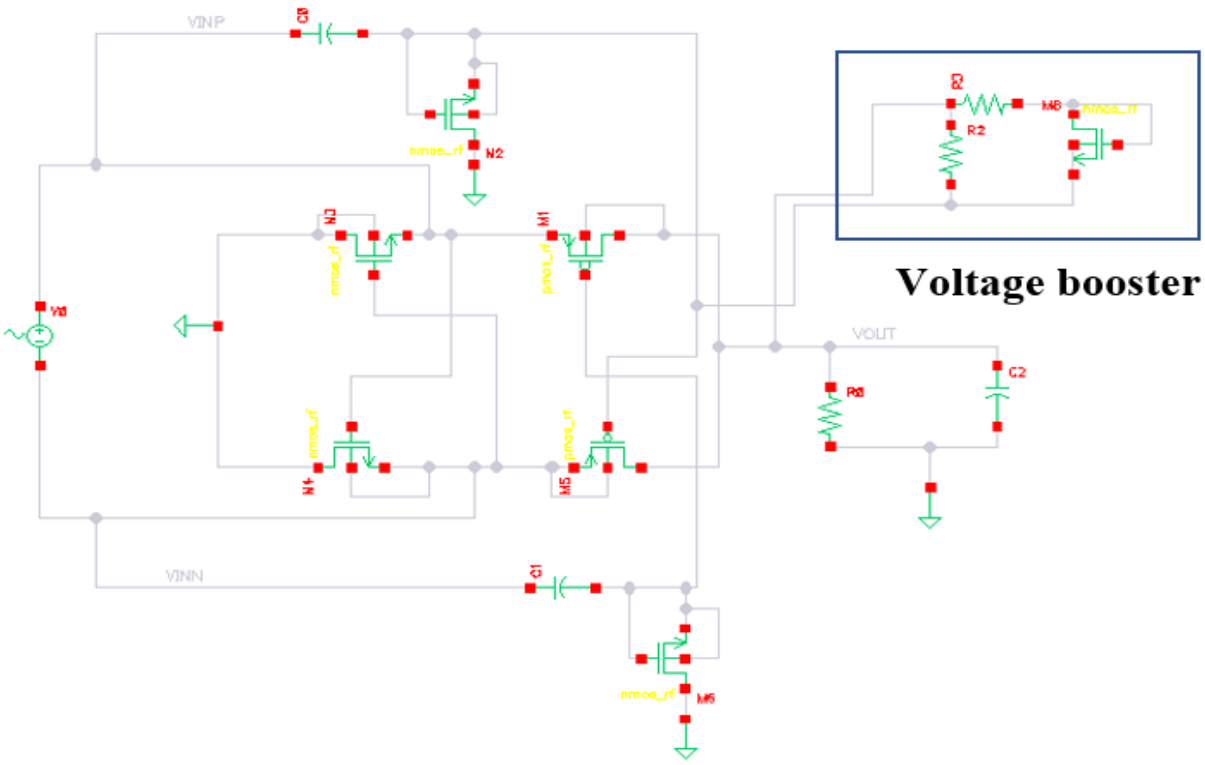


Fig. 12 Schematic View of Differential drive CMOS rectifier with an external bootstrapping circuit with a voltage booster circuit

After increasing the input voltage to an amplitude of 5V, the oxide breakdown occurs again, as shown in Fig 5. This states that the voltage booster is used to make the transistor accept a larger supply voltage.

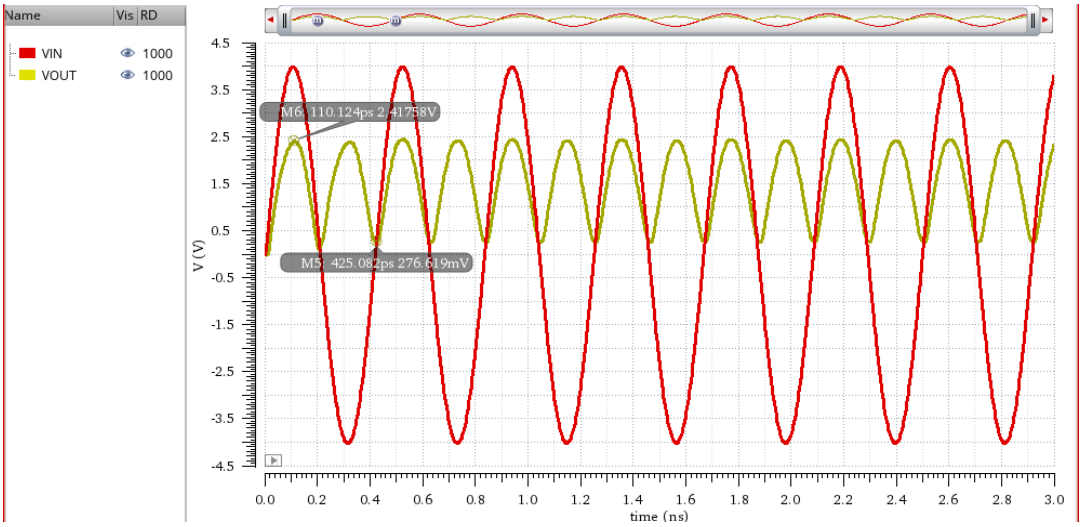
```
Warning from spectre at time = 1.09041 ns during transient analysis `tran'.
    WARNING (CMI-2375): M5: Vgs has exceeded the oxide breakdown voltage of `vbox' = 6.6 V.
        Further occurrences of this warning will be suppressed.
Warning from spectre at time = 1.11162 ns during transient analysis `tran'.
    WARNING (CMI-2377): M5: Vgd has exceeded the oxide breakdown voltage of `vbox' = 6.6 V.
        Further occurrences of this warning will be suppressed.
```

Fig. 13 Cadence warning message about gate oxide breakdown

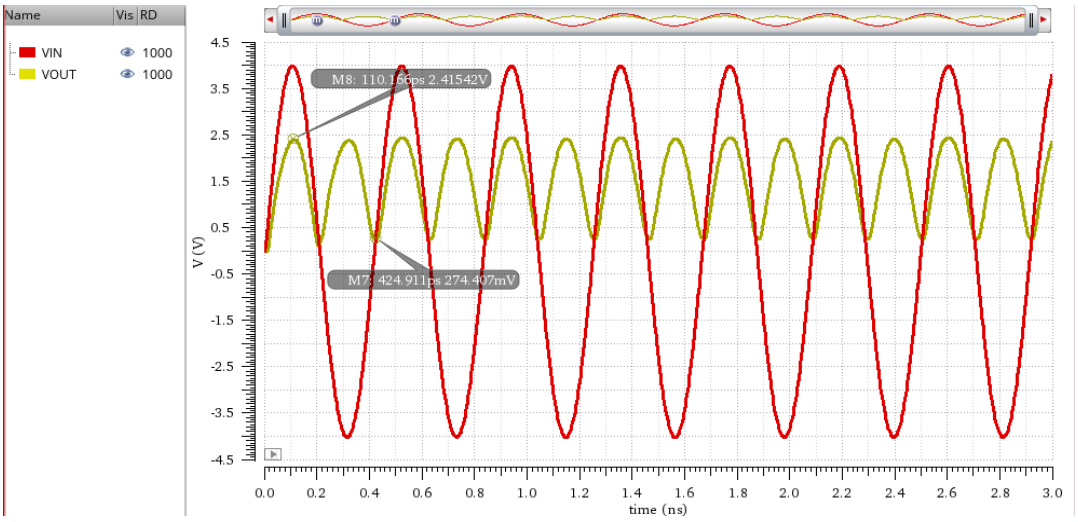
VII. DISCUSSION

A. Simulated Results

The results shown are for the original circuit and using a voltage booster circuit at a maximum input voltage of 4V. Figure 11 depicts a conventional 65nm CMOS process's breakdown voltage verification simulation results.

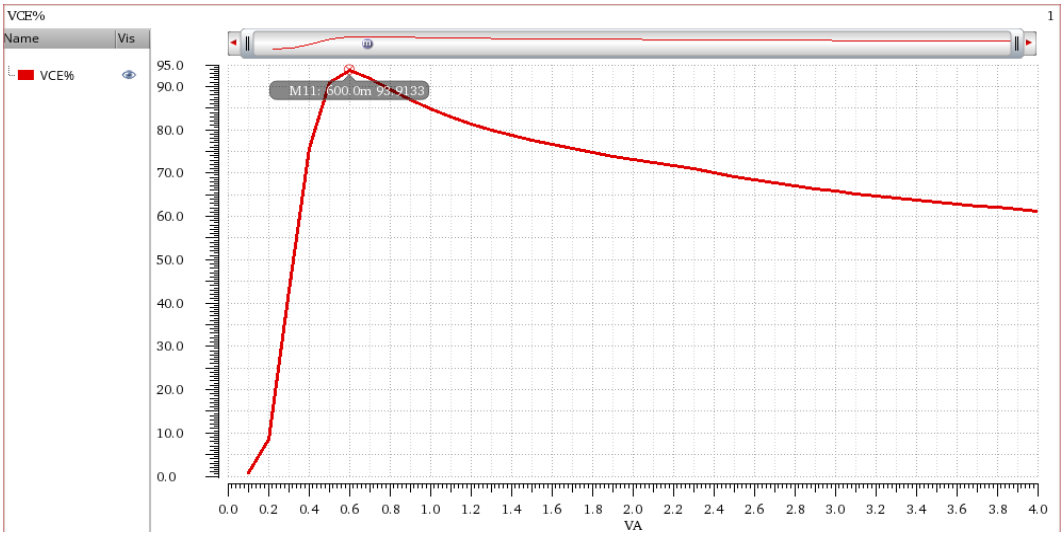


(a)



(b)

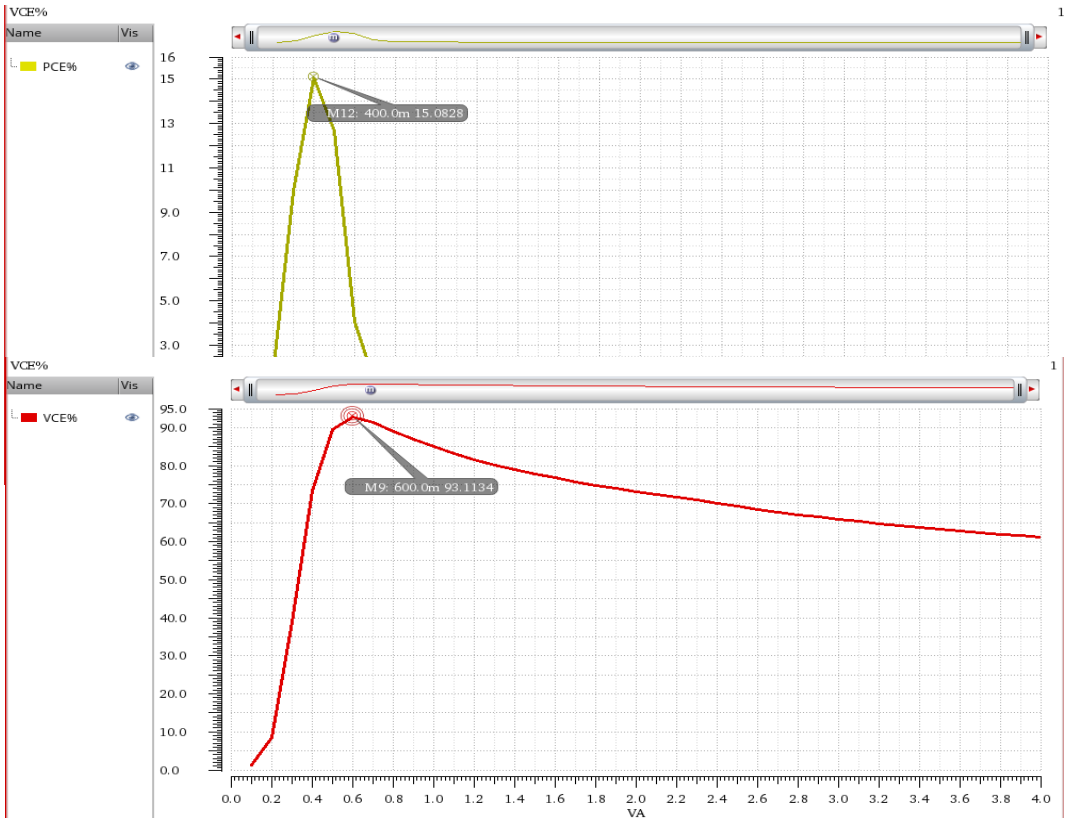
Fig. 14 Input and output waveforms at Freq = 2.4 GHz for (a) original circuit (b) with a voltage booster



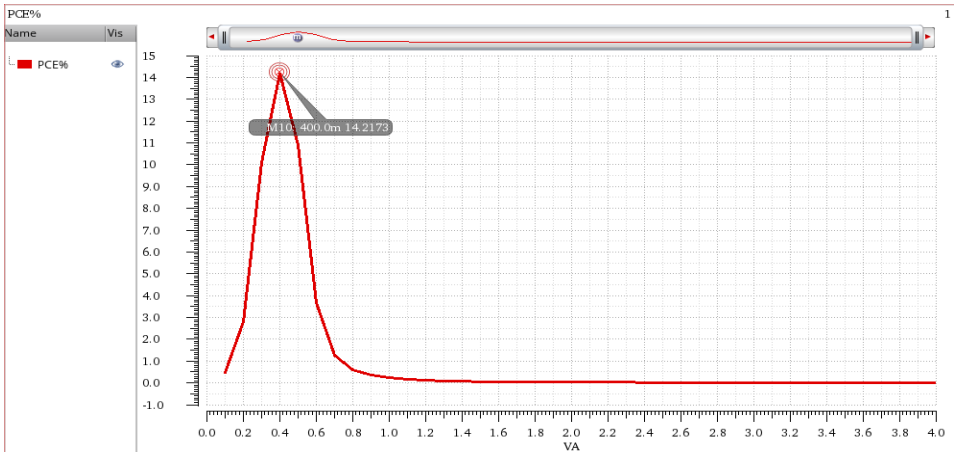
(a)

(b)

Fig. 15 VCE at F = 2.4 GHz for (a) original circuit (b) with voltage booster



(a)



(b)

Fig. 16 PCE at F = 2.4 GHz for (a) original circuit (b) with voltage booster

B. Performance Summary of FWFR CMOS Rectifier at F = 2.4 GHz:

The minimum and maximum output voltages generated using an input voltage amplitude of 4V are 0.27mV and 2.42V respectively, maximum VCE(Vout / |Vin |)= 93.1 % and maximum PCE (Pout / Pin) = 14.2 %.

C. Layout of the FWFR CMOS Rectifier

Fig. 17 shows the layout of the proposed voltage booster rectifier using 65nm COMS technology. The layout area is 0.117mm x 0.079mm=0.009mm^2, and The layout is built using cadence.

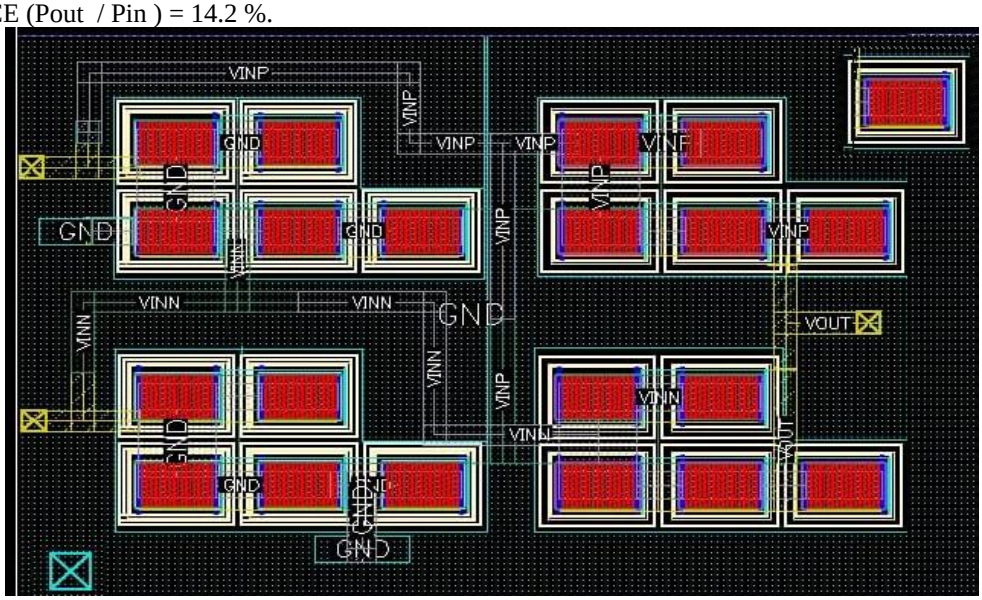


Fig. 17 Layout of proposed voltage booster rectifier using 65nm CMOS technology

VIII. Conclusion

When it comes to embedded electronic circuit design, the optimal energy harvesting design for the 65nm CMOS rectifier circuit is achieved by two designs. The first design reached the breakdown voltage of 2V. The second design reached breakdown Voltage at 4V. This means they achieve double voltage swing 2Vdd due to using a diode voltage booster. The proposed rectifier has a 2.4GHz operating frequency and has a two-stage structure with an increased precision active diode and diode voltage booster in a conventional 65nm CMOS process. The minimum functioning voltage is lower than in earlier articles, and the rectifier may run with input voltage amplitudes ranging from 0.2V to 4V before failure. As a result, the suggested rectifier may function with various vibration energy harvesters, electrostatic energy harvesters, electromagnetic energy harvesters, and piezoelectric energy harvesters. The suggested rectifier has a peak voltage conversion efficiency of more than 93.1 percent and a power efficiency of more than 14.2 percent. Because of its design, the rectifier may serve in various vibration energy collecting systems, including electrostatic energy harvesting, electromagnetic energy harvesting, and piezoelectric energy harvesting.

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