

Original Article

Design and Analysis of 2.45 GHz LNA at 60 nm CMOS Technology for Healthcare Applications

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Abstract - Low noise amplifiers are crucial for improving the sensitivity of receivers and maintaining signal integrity. Its primary function is to amplify weak signals received from antennas with minimal addition of noise. Using LNA on the receiver side enhances the overall performance of the communication system. This article presents the design and simulation of inductively degenerated common-source LNA at the frequency of 2.45 GHz. The proposed LNA is designed using three different topologies, Single Stage Cascode (SSC), Double Stage Cascode (DSC) and Differential Cascode (DIC), to analyze and identify the better-performing topology. The LNA is implemented with a 60 nm CMOS process. CMOS is used due to its low cost and easy integration. The proposed LNA is designed, and the Noise Figure and S parameters results of the proposed LNA are obtained using the QUCS software tool. The differential cascode topology is preferred comparatively for healthcare devices due to its precision, noise performance, and power efficiency. A unique advantage of the differential cascode topology is its superior common-mode noise rejection with high gain, which is particularly beneficial in environments with significant electrical noise. It is evident from the results that differential cascode topology provides comparatively better performance than the other two topologies. The differential cascode LNA achieves a Noise Figure (NF) of 0.0329dB, whereas an SSC of 438dB and DSC of 444dB. The input reflection coefficient of DIC is -0.559dB, whereas SSC is -5.44 e-13dB, and DSC is -5.42 e-13dB, the output reflection coefficient of DIC is 0dB, whereas SSC is -0.267dB, and DSC is -0.267dB and voltage gain of 67.8dB is achieved in DIC, whereas SSC is 231dB, and DSC is 231dB at the operating frequency.

Keywords - CMOS, Cascode, Common source, Differential, Low noise amplifier, Noise Figure, RF amplifier.

1. Introduction

LNA is the first building block of a receiver system [1]. The signals the receiver receives are comparatively weak (in the range of μV and nV). Therefore, using LNA is necessary to amplify the signal and improve the signal strength [2]. The number of radio frequency elements in wireless communication is increasing day by day, which leads to an increase in power consumption and noise. This shows the importance and need for improvement of LNA in wireless RF communication systems [3]. According to Friis's formula, in order to calculate the noise factor of cascaded stages, LNA establishes the overall Noise Figure (NF) [4]. LNA should have sufficient voltage gain to reduce the input-referred noise in RF receivers [5]. The input matching block, core amplifier, and output matching block are the three common stages of any LNA circuit [6].

The primary aim of any LNA is improving sensitivity and noise reduction using its cryogenic cooling technique. Inductive degeneration is a common source, cascade inductor source degeneration, shunt arrangement criticism is a common source, and some of LNA's major topologies [7]. The cascode

common source topology with inductive source degeneration has been widely used for implementing LNA due to its ability to provide input impedance matching, low power consumption, low NF, stability and high gain [5, 8]. The parameters that determine the performance of the LNA are Gain, Power consumption, Noise Figure, input-output impedance matching, linearity, etc. Among these parameters, the Gain and Noise Figure directly impacts the efficiency and signal-to-noise ratio of the entire system.

In this paper, an inductively degenerated common source low noise amplifier is designed under three different topologies (single-stage cascode, double-stage cascode and differential cascode) and with varying Q and power at the frequency 2.45 GHz for healthcare applications. The 2.45 GHz frequency band offers a balance between penetration depth, regulatory compliance, and power efficiency. 2.4 - 2.5 GHz is the frequency range reserved for scientific, industrial and medical radio purposes [4]. CMOS is used in this design due to its easy integration, low cost and better performance. A comparison table is made to identify the best topology in terms of quality factor (Q) and power that provide LNA with better



performance. In this design, an inductor is added to the drain to reduce the noise caused by the cascode transistors. The inductor at the drain can help provide high impedance at the desired operating frequency, which enhances signal gain and ensures proper impedance matching between the LNA and subsequent stages.

The inductive load resonates with the parasitic capacitances in the circuit, creating a high impedance at resonance. This boosts the gain at specific frequencies, improving overall amplification. Capacitive cross-coupling and adding an inductor at the gate of the cascode transistor are used to decrease the nonlinearity effect of the cascode transistors in a differential cascode structure [2].

Capacitive cross-coupling can help cancel out common-mode noise and signals, improving overall Noise Figure (NF). This is crucial in healthcare applications where minimizing noise is essential for accurate signal acquisition. It helps to balance the differential amplifier stages, improving overall stability and reducing phase errors that could otherwise degrade signal integrity. This paper is organized as follows: Section 2 describes the three basic topologies used in this paper. Section 3 explains the steps and formulas used to design the proposed LNA. Section 4 discusses and compares the simulation results for different topologies. Section 5 discusses and concludes the best topology for the LNA design.

2. Basic Topologies Used in this Work

2.1. Single-Stage Cascode Topology

In a basic single-stage cascode configuration, a Common-Source (CS) transistor and a Common Gate (CG) transistor are connected in series. The use of CS and CG transistors helps to improve the gain and linearity of the circuit. This configuration is widely used in Low-noise amplifier design, mixers, and IF and RF amplifier design. High gain, low output impedance, wide bandwidth and improved linearity are the major advantages of using this configuration. Despite its major advantages, the complexity of circuit construction using this configuration is high compared to basic single-stage amplifiers. Cost and power consumption are also relatively higher.

2.2. Double Stage Cascode Topology

Double-stage cascode topology is an extension of the single-stage cascode topology. This configuration is constructed by cascading two cascode configurations. In the first cascade, the series connection of the CS transistor and CG transistor is used. In the next or last stage, construction is similar to the first cascade stage, but the output of the first cascade stage provides the input for the second cascade stage. In addition to high gain, improved linearity and wider bandwidth, this configuration provides reduced noise. This configuration has similar applications and disadvantages to single-stage configuration.

2.3. Differential Cascode Topology

In a differential cascode topology, both the differential amplifier and cascode amplifier are used to improve the performance. Similar to the double-stage cascode configuration, two cascaded pairs in the differential configuration are used. The differential pair acts as an input stage, which consists of two transistors that are connected in a differential configuration. Among the two transistor gates, one gets the direct input signal, while the other gets the inverted form of the inverted signal. The Cascode stage acts as an output stage.

The cascode transistors in this stage are connected in series with the differential pair transistors and are in CG configuration. In addition to the advantages provided by the previous two topologies, this topology also provides a high Common-Mode-Rejection-Ratio (CMRR) and better Power Supply Rejection Ratio (PSRR). This configuration is used in the design of Operational Amplifiers, Low noise amplifiers and analog to digital converters. Using a differential cascode helps improve linearity, resulting in lower harmonic distortion. This is crucial for healthcare applications where the signal integrity must be maintained, especially in sensitive measurements like ECG or EEG.

Besides its enormous advantages, this topology also has a few limitations. Compared to single-stage or double-stage cascode designs, the differential cascode requires more components, leading to an increase in the complexity of design and layout. Due to the stacked nature of the cascode and differential operation, the voltage swing at the output can be limited compared to simpler topologies. This might restrict the dynamic range of the amplifier. Power consumption is slightly higher.

3. Design of Low Noise Amplifiers

The proposed LNA design is implemented using three different topologies (single cascode, double cascode and differential cascode) and with different quality factors (2, 3, 4, 5) and different power consumption (4W, 5W, 6W) for the desired frequency of operation 2.45 GHz. For the antenna to avoid reflection and achieve maximum power transfer, the proposed LNA should be impedance-matched with the outside environment. Equation (1) for the input impedance of the proposed LNA is given below.

$$Z_{in} = \frac{1}{sC_{gs}} + S(L_s + L_G) + \frac{gmL_s}{C_{gs}}$$

$$Z_{in} \approx \frac{1}{sC_{gs}} + S(L_s + L_G) + \omega_T L_s \quad (1)$$

The amplifier's input impedance should be purely resistive for antenna impedance to be purely resistive. To achieve that, it needs,

$$\omega_T L_S = R_S \text{ and } \frac{1}{C_{gs}(L_S+L_G)} = \omega_0^2 \quad (2)$$

Where, ω_0 is the desired frequency.

To calculate the optimum width of the LNA, Equation (3) is used.

$$W_{opt} = \frac{A_b}{2Q^2} \sqrt{\frac{5}{6} \frac{1}{\frac{4}{3}\omega_0 R_S C_{ox} L}} \quad (3)$$

Where, A_b is called the bulk charge factor, which is a constant around 1.2 – 1.4, Gate oxide capacitance is represented by C_{ox} (14 fF/ μm^2), L is the length of the transistor (60 nm), Q is the quality factor and resistance of the antenna is represented by R_S (50 Ω). The transconductance of the device is determined using Equation (4).

$$g_m = \sqrt{\frac{2}{A_b} \mu_{eff} C_{ox} \frac{W}{L} I_{ds}} \quad (4)$$

Where, μ_{eff} is the effective permeability (0.04), and I_{ds} is the drain to source current.

The optimum power can be calculated using the following Equation (5).

$$P_{opt} = \frac{C_{gs}}{C_t} = \frac{A_b}{2Q} \sqrt{\frac{5}{6}} \quad (5)$$

Where, C_{gs} is the intrinsic capacitance which is chosen as 15 fF.

To calculate the value of L_S and L_G , the following Equations (6) and (7) are used.

$$L_S = R_S \frac{C_t}{g_m} = \frac{C_{ex}+C_{gs}}{C_{gm}} \quad (6)$$

$$L_G = \frac{1}{\omega_0^2 C_t} - L_S \quad (7)$$

The remaining unknown load values, such as L_{tank} and R_{tank} are calculated using the Equations (8) and (9).

$$L_{tank} = \frac{1}{\omega_0^2 C_{tank}} \quad (8)$$

Where, C_{tank} is the representation of overall capacitance offered by the next stage, parasitic capacitance and explicitly

added capacitance at the load. Hence, the value of C_{tank} is chosen as 200 fF. The value of R_{tank} is only due to the finite Q value of L_{tank} , which is 10 in this case and is not an explicitly added resistor here.

$$R_{tank} = \omega_0 L_{tank} Q \quad (9)$$

The values of different components used in the circuit of LNAs are designed using the equations mentioned above and are listed in Table 1. The CMOS device of 60 nm technology is used for the design. The quality factor (Q) and bias current (I_{ds}) of the circuit are varied, and the corresponding component values are calculated.

4. Simulation and Result Analysis

The low noise amplifiers of three different topologies are designed in QucsStudio (Quite Universal Circuit Simulator). Qucs Studio offers an intuitive interface for easy circuit design and provides comprehensive tools for straightforward interpretation of simulation results. Each topology is designed for different quality factors (Q = 2, 3, 4, 5) and bias currents (I_{ds} = 4, 5, 6 mA) to study the effect of these parameters on gain and power consumption.

At first, the single-stage cascode circuit is designed and simulated, as shown in Figure 1. All the scattering parameters (S-parameters) that describe the input-output relations and noise figures are observed. Then the double cascode structure is designed as shown in Figure 2 and simulated to obtain S-parameters and noise figure. Finally, the differential cascode structure is designed as shown in Figure 3, followed by the simulation. A comparative analysis of three different topologies based on simulation results is done to decide the best one for RF applications.

The quality factor affects the S parameters related to the reactive components and bandwidth of the circuit. A higher Q factor leads to higher impedance, automatically affecting the input reflection coefficient. The output reflection coefficient is less affected by the Q factor. Generally, at a high Q factor, the resonance is sharp. At this condition, the transmission coefficient or gain will be very high at the resonant frequency but drops quickly outside the resonant frequency. The transmission coefficient will spread over a wide range of frequencies at a low Q factor, making the circuit less selective. In most cases, using a high Q factor leads to a low Noise Figure due to noise filtering and improved selectivity, whereas a low Q factor increases the Noise figure due to reduced selectivity.

Table 1. Designed values of different components used in the proposed LNA for varying Q and I_{ds}

Component	Q = 2, $I_{ds} = 4 \text{ mA}$	Q = 2, $I_{ds} = 5 \text{ mA}$	Q = 2, $I_{ds} = 6 \text{ mA}$	Q = 3, $I_{ds} = 5 \text{ mA}$	Q = 4, $I_{ds} = 5 \text{ mA}$	Q = 5, $I_{ds} = 5 \text{ mA}$
W	185.35 μm	185.35 μm	185.35 μm	82.403 μm	46.34 μm	29.67 μm
L	0.06 μm	0.06 μm	0.06 μm	0.06 μm	0.06 μm	0.06 μm
W_{cascode}	370.70 μm	370.70 μm	370.70 μm	164.81 μm	92.68 μm	59.34 μm
L_{cascode}	0.12 μm	0.12 μm	0.12 μm	0.12 μm	0.12 μm	0.12 μm
L_S	22.04 pH	19.72 pH	17.99 pH	44.34 pH	78.86 pH	123.17 pH
L_G	96.38 pH	96.38 pH	96.64 pH	64.22 pH	48.11 pH	38.44 pH
C_{exp}	38 fF	38 fF	38 fF	38 fF	38 fF	38 fF
C_{tank}	200 fF	200 fF	200 fF	200 fF	200 fF	200 fF
L_{tank}	21.12 nH	21.12 nH	21.12 nH	21.12 nH	21.12 nH	21.12 nH
R_{tank}	3.25 k Ω	3.25 k Ω	3.25 k Ω	3.25 k Ω	3.25 k Ω	3.25 k Ω

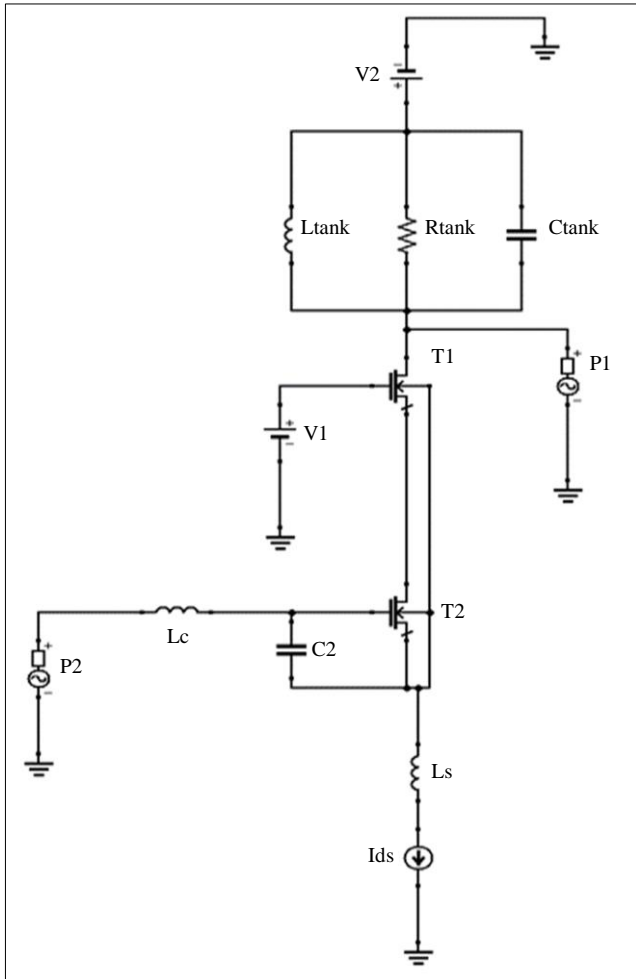


Fig. 1 Circuit diagram of single-stage cascode LNA

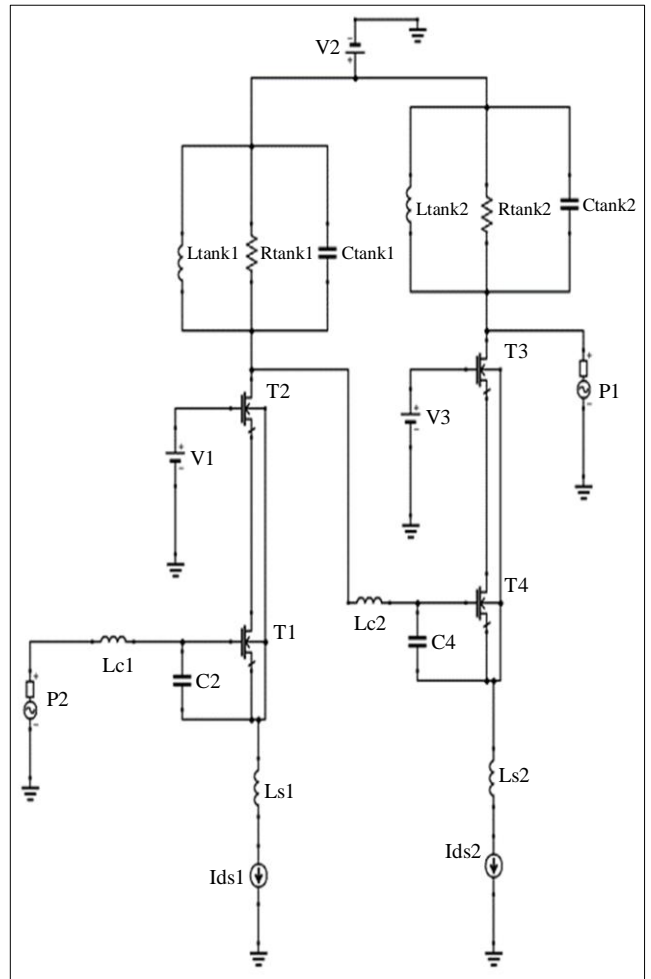


Fig. 2 Circuit diagram of double-stage cascode LNA

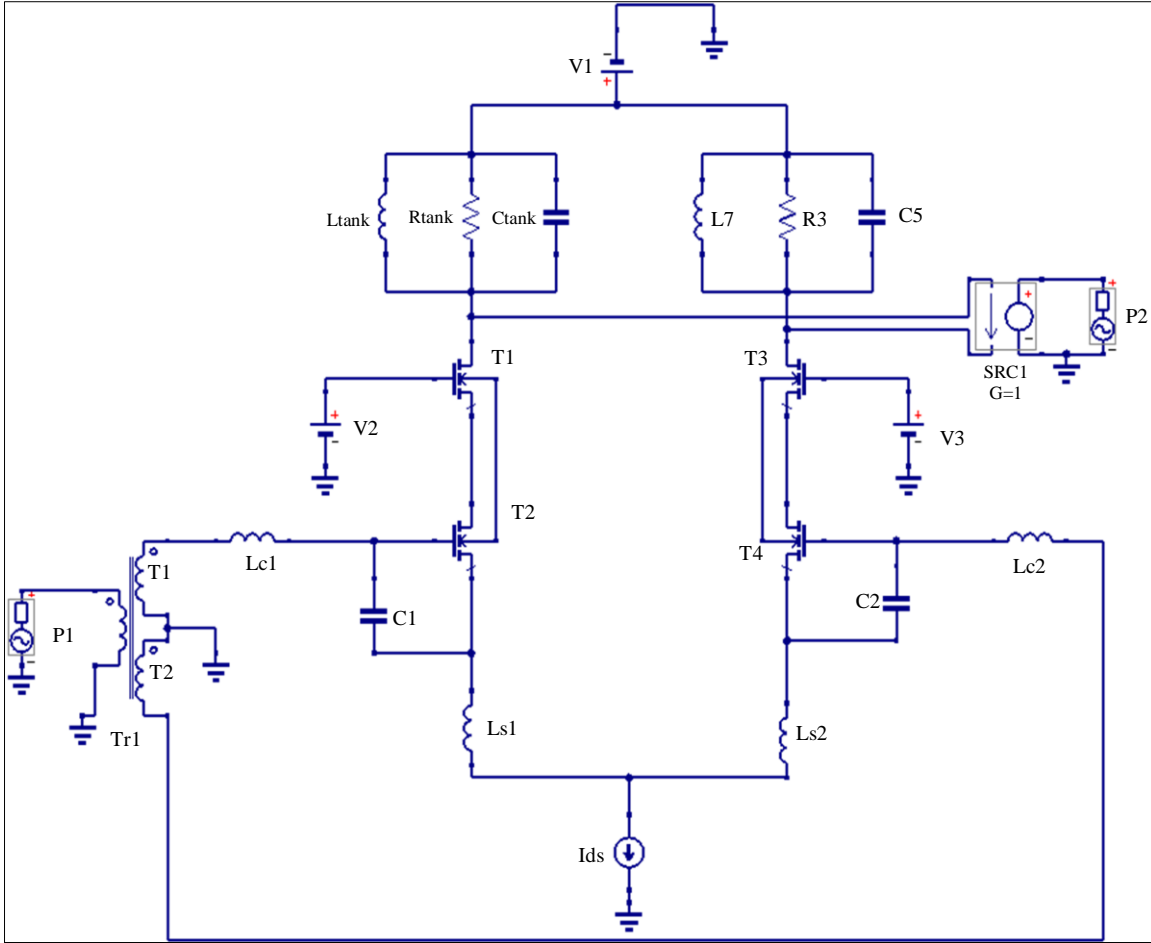


Fig. 3 Circuit diagram of differential stage cascode LNA

4.1. Scattering (S) Parameters

The Scattering parameter plots are obtained by performing the S parameter simulation in QucsStudio, and Equations (11 – 14) are used to obtain the corresponding values computed in terms of dB. The simulation is performed for the frequency range of 2 to 10 GHz.

$$A_1 = S_{11} B_1 + S_{12} B_2 \quad (9)$$

$$A_2 = S_{21} B_1 + S_{22} B_2 \quad (10)$$

Input Reflection co-efficient (S_{11}):

$$S_{11} = (A_1/B_1) \text{ at } B_2 = 0 \quad (11)$$

Reverse voltage gain (S_{12}):

$$S_{12} = (A_1/B_2) \text{ at } B_1 = 0 \quad (12)$$

Transmission or Forward voltage gain (S_{21}):

$$S_{21} = (A_2/B_1) \text{ at } B_2 = 0 \quad (13)$$

Output Reflection co-efficient (S_{22}):

$$S_{22} = (A_2/B_2) \text{ at } B_1 = 0 \quad (14)$$

4.1.1. Single Stage Cascode LNA

The S-parameters of the single-stage cascode LNA, such as input reflection coefficient (S_{11}), reverse voltage gain (S_{12}), transmission coefficient or forward voltage (S_{21}) and output reflection coefficient (S_{22}), are simulated by varying the frequency from 1 GHz to 10 GHz. In a single-stage cascode structure, the input reflection coefficient (S_{11} dB) plot is almost flat and without any dip across the frequency range, as S_{11} shows in Figure 4. It is close to zero (-5.44×10^{-13} dB at $Q = 2$ and $I_{ds} = 6$ mA) at the operating frequency of 2.45 GHz. An increase in the Q factor doesn't lead to a linear change in S_{11} . At $Q = 3$, S_{11} is more negative and at $Q = 5$, S_{11} is less negative. Even the increase in I_{ds} doesn't have much effect on S_{11} .

The reverse voltage gain (S_{12}) shown in Figure 5 is almost negative for the chosen frequency range. The transmission coefficient or Voltage gain is more negative (-0.231 dB at $Q = 2$ and $I_{ds} = 6$ mA) at the operating frequency, which is undesirable, as shown in Figure 6. Increasing I_{ds} negatively impacts the gain. Varying the Q factor doesn't have much impact on gain (except at $Q = 5$ and $I_{ds} = 5$ mA). The output reflection coefficient (S_{22} dB), as

shown in Figure 7, is negative (-0.267 dB when $Q = 2$ and $I_{ds} = 6$ mA) at the operating frequency. It is observed that S_{22} is constant for varying Q factors and I_{ds} .

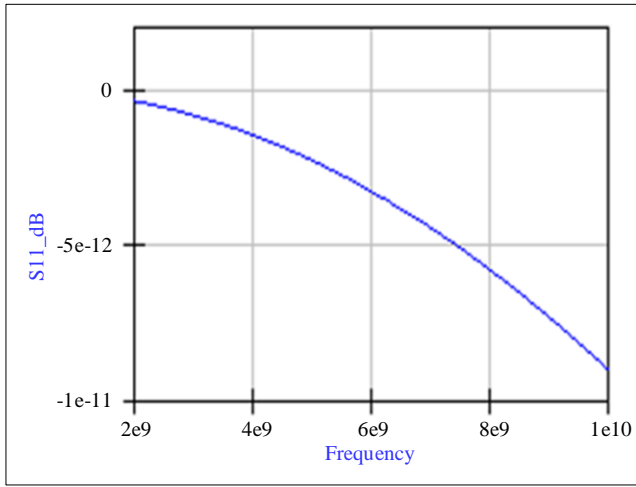


Fig. 4 Input reflection co-efficient (S11) in single cascode LNA

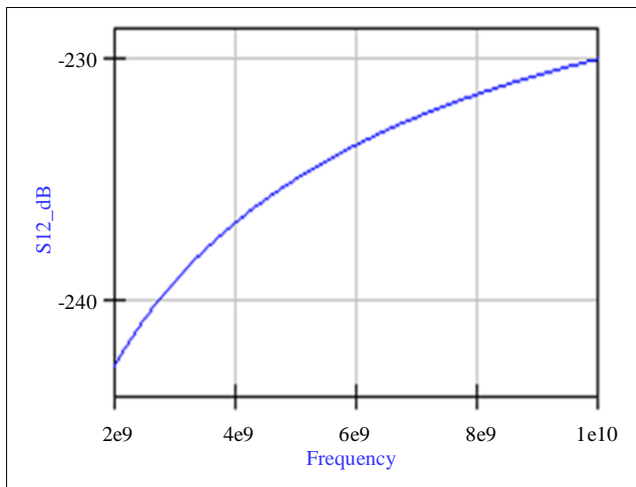


Fig. 5 Reverse voltage gain (S12) in single cascode LNA

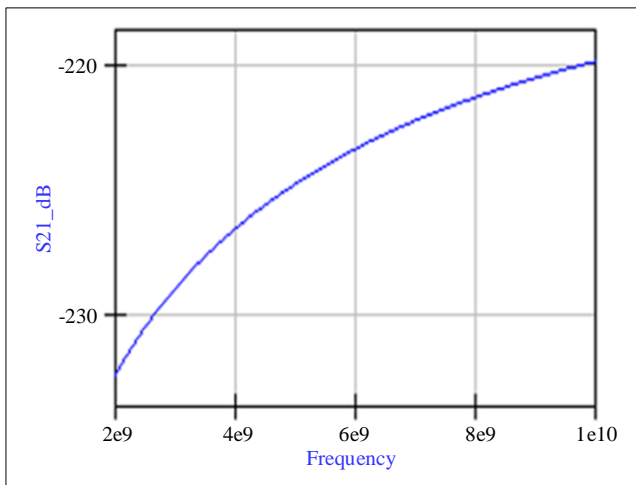


Fig. 6 Forward voltage gain (S21) in single cascode LNA

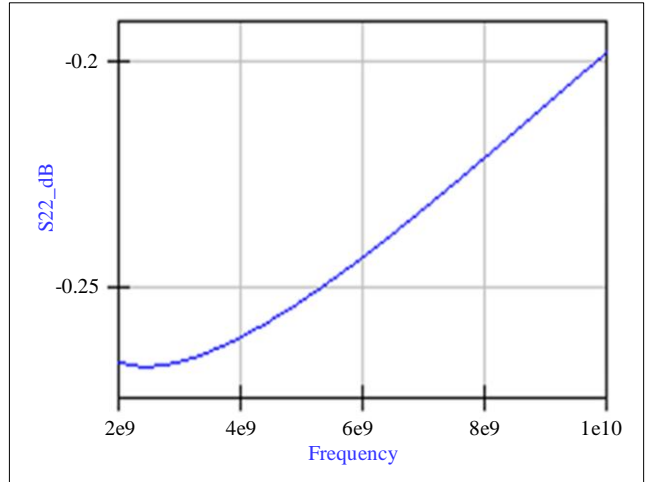


Fig. 7 Output reflection co-efficient (S22) in single cascode LNA

4.1.2. Double Stage Cascode LNA

In a double-stage cascode structure, the frequency varies from 1 GHz to 10 GHz, and the simulation responses of S -parameters are obtained, as shown in Figures 8 to 11. The input reflection co-efficient of -5.44×10^{-13} dB and output reflection co-efficient of -0.267 dB at $Q = 2$ and $I_{ds} = 6$ mA are obtained from the simulations.

These values are similar to single-stage cascode results, and these negative values indicate that the reflected power is more than the transmitted power. For an efficient amplifier, the transmitted power should be more than the reflected power.

Even though the transmission coefficient plot is not as flat as the single-stage cascode plot, the gain is still highly negative (-0.231 dB at $Q = 2$ and $I_{ds} = 6$ mA). The minimum gain requirement for a linear amplifier should be greater than 10 dB.

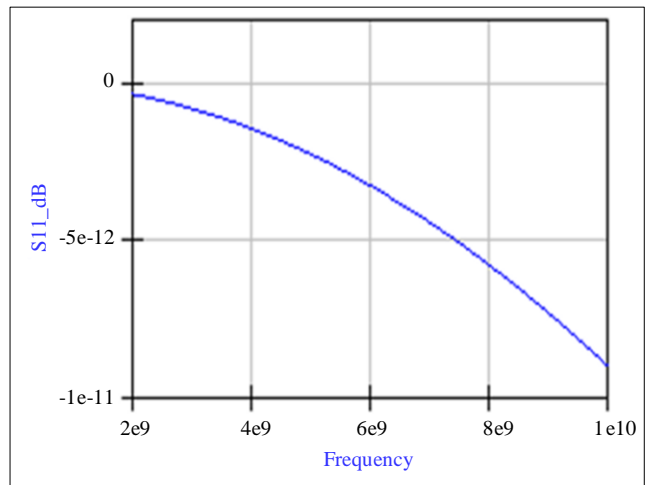


Fig. 8 Input reflection co-efficient (S11) in double cascode LNA

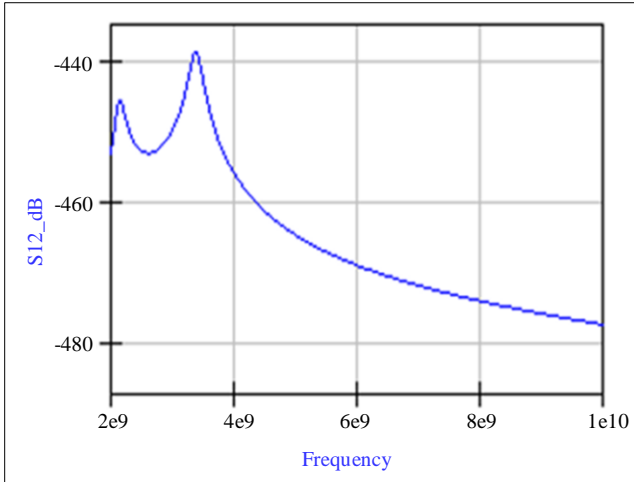


Fig. 9 Reverse voltage gain (S12) in double cascode LNA

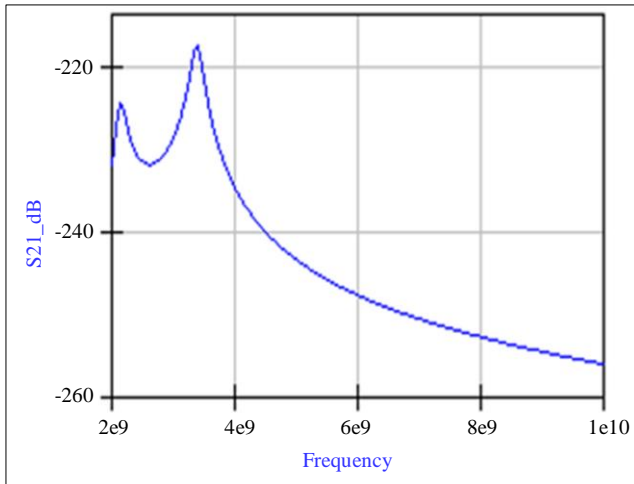


Fig. 10 Forward voltage gain (S21) in double cascode LNA

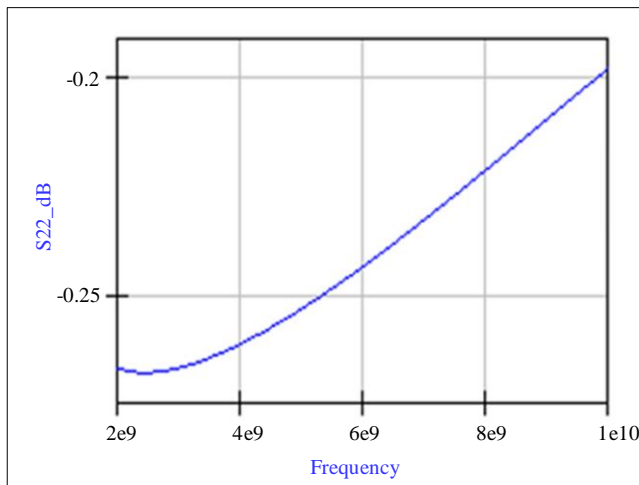


Fig. 11 Output reflection co-efficient (S22) in double cascode LNA

4.1.3. Differential Stage Cascode LNA

In the differential cascode structure, the results obtained are more convincing and efficient than those of the other two structures. The input reflection coefficient (-0.559 dB at $Q = 2$ and $I_{ds} = 6$ mA) is better and less negative at the operating frequency. Varying I_{ds} provide almost identical values. S_{11} is less negative when the Q factor is increased. Ideally, for the LNA to be stable, the S_{11_dB} should be negative (better if lower). The input reflection coefficient plot of the differential cascode is shown in Figure 12. The reverse voltage gain (S_{12_dB}) is shown in Figure 13, which indicates a constant value of -1 dB for the entire frequency range. Differential cascode structure provides the best gain performance. The obtained transmission coefficient (Forward Gain) is highly positive (67.8 dB at $Q = 2$ and $I_{ds} = 6$ mA) at the operating frequency. Gain is slightly improved when I_{ds} are increased, but an increase in the Q factor negatively affects the gain.

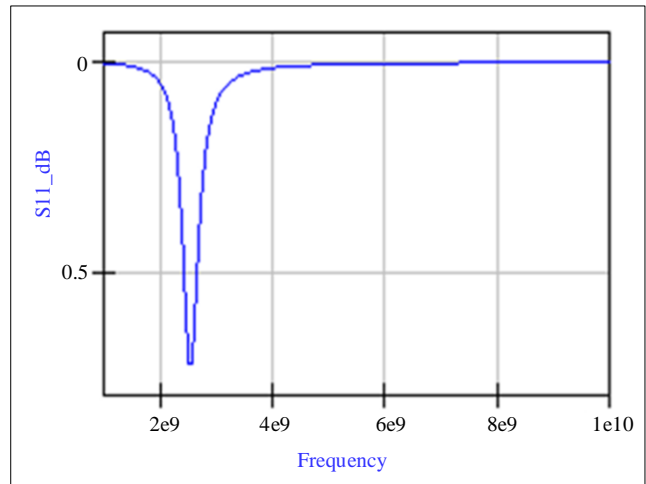


Fig. 12 Input reflection co-efficient (S11) in differential cascode LNA

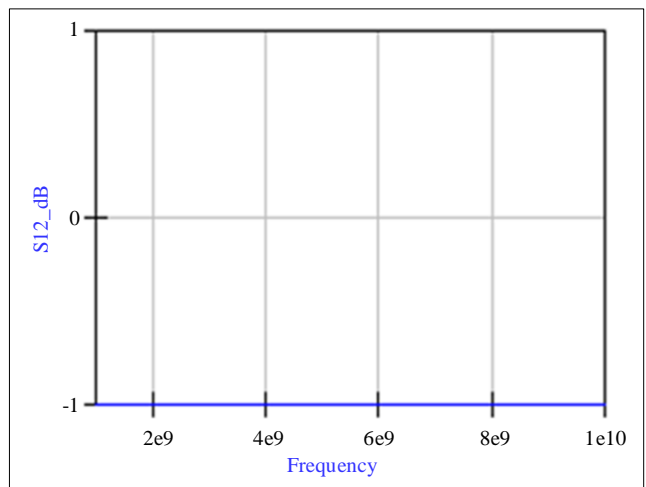


Fig. 13 Reverse voltage gain (S12) in differential cascode LNA

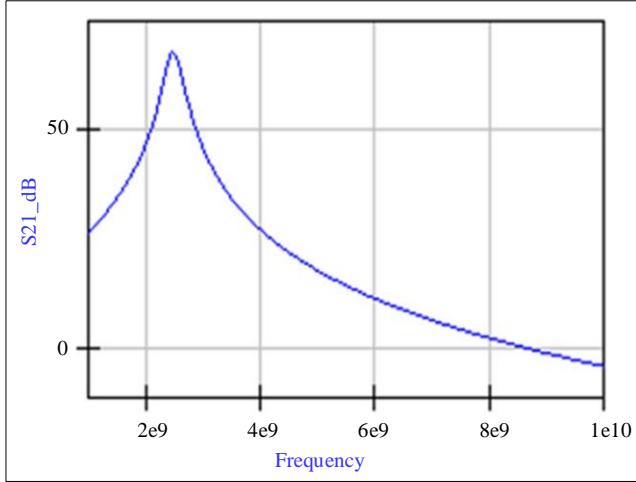


Fig. 14 Forward voltage gain (S21) in differential cascode LNA

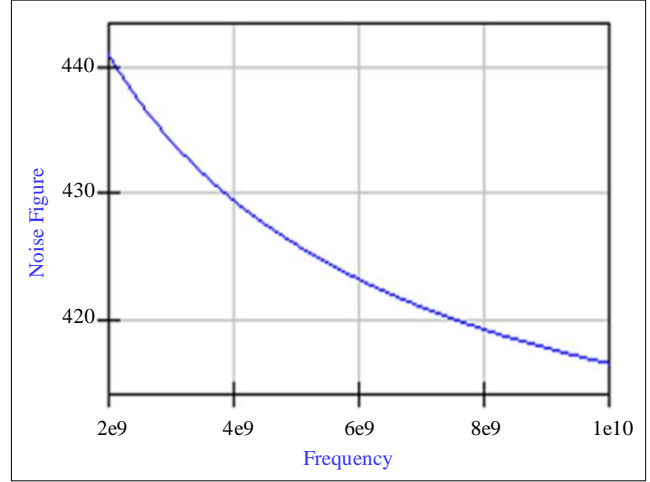


Fig. 16 Noise figure in single cascode LNA

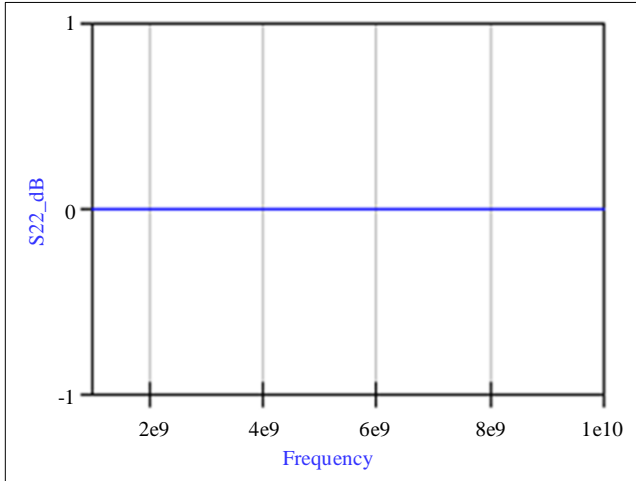


Fig. 15 Output reflection co-efficient (S22) in differential cascode LNA

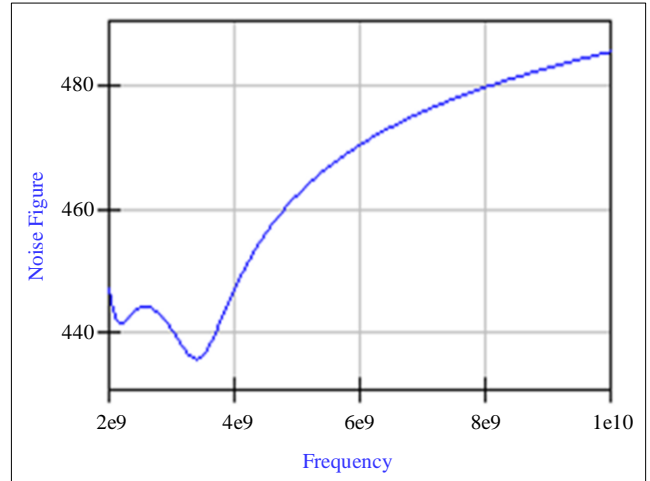


Fig. 17 Noise figure in double cascode LNA

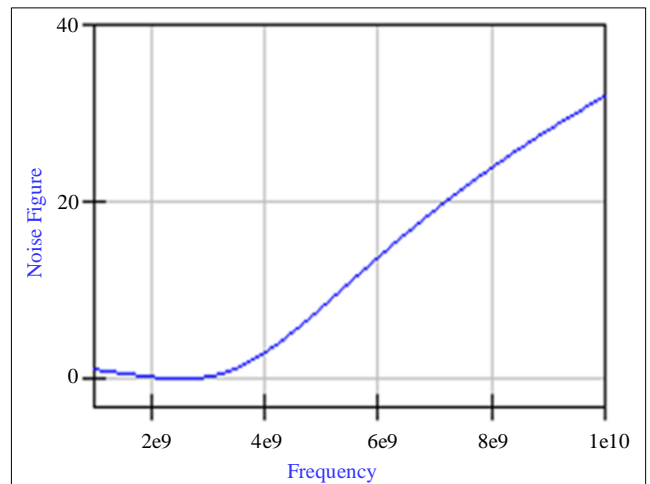


Fig. 18 Noise figure in differential cascode LNA

The transmission co-efficient plot is shown in Figure 14. Generally, the higher voltage gain will result in better performance. The output reflection coefficient is constant (0dB) at the operating frequency irrespective of the Q factor and I_{ds} , as shown in Figure 15.

4.2. Noise Figure

The Noise Figure (NF) is a crucial parameter used to quantify the signal degradation (SNR) as it passes through a system. The Noise Figure of the Low noise amplifier is the dominant contributor compared to other blocks in a system. Hence, it is vital to assess the NF of the designed amplifier to ensure better performance. In the Qucs tool, NF is simulated for all the topologies in the frequency range of 2 to 10 GHz and the corresponding values are obtained based on the Equation (15).

$$\text{Noise Figure (NF)} = 10 \log (1 + F/A_p) \quad (15)$$

Where, F is the noise figure of the amplifier, and A_p is the power gain of the amplifier.

The Noise Figure plot of the single-stage cascode LNA is shown in Figure 16. This topology provides a high noise figure (438 dB at $Q = 2$ and $I_{ds} = 6$ mA) irrespective of the variation

in Q and I_{ds} . Due to high noise figure (dB) and negative gain (dB), this topology is not a good choice for practical applications. The double-stage cascode NF plot is shown in Figure 17. This topology needs to be improved as the obtained noise figure is almost identical to the single-stage cascode. A better Noise Figure (0.0329 dB at $Q = 2$ and $I_{ds} = 6$ mA) close to zero is obtained for the differential cascode amplifier, as

shown in Figure 18. An increase in I_{ds} helps to slightly reduce the Noise figure; on the other hand, the Noise Figure is increased when the Q factor is increased. For a good LNA, the noise figure should be as low as possible (less than 2dB). So, the differential cascode stage is more suitable for practical applications due to the very low noise figure and high positive gain.

Table 2. Simulated s-parameters and noise figure results of three different LNA circuits for varying Q and I_{ds}

Q and I_{ds}	Single Stage Cascode				Double Stage Cascode				Differential Cascode			
	S11 (dB)	S21 (dB)	S22 (dB)	NF (dB)	S11 (dB)	S21 (dB)	S22 (dB)	NF (dB)	S11 (dB)	S21 (dB)	S22 (dB)	NF (dB)
Q = 2, I_{ds} = 4 mA	-8.16e-13	-229	-0.267	434	-8.15e-13	-229	-0.267	440	-0.551	65.7	0	0.0412
Q = 2, I_{ds} = 5 mA	-6.59e-13	-230	-0.267	436	-6.58e-13	-230	-0.267	442	-0.552	66.7	0	0.0366
Q = 2, I_{ds} = 6 mA	-5.44e-13	-231	-0.267	438	-5.42e-13	-231	-0.267	444	-0.559	67.8	0	0.0329
Q = 3, I_{ds} = 5 mA	-3.86e-15	-251	-0.267	477	-1.37e-12	-228	-0.267	437	-0.0941	54.1	0	0.46
Q = 4, I_{ds} = 5 mA	-2.37e-12	-225	-0.267	426	-2.37e-12	-226	-0.267	433	-0.0675	49	0	1.1
Q = 5, I_{ds} = 5 mA	-0.000172	-69.6	-0.267	116	-0.000172	-71.1	-0.267	123	-0.0629	45.8	0	1.78

Table 3. Performance comparison of the existing works with the proposed work

Technology	Frequency Range (GHz)	S11 (dB)	S12 (dB)	S21 (dB)	S22 (dB)	NF (dB)	Reference Number
0.13µm CMOS	2.4			11.8		1.1	[12]
0.13µm CMOS	2.45	-42	-67.8	23.75	-23.46	2.02	[4]
0.35µm 4M2P CMOS	2.45	≤ -14		27		7.9	[15]
45nm Single Stage	3.4	-18.6	-43.6	28.8	-10	2.1	[2]
180 nm CMOS	.4	-22	-8.88	26.5	-28m	3.65	[3]
180 nm Cascode	2.45	≤ 15.15		3		2.48	[5]
180 nm CMOS	2.3-2.6	-15.25	-6.4	22.8	-5.6	3.066	[7]
60 nm CMOS Differential Cascode	2.45	-0.559		67.8		0.0329	Proposed work

It is clear from the observation in Table 2 that differential cascode topology provides better performance compared to the other two topologies. The return loss (input reflection coefficient) of differential cascode topology is negative and has a drop at the operating frequency. The best result for differential cascode topology is obtained using $Q = 2$ and $I_{ds} = 6$ mA as the design provides S11 of -0.559 dB, S22 of 0 dB, S21 of 67.8 dB and NF of 0.0329 dB.

A comparative study of different LNAs in the existing literature is compared with the proposed work in Table 3. From Table 3, it is evident that our proposed design in 60 nm CMOS differential cascode LNA resulted in a very high gain of 67.8 dB and a very low Noise Figure of 0.0329 dB, which is comparatively better than the LNAs available in the survey. This configuration can provide very high gain with low noise figures as required for healthcare applications.

5. Conclusion

The field of communication has undergone massive growth in the current scenario. It is important to understand the effect of noise on the receiver side and the functionality of LNA. In this paper, an inductively degenerated common-source LNA using 60 nm technology has been designed under three different topologies at 2.4GHz for healthcare applications in the QUCS tool. Based on the analysis and comparisons, it has been observed that LNA designed using differential cascode topology provides better performance. The usage of degenerative inductors has improved the noise performance. The designed differential cascode LNA exhibits high gain with a low noise figure. Even though the usage of inductive source degeneration topology has provided a good noise performance, this topology still needs to be improved as it is sensitive to gate-induced current.

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