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Original Article

Area Efficient Full Subtractor Design for Quantum-Dot Cellular Automata

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Abstract *- QCA technology represents a disruptive nanoelectronics paradigm characterized by its terahertz speed, reduced energy consumption, and potential for very high device density. Full subtractors play a crucial role in the Digital Signal Processing (DSP) systems for arithmetic operations and binary data manipulation. This article proposes a dedicated QCA Full-Subtractor (QFS) design to leverage electrostatic intercellular interaction. The proposed QFS design does not utilize any majority gate, greatly diminishing the cell count, required area, and performance. This novel design requires only 15 QCA cells with 7644.00 nm^2 area and 0.5 latency. Functional validation and energy calculations are evaluated using the tool QCA Designer-E.*

Keywords *- Area efficiency, Electrostatic interaction, Full Subtractor, QCA, Nanoelectronics.*

1. Introduction

In recent years, the semiconductor sector has continued to be propelled by escalating consumer preferences for improved integration processes, reliability, and speed in semiconductor Integrated Circuits (ICs). The conventional method of CMOS semiconductors faces limitations in miniaturization because of current leakage issues caused by quantum mechanical tunnelling, preventing effective device shutdown and resulting in higher temperature dissipation that jeopardizes chip integrity. This reality has compelled designers to explore innovative methods to provide enhanced integration and decreased energy use for Digital Signal Processor (DSP) integrated circuit applications.

The CMOS process has encountered constraints throughout the ultra-DSM domain because of several short-channel phenomena that impair circuit performance [1]. Consequently, VLSI designers are investigating many technologies, including single-electron transistors, carbon nanotube field effect transistors, graphene nanoribbons, and Quantum-dot Cellular Automata (QCA), among the most viable alternatives to CMOS semiconductors [2, 3].

Quantum-dot Cellular Automata (QCA), a rapidly advancing nanocomputing technology, was presented by Lent et al. in 1993 [4]. This method could soon substitute standard CMOS technology for implementing digital circuits at the nanoscale. The basic principle of QCA is to encode the binary information through positioning the electrons within the Quantum dots, enabling ultra-low power and high-speed processing. Quantum dots are the nanoscale semiconductor particles that restrain electrons in three dimensions heading to discrete energy levels. These quantum dots are the basic building blocks of QCA cells, and electron confinement within these dots aids the external electric fields in controlling the positions of the electrons. A QCA cell fundamentally has four quantum dots arranged in a square formation, accommodating two movable electrons capable of tunnelling across the dots [5].

Two primary polarisation states are determined according to the positioning of these two electrons at the diagonal corners. The binary numbers '0' & '1' correspond to the polarisation states P = -1 & P = +1, correspondingly [6], as seen in Figure 1(a). The electron configuration in a particular cell is affected by the electron configuration in adjacent cells owing to the coulombic interactions between them [7]. This characteristic enables the transmission of information in binary format using QCA circuits.

Unlike traditional transistor-based circuits, no current flow is necessary for information transfer in the circuit. The interactions of QCA cells form QCA logical gates. The fundamental logic gates of QCA are indeed the inverter alongside the Majority Voter (MV) gates [8]. The basic QCA Inverter gate simply reverses the state of the input cell polarization and the binary value. It is basically implemented in two models, as shown in Figure 1(b), and the positioning of

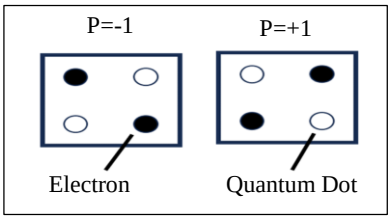
the cells is in such a way that its output is opposite of its input due to the spatial configuration and interactions. The basic MV gate is shown in Figure 1(c) takes 3 inputs, and it outputs a binary value that appears in the majority of the inputs. QCA cells are arranged in arrays forming a binary wire, as accompanied in Figure 1(d), to propagate the binary information via the electrostatic effect between adjacent cells.

QCA technology operates without the usage of current or voltage. The phenomenon is predicated upon Coulombic interaction among electrons inside quantum dots. Consequently, it will serve as a potential contender in place of CMOS semiconductor technology previously employed within Integrated Circuits (ICs). A multitude of efforts have been documented in the literature aimed at the cost-effective implementation of QCA circuits. The QCA logical design circuit has been driven by its potential uses within low-power electrical design. It has recently garnered considerable interest. Conversely, subtraction serves as a fundamental function in several digital applications. The clocking mechanism is the heart of the QCA circuits, which controls the movement of electrons and ensures synchronized information transfer. The QCA clocking system typically engages in dividing the circuit into zones with four clock phases as depicted in Figure 2. Each clock phase controls the electron tunneling within the cells for a sequence of operations like switch, hold, release, and relax [10].

The key elements of this paper regarding the suggested structures have been summarised as follows:

- A unique, complete subtractor structure is suggested, employing electrostatic interactions among cells to achieve the necessary functionality.
- The comparison findings indicate a significant improvement in complexity, area occupancy, power dissipation, and delay. The suggested QFS architecture occupies 20% less space and utilizes 25% fewer cells. The suggested design dissipates 33% less energy than the QFS documented in the literature.

The article's structure follows: Section 2 examines the literature review. Section 3 presents the design and modelling of the suggested model. Section 4 discusses the findings from the circuit simulations, comparing area, latency, energy dissipation and cell count. Conclusions are put forward in Section 5.



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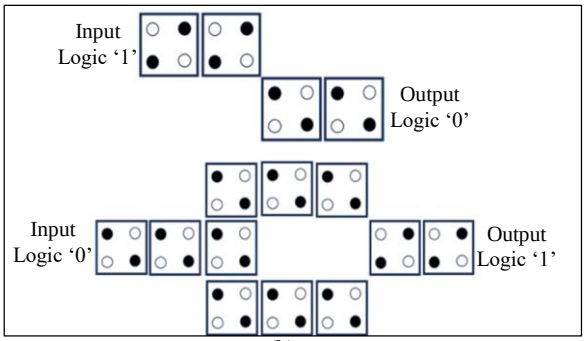

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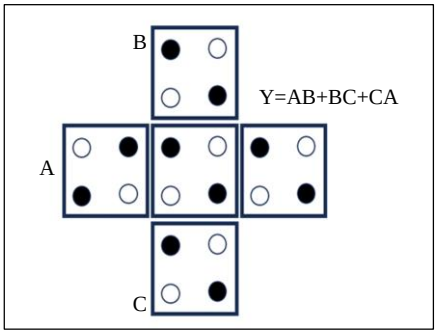

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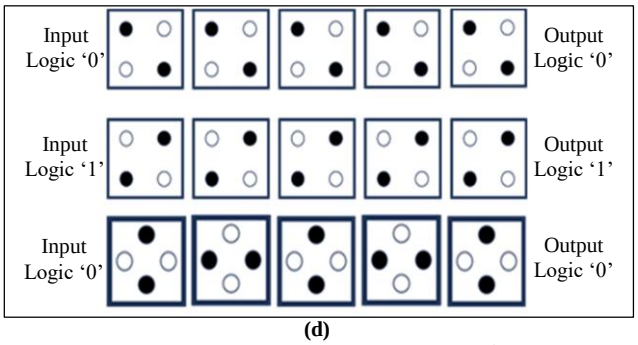


(d)

Fig. 1 (a) Polarization in QCA cell, (b) Two models of inverter gate, (c) Majority gate, and (d) Basic QCA binary wire and rotated cell type binary wire [9].

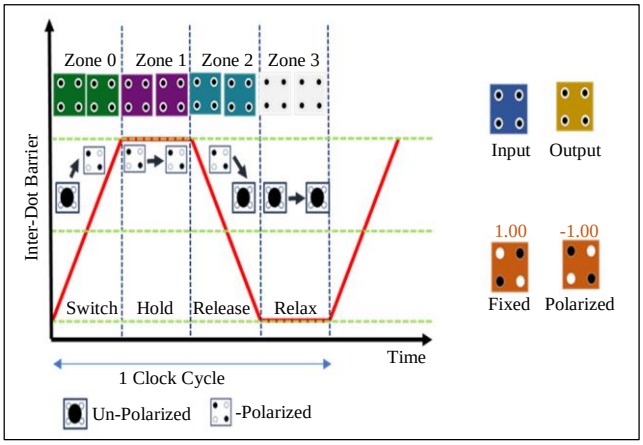


Fig. 2 Clocking mechanism in QCA and colour representation of the cells [9]

2. Literature Review

The following section provides a summary of the existing comparable works. Numerous QCA-based subtractor circuitry exist within the literature; however, there have been few studies on full subtractor circuitry. Limited prior studies have documented subtractor circuitry. The essential factors from the available literature include cell count, architecture schematic, clocking latency, and crossover requirements. Karthigai Lakshmi et al. [11] presented a Full-Subtractor circuit based on QCA in 2010, using seven Majority gates and four inverter gates. The design required 178 cells. Kumari and Gurumurthy [12] introduced majority gate-based QFS 2014 using vertically stacked elements to reduce the area and cell count. It required 61 cells to be implemented, and 37 cells were used for interconnections.

Dallaki and Mehran [13] proposed a QFS circuit in 2015 using an XOR gate constructed with majority gates. 136 cells are needed to implement, and a latency of 7 clock phases is noted. In 2016 Labrado, and Thapliyal [14] proposed a QFS using a 5- input and a 3- input Majority gates. They used 3 inverter gates, and the design needed 63 cells and 0.5 um2 area with a latency of 0.75. An XOR gate is proposed in [15], and it is used to implement a QFS with only 37 cells, 0.04 um2 of occupied area, and 0.75 clock cycles.

A 1-bit Quantum Flip-Flop using just an Exclusive-OR gate and a Majority gate is suggested in [16], necessitating 122 cells. A 5-input Majority gate-based Quantum Flip-Flop is presented in [17], employing 53 cells, occupying an area of 0.047 um^2, with a latency of 0.75. In 2019, Mosley developed a novel structure for the majority gate (MV32) and used it to create a Full-Subtractor circuit. The QFS design is shown in Figure 3(a) has just 29 cells and comprises an area of 0.024 μm^2 [18]. A 27-cell QFS is presented in [19], using an XOR gate that relies on an explicit cell connection, as seen in Figure 3(b). It included an area of 0.03 μm^2, and its latency is 0.5. Bahar et al. [20] suggested a Quantum Field System using 44 cells and an area of 0.04 μm^2.

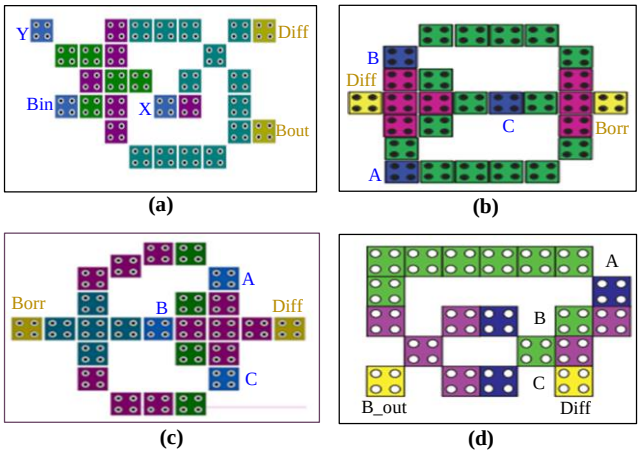


Fig. 3 Full subtractor designs [18-22]

Ismail et al. in [21] introduced a 3-input XOR gate using just 8 cells. Then, it was utilized to propose a QFS circuit, as displayed in Figure 3(d), using only 20 cells and 0.5 latency. Hosseinzadeh et al. in [22] proposed a 25-cell QFS that takes 0.025 um2 area with a latency of 0.75. As an observation, for the design of QFS, the least number of cells used so far is 20, and the least occupied area is 0.025 um2 with a minimum latency of 0.5 clock cycles.

3. Design of Proposed Novel 1-Bit Full-Subtractor

The following section presents a unique Full Subtractor featuring superior performance metrics. Prior studies concerning subtractors have been extensively executed using QCA technology [11-22]. The operational indications for the subtractor include superior power usage, latency, and complexity.

The suggested Full Subtractor has been introduced to achieve an efficient performance concerning delay, area, cell count, along power usage. Figure 4 illustrates the many components of the research methodology used in conducting the thesis inquiry. The methodology is a systematic and organized approach for effectively resolving a specific problem. Previous study indicates that Figure 4 illustrates the significance of establishing requirements for QCA-based subtractors.

Furthermore, the selection of device technology is contingent upon several variables. The proposed circuit is then simulated using optimization techniques to meet the required criteria. The QCA-based subtractor concept has been successfully implemented in the fields of DSP applications and exhibits minimal power requirements. The suggested designs are validated using simulations conducted with QCA Designer software, as seen in Figure 6.

A 1-bit Full Subtractor corresponds to a combinational logical circuitry including three inputs and two outputs. It does subtraction using three binary inputs: the minuend (A), subtrahend (B), along Borrow-in (Bin), yielding a Difference output (Diff) alongside a Borrow-out (Borrow) output. The Boolean expression is given by the Equations (1) and (2).

$$Diff = A \oplus B \oplus Bin = ABBin + \bar{A}\bar{B}Bin + \bar{A}B\overline{Bin} + A\bar{B}\overline{Bin} \quad (1)$$

$$Borrow = \bar{A}B + \bar{A}Bin + BBin \quad (2)$$

Most of the QCA Full subtractor designs reported so far used an XOR gate to implement the Diff function and majority gate for the Borrow function, as demonstrated in Figure 5.

The aforementioned part presents a distinctive design for building a QCA 1-bit Subtractor, only relying on the electrostatic interactions between neighbouring cells. This

architecture does not require an additional majority gate to execute its Borrow operation. The suggested QFS necessitate just 15 cells and an area of 0.008 μm². The layout delay has become just 0.5 clock cycles, and the configuration of the recommended QFS is demonstrated in Figure 6.

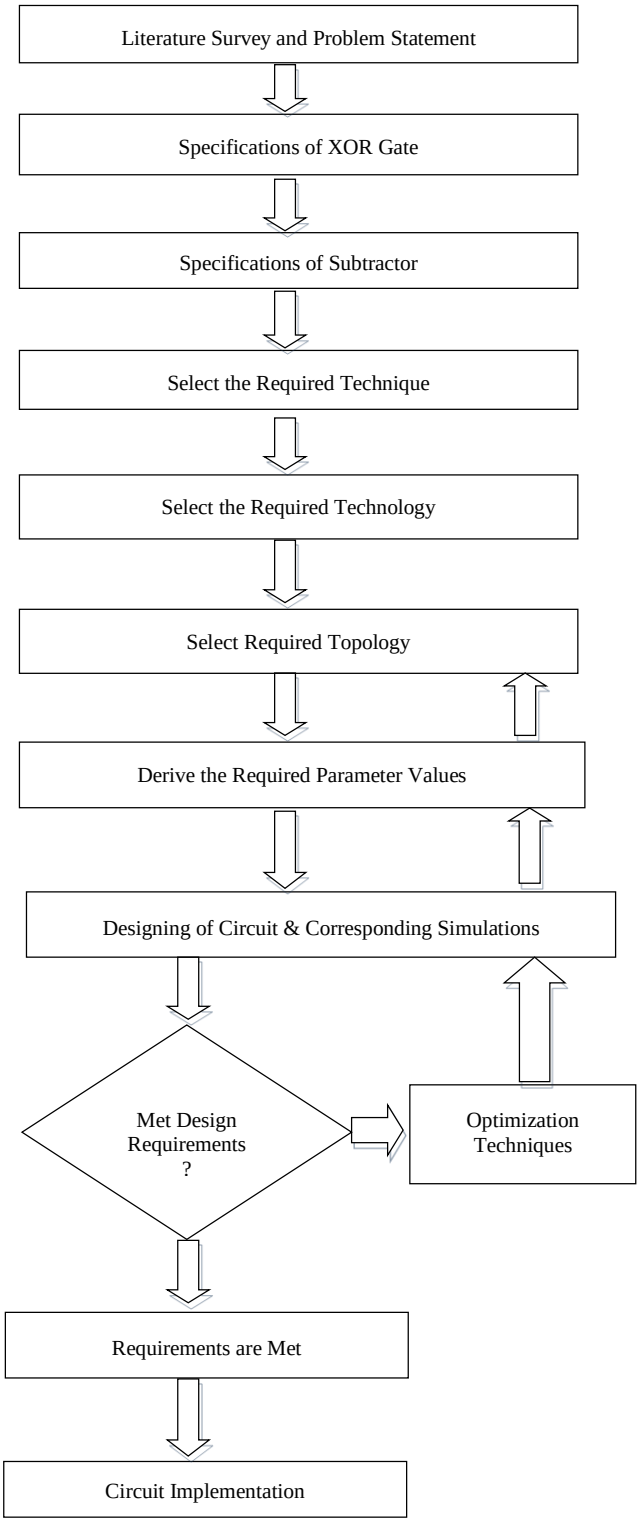


Fig. 4 The methodology adopted in this work

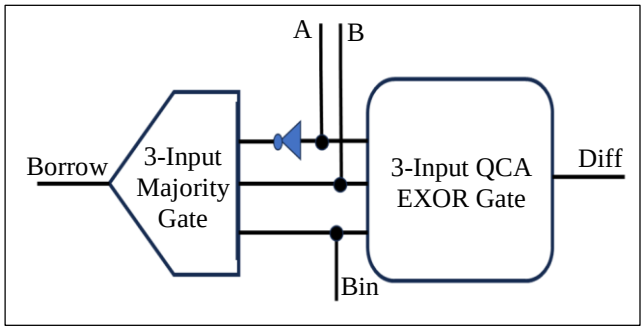


Fig. 5 Block representation of QCA 1-bit subtractor

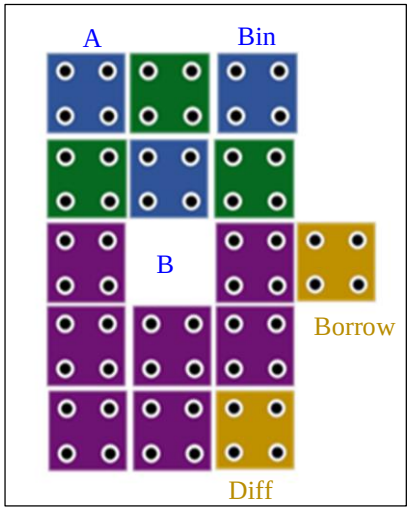


Fig. 6 Layout of proposed QCA full-subtractor

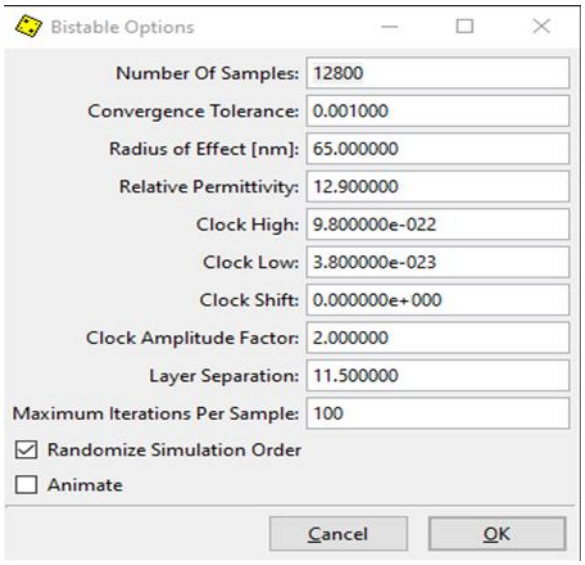
4. Simulation Outcomes and Analysis

A smaller change of a subtractor area will end up with an ensuing decrease in the scaled-up components. The following section compares the recommended QCA subtractor with prior research. The benefits associated with the QCA circuity shown in this work are apparent. Table 3 illustrates that the proposed Subtractor exhibits a considerable advantage beyond all prior implementations.

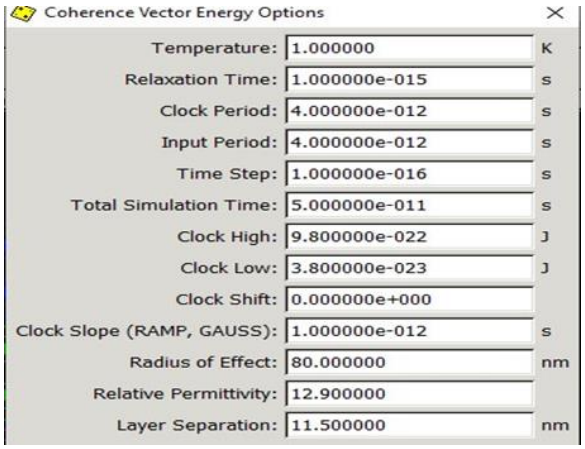
The recommended QFS design is simulated on the QCA Designer-E (QD-E), the latest tool introduced in 2018 by Sill Torres et al. [23]. It offers three simulation Engines in which we used the Bistable approximation mode for functional verification and the Coherence vector (w/ Energy) mode for the energy dissipation analysis. The default settings are selected across both simulation engines, as seen in Figure 7(a) & (b).

The recommended QFA is implemented in exhaustive method, as the outcomes need verification for just eight input possibilities. The truth table is represented in Table 1, while the outcomes of the simulation for the bistable mode are illustrated in Figure 8. The maximum polarisation values for Diff and Borrow have been determined as 0.992 and 0.950, correspondingly, according to the Figure 8. Coherence vector

Energy mode simulation results are organized in Table 2. The sum and average values of E_Bath total values are noted as $1.53e^{-2}$ eV and $1.39e^{-3}$ eV, respectively.



(a)



(b)

Fig. 7 Option settings in QCA simulation engines (a) Bistable approximation, and (b) Coherence vector energy mode.

Table 1. 1-bit Subtractor truth table

Inputs of 1-bit Subtractor			Output	
Bin	**A**	**B**	**Borrow**	**Diff**
0	0	0	0	0
0	0	1	0	1
0	1	0	1	1
0	1	1	0	0
1	0	0	1	1
1	0	1	0	0
1	1	0	1	0
1	1	1	1	1

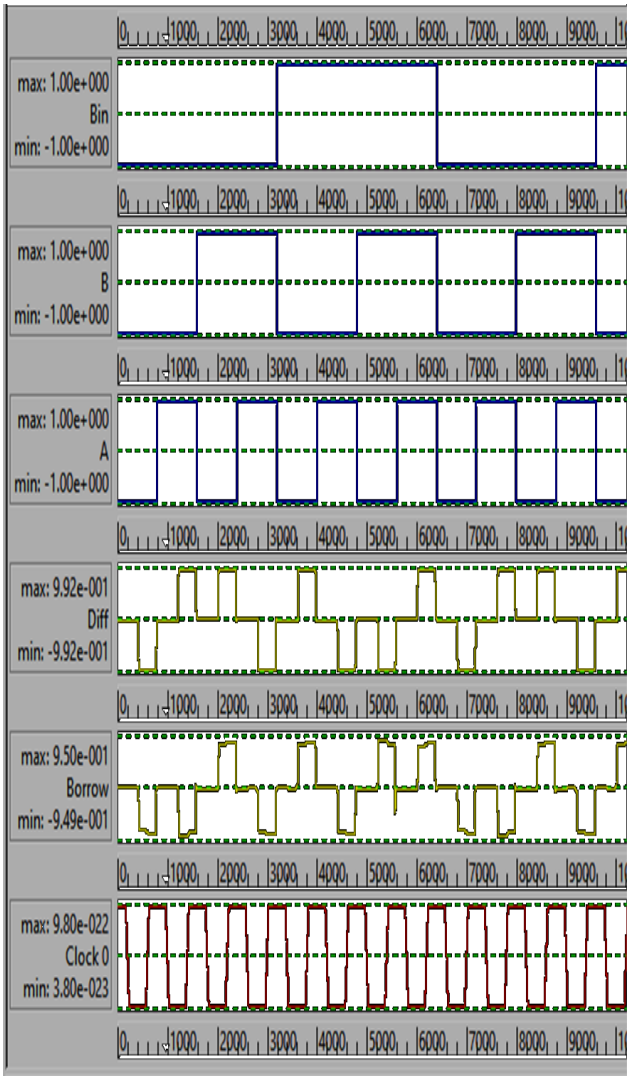


Fig. 8 Bistable approximation simulation results of the proposed QFS

The comparison between the recommended QFS and the previously available QFS documented in the available literature across essential design parameters is shown in Table 3.

A smaller change of a subtractor area will result in an ensuing decrease in the scaled-up components. The following section compares the recommended QCA subtractor with prior research. The benefits associated with the QCA circuity shown in this work are apparent. From Table 3 and Figure 9, it is evident that the proposed Subtractor exhibits a considerable advantage beyond all prior implementations.

The proposed subtractor occupies at least 10% less area when compared to existing works. Also, the proposed subtractor uses at least 5% less number of cells when compared to existing works. Similarly, the proposed subtractor occupies a minimum of 48% less energy dissipation when compared with existing works.

Table 2. Energy dissipation analysis of the proposed QFS

Total E-bath: (eV)	Total E-clk: (eV)	Total E-Error: (eV)	Total energy Dissipation (Sum-E-Bath)	Avg Energy Dissipation/Cycle (avg-E-bath)
1.4966e-3	3.2094e-3	-1.5568e-4	1.53e-02 eV (Error: +/- -1.61e-03 eV)	1.39e-03 eV (Error: +/- -1.46e-04 eV)
1.7462e-3	3.8197e-4	-1.8654e-4		
3.9901e-4	9.6747e-5	-3.4079e-5		
1.6843e-3	7.5334e-4	-1.7881e-4		
1.4165e-3	7.5334e-4	-1.5012e-4		
5.2508e-4	9.6741e-5	-4.8037e-5		
1.9940e-3	3.8199e-4	-2.1523e-4		
2.4298e-3	3.209e-3	-2.6164e-4		
1.4966e-3	3.209e-3	-1.5564e-4		
1.7463e-3	3.819e-4	-1.8654e-4		
3.9901e-4	9.674e-5	-3.4079e-5		

Table 3. Comparison across design metrics QCA full subtractors

QFS Design in	Latency	Area (um^2)	No Cells are Required	Crossover Type
[7]	2	0.132	178	Multilayer
[8]	1	0.04	98	Multilayer
[9]	1.75	0.168	136	Multilayer
[10]	0.75	0.05	63	Rotated-cell based
[11]	0.75	0.04	37	No
[12]	0.75	0.1	83	No
[13]	0.75	0.047	53	Rotated-cell based
[14]	0.75	0.024	21	No
[15]	0.5	0.03	27	No
[16]	1	0.04	44	Clock-zone
[17]	0.5	0.01	20	No
[18]	0.75	0.02	25	No
This paper	0.5	0.008	15	No

Table 4. Comparison of energy values of QFSs

QFS Design in	Energy Dissipation (eV)	
	Average	Total
[15]	2.09e-3	$2.30e^{-2}$
[9]	6.78e-3	$7.46e^{-2}$
[7]	4.46e-3	$4.91e^{-2}$
[20]	2.07e-2	$2.28e^{-2}$
This paper	1.39e-3	$1.53e^{-2}$

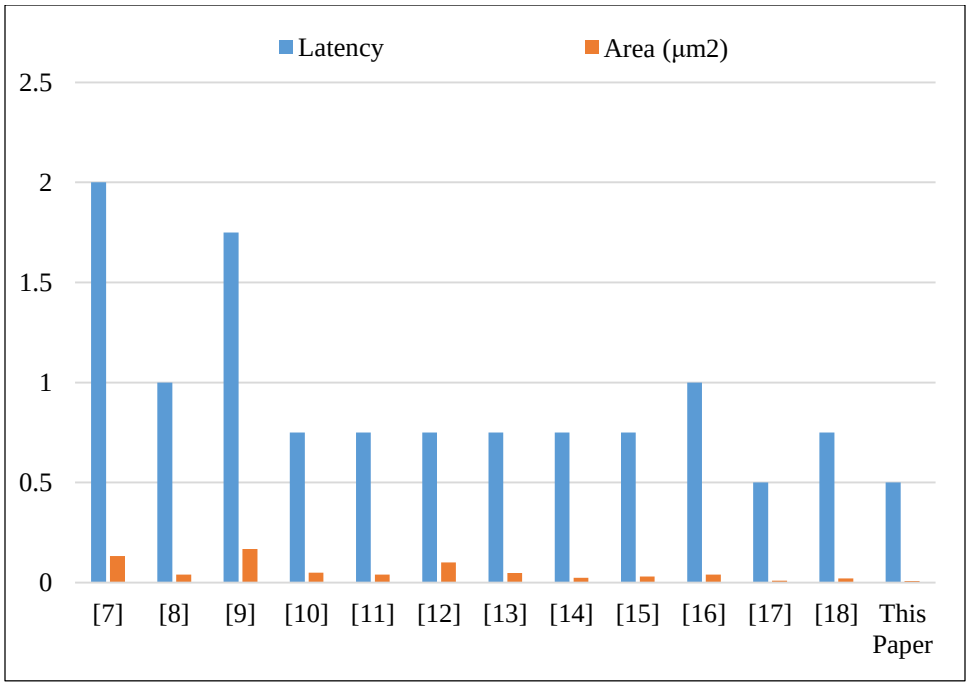


Fig. 9 Comparison across design metrics QCA full subtractors

5. Conclusion

Developing low-power subtractors remains a continual challenge for digital signal processing applications. In this work, the authors introduced a new architecture for implementing a full subtractor based on the principle of intercellular interaction in QCA. Not at least one majority gate is required to design the proposed QFS. It exhibits superior performance in almost all design parameters when compared to the previous designs. Functional validation and energy calculations are evaluated using the tool QCA Designer-E. The proposed subtractor occupies at least 10% less area when compared to existing works. Also, the proposed subtractor uses at least 5% less number of cells when compared to existing works. Similarly, the proposed subtractor occupies a minimum of 48% less energy dissipation when compared with existing works. In subsequent years, we will endeavour to investigate and develop superior full subtractor component architectures to serve as fundamental modules enabling larger-scale mathematical operations circuitry that utilize the QCA framework.

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