SSRG International Journal of Electrical and Electronics Engineering
ISSN: 2348-8379/ https://doi.org/10.14445/23488379/IJEEE-V11I12P115

Volume 11 Issue 12, 160-169, December 2024

Original Article

Prevention of Voltage Sag, Swell and Harmonics in Grid Connected Systems Using 19-Level Inverter UPQC

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Received: 09 October 2024 Revised: 10 November 2024 Accepted: 08 December 2024 Published: 31 December 2024

Abstract - *The Adaptive Fuzzy Logic Controller (AFLC) approach is used to build and assess a 19-level Unified Power Quality Conditioner (UPQC). The UPQC corrects voltage sag, swell, and harmonics to improve power quality. To improve performance and mitigate the effects of power quality disruptions, the compensation levels are dynamically changed using the AFLC algorithm. The study uses Matlab/Simulink for UPQC and AFLC demonstrations, providing simulation results and performance evaluations.*

Keywords - *AFLC, ANFIS, Multilevel inverter, Power quality, Shunt & series compensator, Total Harmonic Distortion (THD).*

1. Introduction

The idea of power quality differs for different elements of the power system. Power quality, in the eyes of the power supplier, refers to the level of electricity delivered to the consumer in accordance with his capacity, with appropriate reliability and regulation of voltage and frequency. The consumer perceives the capacity to use the supplied power with precise signal magnitude and shape as the assertion of power quality. Power quality problems affect the system's quality of power and the reliability of the power supply, and there are environmental concerns. Some concerns with electricity quality are about the short duration, while others are about the longer duration. Power quality problems are classified as short or long-term depending on how long they last. If they last less than a minute, they are classified as short-term problems. Even a temporary power quality issue might reduce system performance and cause the power system to operate unintentionally. Increased use of power electronic converters and non-linear equipment is to blame for the worsening of voltage or current in the power distribution system. Power quality can be significantly compromised by voltage and current disturbances; two of the main challenges are voltage sag and swell, which frequently lead to equipment failure or damage. Voltage sag is a brief decline in rms voltage below the typical level, usually between 0.1 and 0.9 pu, that lasts anywhere from a few cycles to a fraction of a second. High-demand events, including the starting of large motors that draw excessive inrush current or short circuits that upset voltage stability, often constitute the source of this issue. Critical problems like industrial motors halting because of inadequate power or delicate devices like Programmable Logic Controllers (PLCs) shutting down because they might erroneously interpret the decrease as a malfunction can result from voltage sags. On the other hand, a temporary rise in rms voltage over the typical range, often between 1.1 and 1.8 pu, that lasts for up to one minute is known as a voltage swell. Usually, this is brought on by the unexpected disconnections of heavy loads or system malfunctions that result in voltage imbalances. Swells have the potential to overstress equipment, leading to insulation failure in transformers or circuit overheating those damages delicate electronics like Variable Frequency Drives (VFDs). Such challenges illustrate how crucial it is to implement effective power quality controls to protect against damage and ensure system dependability. Power electronic converters, such as rectifiers and thyristor converters, are non-linear types of loads that cause significant disruption in AC mains. Problems with voltage and current quality can be mitigated using one of two methods. The first approach method is load conditioning, which ensures that the operational equipment is resistant to power disturbances, enabling operation even under significant current and voltage distortion. This paper has used deep dives into Active Power Filters, focusing on technical design and optimization. [1], study investigating the incorporation of ANFIS controllers into UPQC and compares their impact to typical PI controllers [2] has picked up comprehensive investigations on tuning ANFIS controllers, offering light on performance-enhancing methodologies. [3] This paper has considered the study demonstrating combining a 3-Φ photovoltaic system with UPQC, focussing on renewable energy [9]. Also, the article investigated the behavior and usefulness of Type-1 Fuzzy Controllers to tackle power quality issues by integrating them with UPQC. [13] This work outlines a thorough design strategy for I-UPQC$_{PV}$, including shunt and series compensator [18]. This work includes a study that provides a detailed methodology and specifics of a methodical approach to the mathematical modelling of PV arrays using Simulink [35]. DSTATCOM is particularly effective at minimizing current-related issues such as current harmonics alleviation, reactive power compensation, and reconciling unbalanced source currents. DVR is the most effective device for mitigating almost all voltage-related issues, including voltage sag, swell, harmonic, and flicker compensation and balancing unbalanced voltage at the Point of Common Coupling (PCC). DSTATCOM and DVR function as voltage source inverters linked back-to-back with a common self-supporting DC bus to create a universal device that can solve almost all voltage and current related electrical performance problems. UPQC is primarily used in distribution systems near the Point of Common Coupling (PCC), which connects linear, nonlinear, and sensitive loads [14, 30, 34]. UPQC primarily consists of a series controller whose primary objective is to regulate voltage sag, swell, and other flickers, whereas the shunt controller is used to compensate for the harmonics. The dc-link filter connects these two converters.

2. UPQC

At the transmission level, the Unified Power Quality Conditioner (UPQC) is an extremely successful approach for reducing a number of serious power quality problems. It primarily consists of two consecutive inverters using voltage sources that share a DC bus capacitor. As illustrated in the figure below, Block diagrams can represent the UPQC's overall structure. The Unified Power Quality Conditioner (UPQC) is often used in distribution systems near the PCC to connect linear, nonlinear, and sensitive loads. It combines the functions of DSTATCOM and DVR into a single device. The UPQC's shunt-powered Active Power Limiter component offers VAR backup to the load while mitigating harmonics to ensure a high-quality power supply. The UPQC's series model APF injects appropriate voltages into the supply, compensating for voltage-related faults such as harmonic distortions, swelling, and flicker.

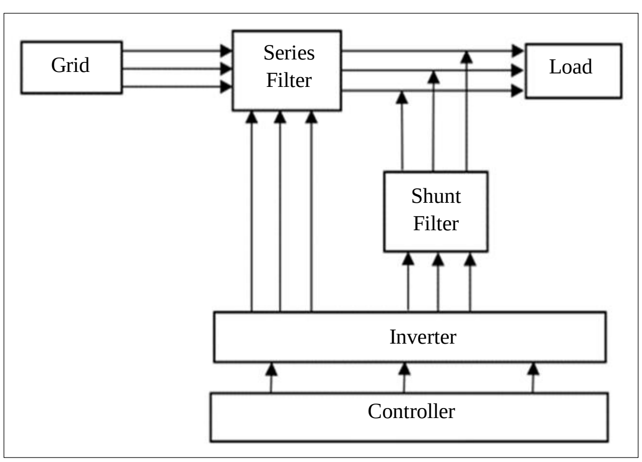

Fig. 1 Block diagram of UPQC

The primary goal of the UPQC is to foster a better quality of power by limiting the harmonics of current at load and boosting the supply's power factor [6]. A DC source is first transformed into an AC source before injecting compensating voltage into a three-phase transmission line. This alternating current source is then sent into the transformer. Gate pulses are necessary [7, 8] to ease the conversion of DC to AC.

3. Modelling of System

A three-phase zero impedance voltage source is a three-phase programmable voltage source. It is possible to pre-program time variations for the fundamental's amplitude and phase frequency. Additionally, the fundamental can have two harmonics superimposed on it.

3.1. Series Compensator

In the preceding series, the compensator block is described. Here, the 3-Φ into 2-Φ is reduced using the abc-dq algorithm, and the subsequent grid voltage is compared to the reference voltage. After comparing the voltages, the AFLC controller block produces an error signal to adjust the voltage levels accordingly. The PLL block under consideration has values such as a minimum frequency of 45 Hz, an isolation frequency cut-off of 25 Hz, and a phase of 0. In this case, the necessary voltage is compensated. As a result, stabilization is achieved by tuning the AFLC controller through this compensator.

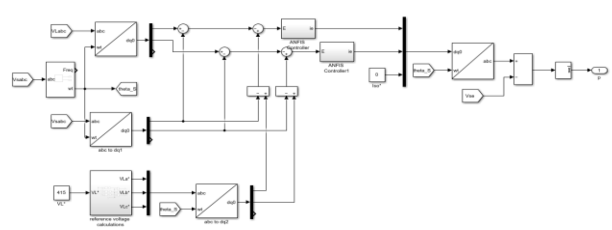

Fig. 2 Simulink model of series compensator (AFLC controller) block

3.2. Shunt Compensator

The same ABC-DQ algorithm is applied for 3-Φ to 2-Φ conversion and vice versa in the shunt compensator described above. It uses an effective low pass filter with a zeta of about 0.707 and an ideal frequency of 120 hertz. The PLL block that is being considered here primarily produces two types of output, one of which is a frequency output and the other is a ramp output that contains values such as the minimum frequency of 45 Hz, the filter limit frequency of 25 hertz, and the phase is set to 0. Derivative actions have a 10 mS time constant. The compensator mainly aims to reduce harmonics connected to the transmission end.

3.3. Series Transformer

The above series transformer block consists of mainly 3 single transformers. The value of passive elements is 10Ω and 10μF, respectively. The transformer ratings are 230-700 V (Vrms), and the Magnetization resistance and inductance values considered are 500 and 499.99 pu, respectively.

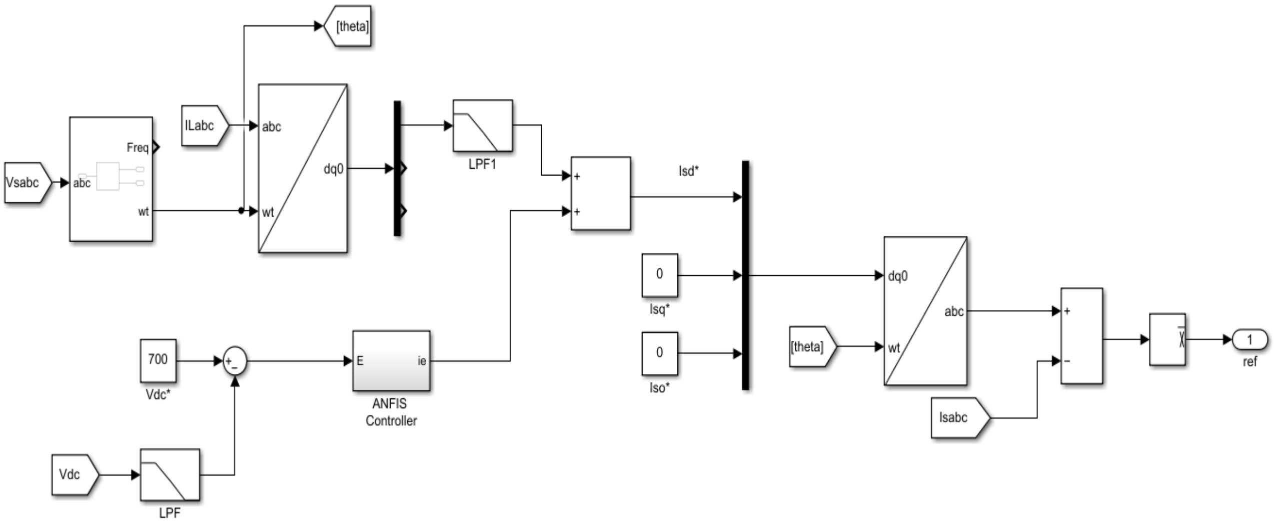

Fig. 3 Simulink model of shunt compensator (ANFIS controller) block

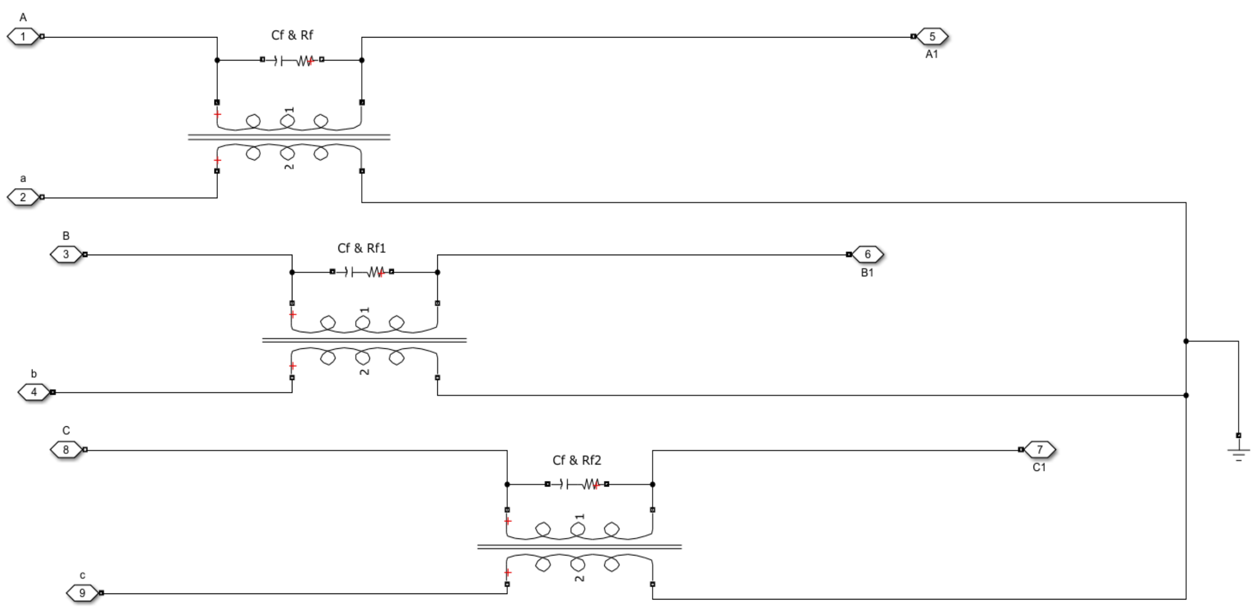

Fig. 4 Simulink model of the series transformer block

3.4. Systems Using Interval Type-2 Fuzzy Logic

The Adaptive Fuzzy Logic Controller (AFLC) algorithm is designed to model complex systems by combining fuzzy logic principles with optimization techniques to enhance accuracy and adaptability. The process begins with deriving an initial fuzzy model, which identifies the inputs, linguistic variables, and rules. This model can be extracted using methods like subtractive clustering or grid partitioning. Subtractive clustering identifies significant input-output relationships by calculating the potential of data points based on their Euclidean distances, designating cluster centers that represent fuzzy rules. Each cluster center corresponds to a rule that captures the system's input-output behavior. Alternatively, grid partitioning divides the input space into fuzzy regions, forming antecedents of rules when the input variables and their membership functions are limited. The ANFIS methodology combines gradient descent for optimizing premise membership functions and least squares estimation for consequent equations to refine the model. In selecting the final fuzzy model, input variables are evaluated by their contribution to reducing modeling error, often using Root Mean Square Error (RMSE) as the criterion.

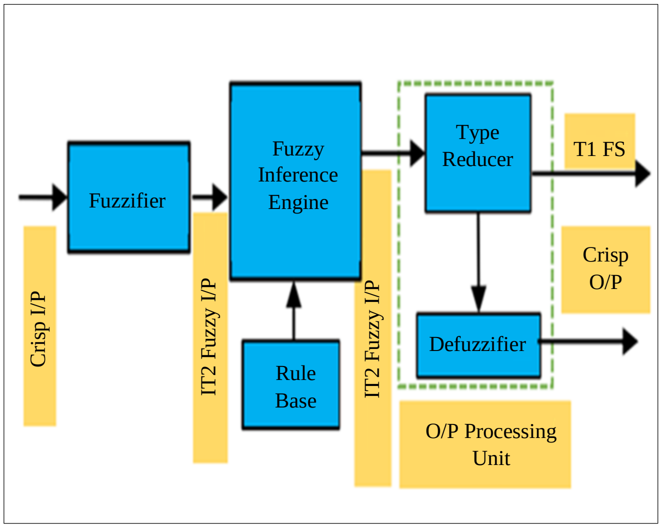

Fig. 5 Type-2 FLS

The model is optimized further by updating the premise and consequent parameters using neural network-based backpropagation. AFLC excels in handling non-linear systems with high uncertainty compared to traditional controllers due to its ability to incorporate domain-specific fuzzy rules and adapt dynamically during training, ensuring robust performance across various applications. Because type-1 fuzzy sets cannot express uncertainty, type-2 fuzzy sets are highly helpful in rule-driven Fuzzy Logic Systems (FLSs). A type-2 FLS's block diagram is shown in Figure 5. These FLSs sometimes referred to as applications of fuzzy set function approximation, are designed to lower the value of an error function. They are utilized in many different fields, such as rule-driven categorization, fuzzy logic control, and fuzzy logic signal processing [36].

Better modelling and handling of uncertainties are made feasible by introducing type-2 fuzzy sets into an FLS. In real-world scenarios marked by ambiguity and uncertainty, it is crucial. The Fuzzy Logic System (FLS) aims to minimize the discrepancy between the system's output and the expected output to approximate specific functions or behaviors. By utilizing type-2 fuzzy sets, the FLS can handle uncertainties in input variables and membership functions, enhancing its capacity to deal with intricate and uncertain environments. The type-2 FLS is an effective tool for many applications because it enables more precise and reliable modelling, control, and decision-making when uncertainties are considerable. It may be applied to signal processing jobs, categorization issues, fuzzy logic-based control systems, and any situation where accurate management of uncertainties is essential for attaining desired results. In an FLS, rules are created as IF-THEN statements drawn from numerical data or expert knowledge. The inputs and outputs of the FLS and the terms that occur in the rules are all connected to fuzzy sets identified by membership functions. Unlike interval type-2 FLSs, which contain at least one interval type-2 fuzzy set to handle uncertainties more thoroughly, type-1 FLSs only employ type-1 fuzzy sets for all their membership functions. The fuzzifier block in Figure 6 initially creates fuzzy sets from the measured crisp inputs. Since fuzzy sets rather than numerical values are used to create the rules in the FLS, this step is essential. There are three different types of fuzzifiers accessible in an interval type-2 FLS. When the noise is stationary, measurements can be represented as a precise pair, as a type-1 fuzzy set when the noise is non-stationary (which is not conceivable in a type-1 FLS), or as an interval type-2 fuzzy set. The inference block fuzzifies the input fuzzy sets before transferring them to the fuzzy output sets. In this process, each rule's output is determined by employing an inference mechanism after each rule has been quantified using fuzzy set theory. The inference block activates a subset of rules based on the fuzzy input sets, and each rule is inferred separately. One or more fired-rule fuzzy output sets make up the inference block's output. The FLS's final output is frequently used in engineering applications when a numerical value rather than a fuzzy set is desired. The output processing block in Figure 5 is responsible for tuning the fuzzy sets produced by the fired-rule algorithm into a numerical value. This is accomplished in a type-1 FLS by defuzzification, which uses techniques like determining the membership function's center of gravity or calculating a weighted average of the centers of gravity of the rule consequents.

For an interval type-2 FLS, it is more difficult and takes two steps to convert an interval type-2 fuzzy set into a numerical number. The interval type-2 fuzzy set is converted into an interval-valued type-1 fuzzy set in the first stage of type-reduction. For this, type-reduction strategies are employed, such as the KM algorithm created by Karnik and Mendel. The type-reduced set's two endpoints are averaged to get the defuzzified value in the second stage, referred to as defuzzification [25, 29]. Figure 7 shows that the type-reduced set and sharp numerical values may both be produced by an interval type-2 FLS. The latter measures the uncertainties processed through the FLS due to unknown input measurements setting off rules with unknown antecedents, consequents, or both.

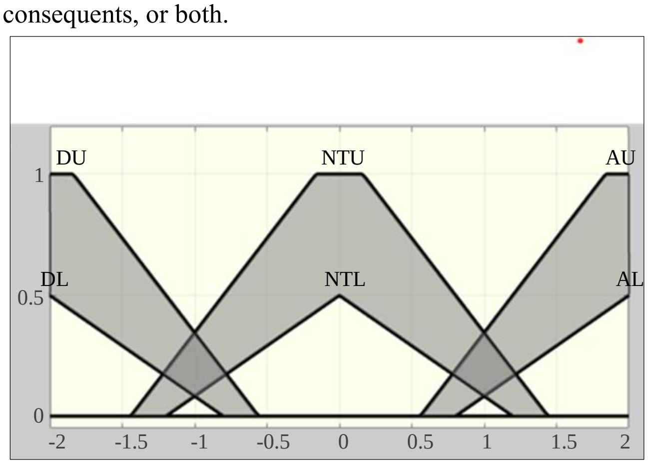

Fig. 6 Membership function of IT2FLC -error

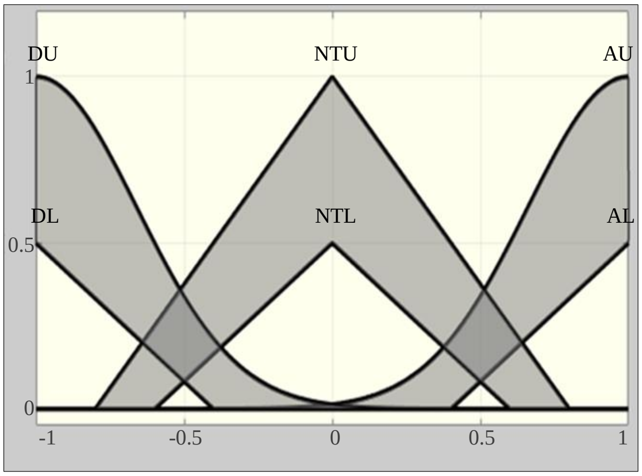

Fig. 7 Membership function of IT2FLC-change in error

Table 1. Rule base for IT2FLC

E / **CE**	**D**	**NT**	**A**
D	D	D	NT
NT	D	NT	A
A	NT	A	A

Key assumptions in the simulations using Matlab/Simulink were normalizing input data into a unit hypercube and designing the initial fuzzy model using subtractive clustering. During the training phase, membership functions were optimized, with subsequent parameters estimated using least squares and premise parameters modified using gradient descent. To validate the model, real-world data were compared to simulated outputs using the Root Mean Square Error (RMSE) as the major evaluation criterion. The model was considered appropriate if the RMSE was minimized, and its performance remained consistent after removing less relevant input variables, confirming its fit with real-world behavior.

4. Multilevel Inverter

For the traditional diode clamp model to produce a 19-level multilevel output, it would require 4 capacitors, 18 diodes, and 24 switches. At least five H-bridges would make up the traditional cascaded H-bridge. To generate a 19-level multilevel output, at least 20 switches, or four switches per H-bridge, would be necessary. In order to generate the 19-level multilevel in our hybrid topology (a combination of diode clamp and Cascaded H-bridge), we utilized 16 switches, 8 diodes, and 4 voltage sources, shown in Figure 8. The switching of these switches is done mainly by regulating the switching signals.

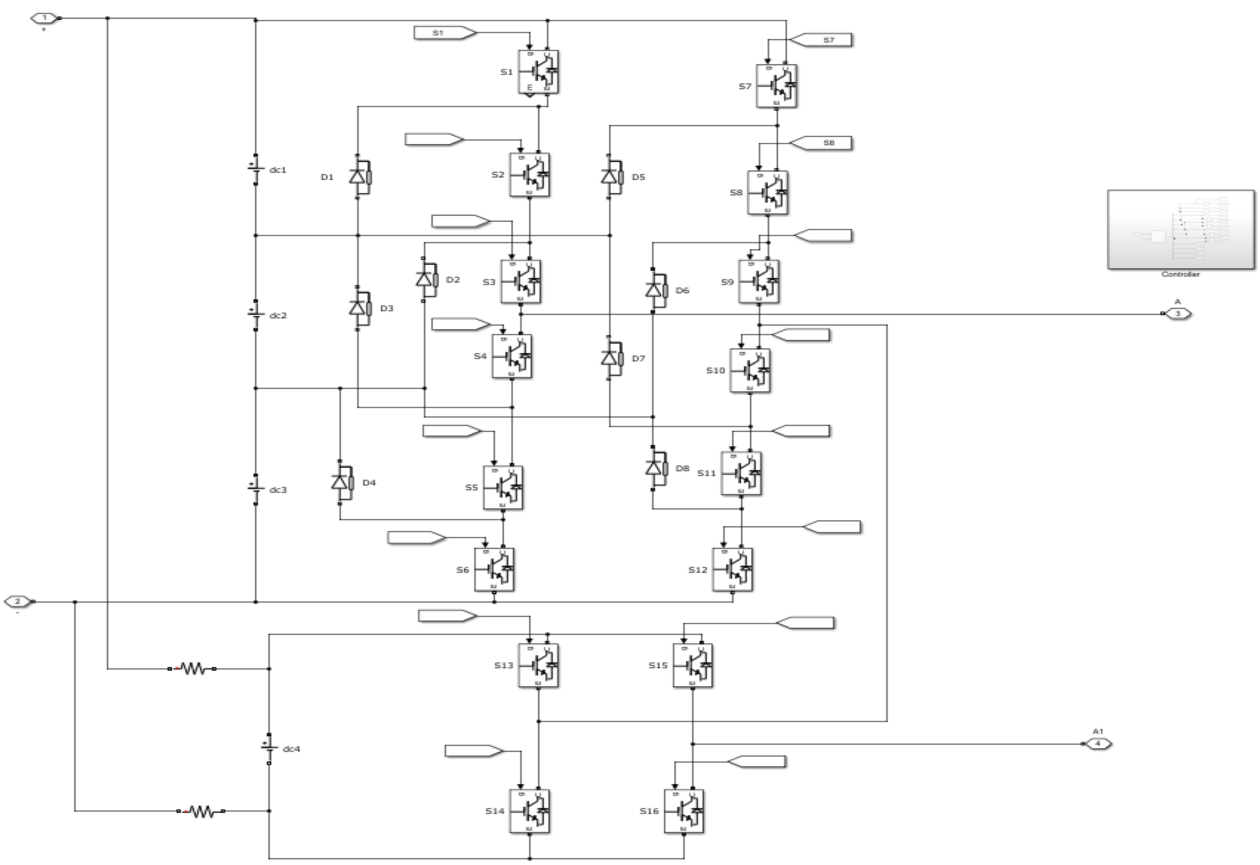

Fig. 8 Simulink model of 19-level inverter

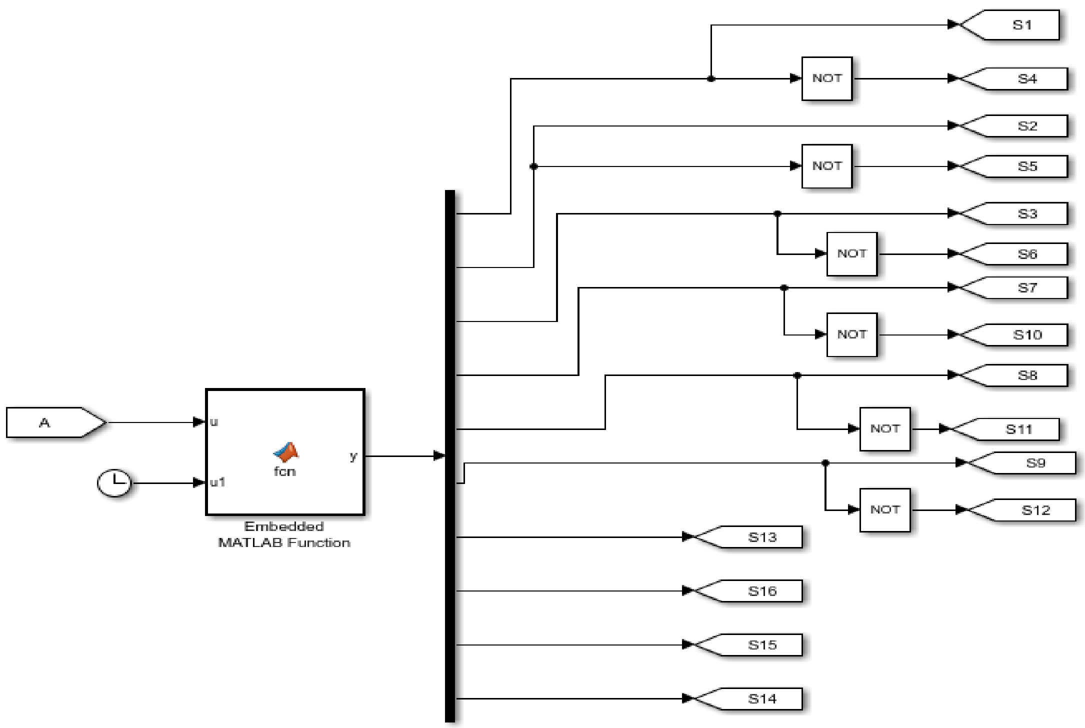

Fig. 9 Control structure for 19-level inverter

Figure 9 shows the control structure for the 19-level inverter, where 10 control signals control the 16 switches. The switches S1&S4, S2&S5, S3&S6, S7&S10, S8&S11, S9&S12 are in pair. Each of these pairs will be assigned a control signal, and the rest of the switches, S13, S14, S15, and S16, are controlled by a control signal each. For their switching, the input variables are formed up of two parameters: ‘u1’, which stands for a reference value and ‘u’, which represents the amount of time consumed or another time-related parameter. The code uses the value of t, the absolute value of u, to determine which range u falls into based on the logic given for each level.

5. Results and Discussion

The system exhibits a clear link between the changes in voltage and current levels in the measured waveform during the voltage sag (0.5-0.6s) and swell (0.8-0.9s). The increasing current waveform indicates that the source voltage declines during the voltage sag, which causes the source current to rise to preserve the power balance. Conversely, as the current waveform is reduced during the voltage swell, the source voltage spikes and the current drops proportionately to avoid overvoltage. By smoothing out the waveforms and guaranteeing that the load voltage is steady and distortion-free, the system’s 19-level multilevel inverter successfully reduces these oscillations. The inverter facilitates this dynamic voltage and current adjustment, which guarantees optimal power quality and harmonic reduction during the fault conditions, showcasing the system’s ability to handle voltage variations efficiently.

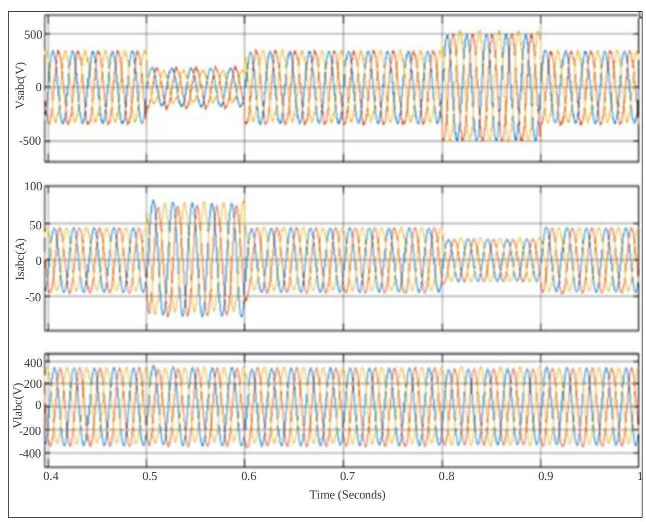

Fig. 10 Waveforms of voltage sag and swell and mitigated waveform (AFLC)

The 19-level waveform in the previous Figure 11 is visible. The system was given a value of 700V because the calculated Vdc value was roughly 680V. Even variations in the Vdc value can be seen under fault conditions.

Figure 12 depicts the waveform of the load current for the three different phases, Phases A, B, and C, respectively. It is nearly a pure sinusoidal wave, which denotes the quality of the current delivered to the load with the least amount of harmonics.

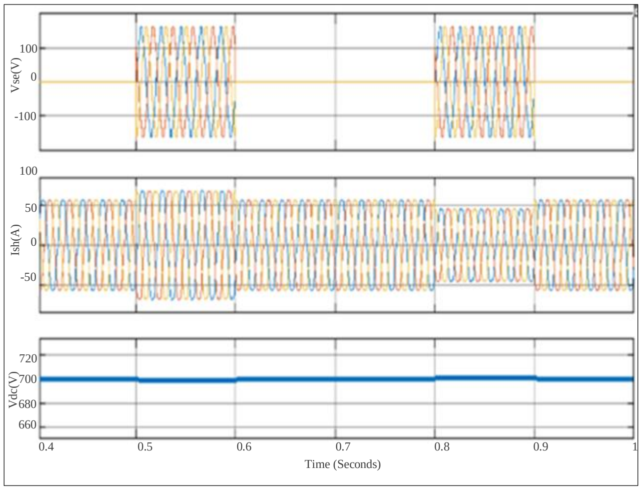

Fig. 11 Multilevel inverter output (AFLC)

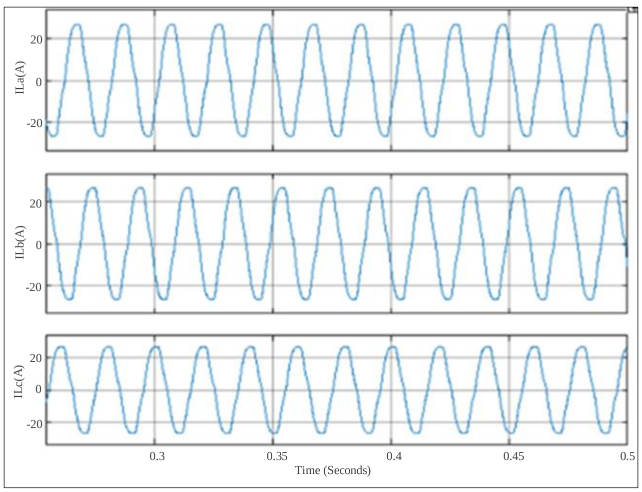

Fig. 12 Load current waveforms (AFLC)

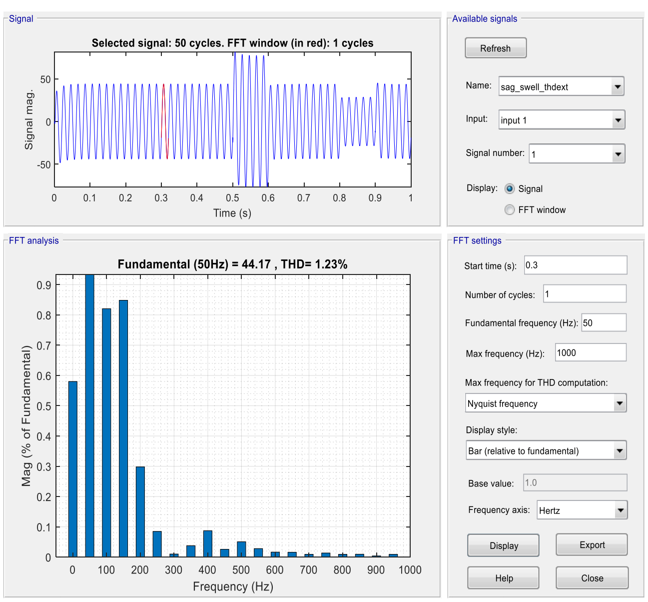

Fig. 13 Source current THD (AFLC)

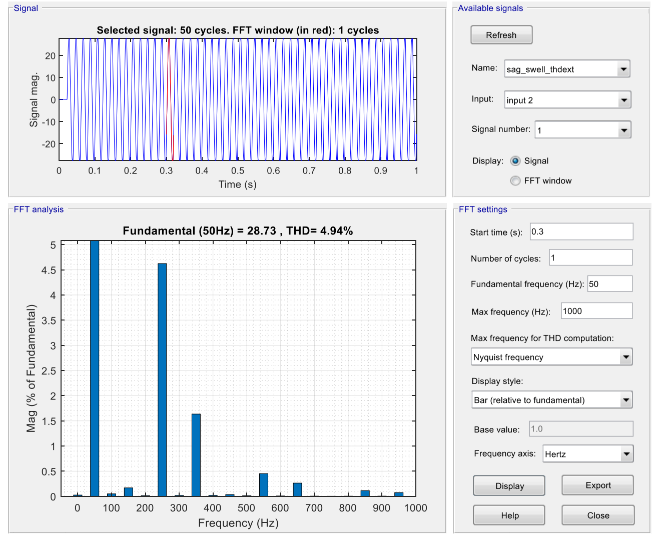

Fig. 14 Load current THD (AFLC)

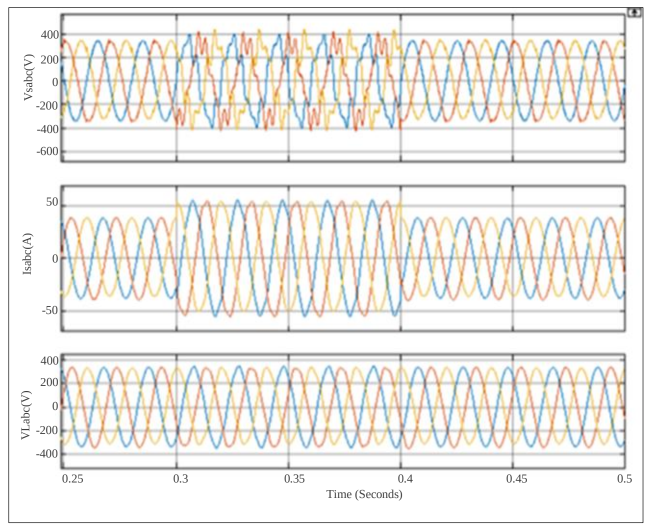

Fig. 15 Voltage harmonics mitigation (AFLC)

The IEEE 519 standard, formerly known as IEEE Recommended Practices and Requirements for Harmonic Control in Electric Power Systems, sets acceptable harmonic distortion limits in electrical systems for ensuring grid-connected equipment compatibility, operational reliability, and power quality. According to the short-circuit ratio at the Point of Common Coupling (PCC), Total Harmonic Distortion (THD) is stipulated for voltage not surpassing 5% and for current stay within predetermined bounds.

These limits preserve system efficacy throughout various operating circumstances by curbing harmonic interference. According to the FFT analysis of the above-improvised system, the current harmonics mitigated on the source side account for 1.23% and on the load side sum to 4.94%, respectively. As seen in the above figure, this improvised UPQC system was also employed to reduce voltage harmonics.

Fig. 16 Source current THD (Voltage Harmonics-AFLC)

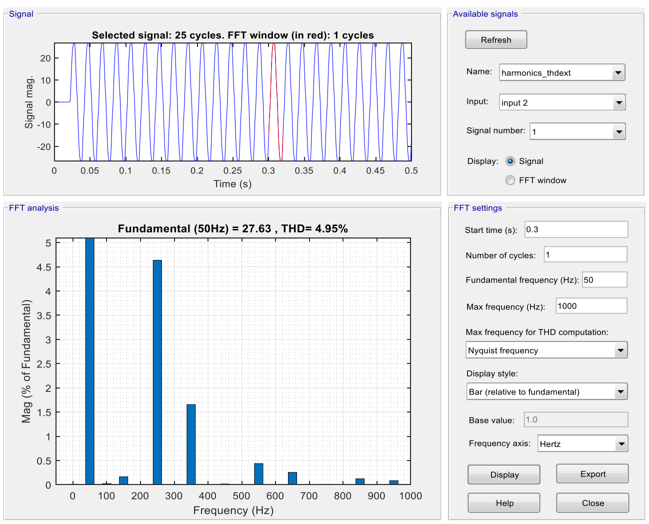

Fig. 17 Load current THD (Voltage Harmonics-AFLC)

The final load voltage waveform, which is free of distortions, is also made very clear after passing through the developed UPQC system, as well as the distorted voltage waveform during the timestamp from 0.3 to 0.4s on the source end prior to passing through this improvised UPQC system. The FFT analysis was also carried out on this system, designed to reduce voltage harmonics. The results are exceptional, as shown above, with the source current's total harmonic distortions coming in at 3.53% and the load current's being calculated at 4.95%.

6. Environmental Impact and Sustainability

The deployment of UPQC systems, particularly those with complex components such as 19-level Multilevel Inverters (MLIs), has both good and detrimental impacts on the environment. During operation, UPQC systems control power quality by adjusting for voltage sags, swells, and harmonics, which can indirectly minimize energy losses and enhance grid efficiency. However, the system requires energy to function, particularly during compensation periods. For example, while addressing voltage sags, the system may require extra energy from the source to maintain voltage levels, increasing the demand on power plants. In terms of lifecycle consequences, producing UPQC components such as inverters and capacitors releases greenhouse gas emissions due to the energy-intensive procedures required in procuring materials (e.g., copper, silicon) and creating semiconductors. Furthermore, if these components are not properly disposed of, they might generate waste. However, multiple inverters reduce switching losses, resulting in lower heat dissipation and higher efficiency, lowering long-term energy usage. Proper maintenance and recycling measures, such as extracting precious metals from inverters, can decrease environmental effects throughout the system's lifespan. The total environmental advantage is visible in long-term efficiency improvements, particularly smart grids that optimize energy flow and decrease waste.

7. Conclusion

The use of an AFLC controller with the proposed 19-level Multilevel inverter has substantially enhanced the performance of the UPQC in this work. The harmonic distortion was effectively decreased to 1.23%, far below the IEEE 519 standard limit of 5%, to achieve better power quality and fully adhere to regulatory standards.

7.1. Future Scope

Future research may investigate the integration of the proposed 19-level Multilevel Inverters (MLIs) with Deep Reinforcement Learning (DRL) as an innovative approach to power system problems and smart grid advancement. DRL enhances stability, fault resilience, and renewable integration while optimizing MLI switching to achieve ultra-low THD and IEEE 519 compliance. Its real-time flexibility facilitates demand response, DER management, and decentralized smart grid operations, providing an intelligent and sustainable energy framework that is in line with the demands of the power system in the future.

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