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Original Article

Design and analysis of Delay Controllable Reconfiguration ALU Using FinFET and CNTFET

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Abstract *- The Arithmetic and Logical Unit (ALU) is the central functional programmable logic block in real-time ICs. Traditional Arithmetic Logic Units (ALUs) have been developed utilizing CMOS technological devices, leading to high power usage, delays in processing, and many devices. This work addresses the conceptualisation and subsequent investigation of a delay-controllable reconfiguration ALU using FinFET and CNTFET technologies. The first development entails the establishment of a novel COPFA and CISFA using multiplexing selection circuitry. Consequently, these adders are used to create delay-controllable adders and delay-controllable subtractors. The Delay controllable reconfiguration ALU can be generated by incorporating the arithmetic and logical functions. The computational findings demonstrate that the suggested nanotechnology-based designs surpassed the traditional adders and subtractors regarding reducing power and latency. The power consumption of the proposed CNTFET 4-bit ALU is atleast 32% lower than that of the existing 4-bit ALUs. The delay period of the CNTFET4-bit proposed ALU has been reduced by 50% compared to the existing ALUs.*

Keywords *- ALU, Power usage, Delay, FinFET, CNTFET, Reconfigurable adders.*

1. Introduction

In the last few decades, there has been a demand to reduce digital circuits' size and power usage by conserving time while boosting speed performance. The basic digital circuits are designed using adders and multipliers as their foundational components. Moreover, these components are often used as distinct modules in Digital Signal Processing (DSP) and Arithmetic Logic Unit (ALU) systems. Digital Signal Processing (DSP) encompasses techniques such as spectral analysis, digital filtering, Fast Fourier Transform (FFT), and Discrete Fourier Transform (DFT) to enhance and analyze digital communications. The power usage performance depends on the operation of the adder. With the VLSI sector, there is rapid progress in developing sections for efficient electronics, particularly for low-power arithmetic circuits. Enhancing power and area usage of high-speed data path design is a research field focused on optimizing its design. The speed of the adder is constrained by the time required for carry propagation when using digital adders [1, 2]. The state of each bit is sequentially generated in a consistent sequence inside an adder circuit and propagates a carry onto the following location. ALUs are essential components for several high-performance systems. The efficiency of a system is determined by the efficiency of the multiplier, which is the largest and slowest element in the system. Therefore, optimising the multiplier's speed and area is essential. Various techniques and concepts have been developed to achieve a more favorable balance between area and speed since these two factors impose conflicting constraints. In addition, numerous DSP applications are targeted for portable devices, so battery life and power consumption are important constraints in the design process [3, 4]. In VLSI designs, power efficiency has become the primary design criterion since the power optimisation capacity of a circuit significantly influences its overall efficiency. The ALU is the fundamental component of microcontrollers, microprocessors, and digital computers, executing all calculations and operations. Over recent times, the demand for low-power, portable devices has surged significantly. The miniaturisation of MOS transistors to the nanoscale has encountered unavoidable and severe short channel effects. Moreover, traditional CMOS design topology results in significant power loss. Nonetheless, the power usage for circuits based on CNTFET may be significantly decreased [7]. To enhance the energy utilisation of arithmetic circuitry within processors, getting an energy-efficient ALU architecture is essential. In the design of an energy-effective Arithmetic Logic Unit (ALU) for more complex adders, a critical consideration is the reduction of total power consumption. The key factor that improves energy efficiency within computational fundamentals is the reduction in dynamic power consumption. Enhanced leakage current within discrete devices produced in VLSI ICs substantially

increases static power consumption. To develop an energy-effective ALU cell, it has become essential to concentrate on minimising both static and dynamic power consumption. This is readily demonstrated by the next examination of power dissipation within circuits using CMOS technologies [8]. The quiescent power usage has significantly increased due to a significant rise in current leakage within the discrete circuits manufactured within VLSI IC. To develop an energy-effective ALU module, it is necessary to focus on reducing static and dynamic power utilization. This was demonstrated in the subsequent discourse regarding power dissipation within CMOS-based circuitry. In the past few years, FinFET, Carbon nanotube FET (CntFET), and RibbonFET have been extensively employed in many applications to enhance the efficiency of area, power, and latency. The manipulation of the parameters of various layers, including dimensions, thickness, temperatures, current, voltages, fabrication elements, gate oxidation, and the introduction of additional terminals, are modified to create these improved FET models. Consequently, this investigation examined the FinFET and CNTFET versions to develop a variety of computations.

This work has the following main features: First, a Modified Full Adder (MFA) is designed with 10 transistors and multiplexer select logic. Subsequently, the Carry Input Selectable Full Adders (CISFA) and Carry Output Predictable Full Adders (COPFA) have been established by altering the MFA's carry input and carry-out functions. In addition, we have designed a 4-bit delay-controllable adder and subtractor employing MFA, CISFA, and COPFA components. The delay-controllable subtractor has been built by employing the two complementation addition characteristics as a fundamental component. The 4-bit delay-controllable adder and subtractor modules are expanded to include reconfigurable features, creating N-bit representations of delay-controlled reconfigurable hybrid adder, subtractor, and adder-subtractor. A delay-controllable reconfigurable ALU has been constructed using delay-controllable adders and logical operations employing FinFET and CNTFET technology. Simulation outcomes demonstrate that the suggested models surpass traditional adders and subtractors in reducing area, power, and latency. The remaining sections of the paper are presented as follows: Section 2 focuses on the literature review and addresses the issues at hand. Section 3 pertains to the suggested approach. Section 4 pertains to the analysis of simulation outcomes and subsequent discussions. Section 5 closes by discussing potential areas for future development or expansion.

2. Literature Review

This section thoroughly overviews numerous adders produced during the last several years. The investigation focuses on the examination of hybrid adders. Within this addition method aimed at enhancing speed, a Radiation-Hardened Majority-Driven Magnetic Full Adder (RHMFA) [9] has been created and implemented. When examining approximation adders, it is seen that using FinFET technology results in about double the speed of standard RCA additions. In their study, the authors in [10] designed approximation adders that demonstrated an efficient layout but slower speed. On the other hand, the carry look ahead method resulted in quicker performance but required a larger footprint. In order to address the problems of power usage, along with delays within 4-bit and 8-bit CNTFET Ternary Full Adders, a novel strategy has been proposed [11]. This approach does not use Mux and instead utilizes approximate adders. Simulations showed that the modified structures performed better than conventional methods. The authors in [12] designed an integrated FinFET Full addition architecture for processing images and video tasks.

The design of the adder demonstrates the gate width and incorporates two separate RCAs having inputs of zero and one, correspondingly. In their study, the authors in [13] introduced the PTL dependent subtractor using gate-level changes, resulting in fewer gates needed to carry out the processes in their suggested research. It offers both area reductions and overall power optimization. The evaluation outcome indicates that the circuit outperforms the others in terms of efficiency and speed. The ternary adder and 1-trit multiplication design were designed [14] and assessed for their performance with dimension, power, and latency. A straightforward and effective improvement at the gate level results in decreased power consumption, reduced area, and minimized delay when using the Trit Ternary Subtractor [15]. The effectiveness of the modified CSLA was assessed in conjunction with those produced by different adders. The high-speed capabilities of TUTS have been utilized for mathematical operations in computational units.

The authors in [16] introduced a CNTFET adder as well as a subtractor that demonstrates both outstanding performance and a compact architecture, although at the expense of increased area consumption. Furthermore, CNTFET may be easily used in low-power multiplication. The simulation outcomes demonstrated greater efficiency than conventional adders utilising FinFET technology. In their study, the authors in [17] introduced a novel FinFET Hybrid Adder/Subtractor Circuits that offers minimal error efficiency. This circuit exhibits a linear relationship between delay time and the number of bits (N), meaning that the addition algorithms in this circuit can perform the maximum delay procedure. Typically, it yields quicker results via a more prolonged procedure than other adders. Its provision is a substantial quantity of logical gates and a high fan-in. The authors in [18] designed an 8-bit Dadda multiplier employing 14 nm FinFET semiconductor technology and an approximated 4:2 compressor. Carry propagation addition algorithms are developed using a 4:2 compressor to decrease the vertical size of the output rows. The authors in [19] constructed the Majority Imprecise Multiplication using 7 nm FinFET technology. The multiplier uses enhanced quantum

dot cell automata to generalize majority logic interpretations. Partial product eliminations have been achieved using hybrid compressors that include most logic gates. The authors in [20] devised an approach for constructing an area-efficient FinFET-approximation multiplication. This methodology operates at minimal voltage and minimizes current consumption within the circuitry. These modifications were made for an existing functioning EETM and currently operational conveyors. An N-bit ALU [21] has been built employing 18 nm FinFET technological advances. It mostly performs addition operations and is designed to prioritize speed, making it a crucial performance indicator. Digital circuits featuring outstanding performance are consistently valued and prioritized. This approach is experiencing significant difficulties with computation.

The authors in [22] engineered a high-speed 8-bit Arithmetic Logic Unit (ALU) called HS-ALU utilizing 18 nm FinFET technological devices. This ALU was constructed on the principles of the Kogge Stone additions and the Dadda multiplier. This procedure is often found in many real-time DSP systems. However, it requires a significant amount of power. The authors in [23] created the FALU-32, a 4-bit ALU based on 32 nm-FinFET technology. This ALU was constructed utilizing array multipliers and carry save adds. The power consumption of the FALU-32 circuitry has to be reduced for two specific reasons: to minimize heat dissipation as well as to maintain a large number of operations necessary for managing the IC. Moreover, the available research presents alternative designs that run the device at reduced voltages to minimise power consumption; however, decreasing the power supplied diminishes the cell's drive capability and negatively impacts voltage scaling across numerous components. This study emphasises researching the functioning of effective reconfigurable ALUs in terms of area and power and utilises numerous key methodologies to evaluate ALU performance. The anticipated performance of the ALU has been assessed against the major ALU designs listed above.

3. Proposed Delay Controllable Reconfigurable ALU

ALUs constitute the fundamental components of any electronic circuitry, and their performances determine the efficiency of many different applications. Therefore, proper adder implementation will boost processor and controller performance. The present section provides a comprehensive study of the development of the delay-controlled reconfigurable ALU, created by utilizing the delay-controlled reconfigurable adder, subtractor, and multiplier, respectively. Furthermore, these adders are constructed using the MFA, COPFA, and CISFA units. Figure 1 depicts the block schematic of MFA, featuring two multiplexer devices for sum and carry generation. Cin serves as the selection source for the MUX21, which provides the overall result determined by the data selection mechanism for XOR and XNOR outputs.

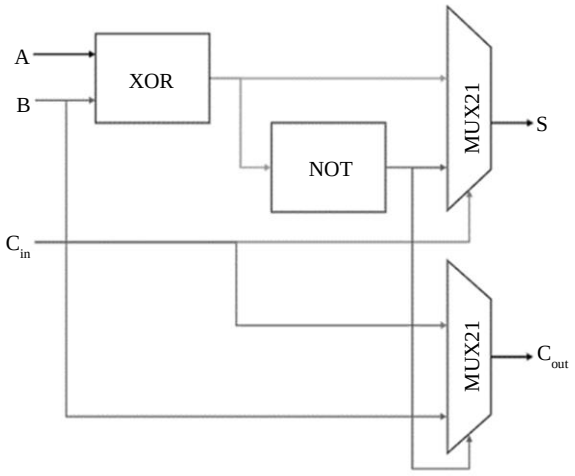

Fig. 1 Block schematic of the MFA

Furthermore, the XNOR of inputs A and B can be utilized as a selection input for the MUX21-A, creating the carry outcome according to data selection criteria. Subsequently, the carry result of the MFA was generated. An important benefit of CISFA has been its inherent capacity to choose the carry inputs. The degree of complexity of the adding operation is mainly determined by the production of carries and the kind of forwarding. The efficient execution of -bit adders may be achieved by reducing the number of operations required for various carry inputs. Overall, the CISFA unit considers the selected additional carry input (Cins), which is distinct compared to the initial carry input (Cin). Figure 2 depicts the block architecture of CISFA, which is derived from the basic principles of MFA, with an additional OR gate. At first, Cins & Cin were utilized as inputs for MUX21, a component employed to choose both carry inputs. Whenever inputs A and B have the same value, MUX21-A will provide the output Cins. When inputs A and B have values that are not equal, the result produced by MUX21-A (OUTA) serves as the selection input for MUX21-A, resulting in the sum result using XOR-XNOR selection circuitry.

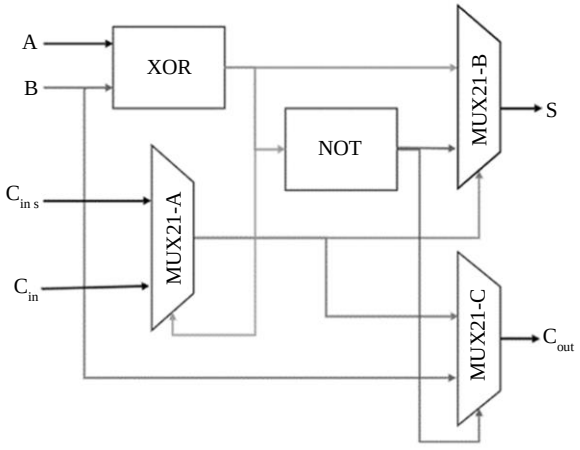

Fig. 2 Block schematic of the CISFA

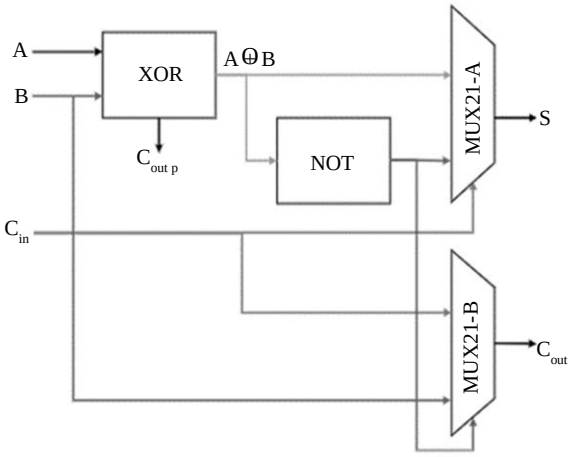

Fig. 3 Block schematic of the COPFA

In addition, the XNOR operation is used to pick both inputs A and B for the MUX21-A. This selection determines the output of the carry operation depending on the input data selection mechanism. An important benefit of COPFA has been its ability to forecast two carry outcomes: the carry result (Cout) and the expected carry outcome (Coutp). The carry outcomes serve as sources to operate the CISFA component, enabling rapid data shifting. The schematic representation of COPFA, as seen in Figure 3, incorporates an XOR-AN component in place of the XOR gate. This component produces both XOR and AND outcomes, with the AND signal serving as the interim carry result. Cout often arises when at least two instances of a single input data exist. This interim carry out function serves to verify the presence of ones and then produce the Coutp. Figures 4, 5, 6 and 7 represent complete swing logic based XOR gate, NOT gate, 2X1 MUX and XOR-AND gate, respectively.

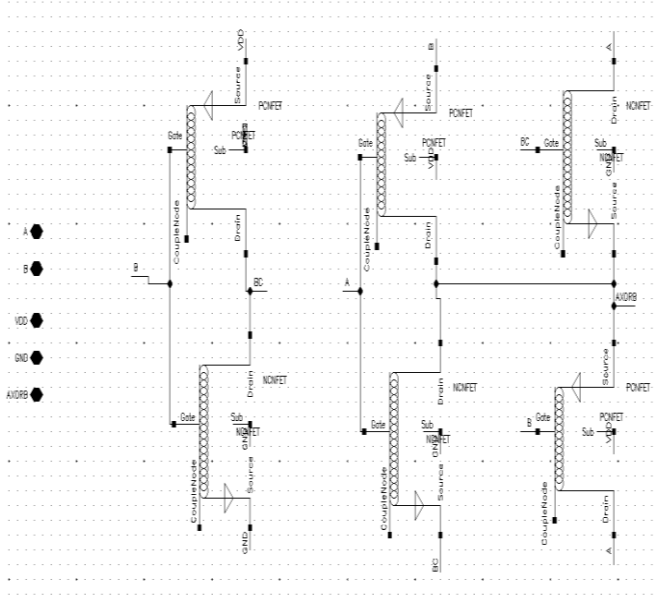

Fig. 4 CNTFET based XOR gate

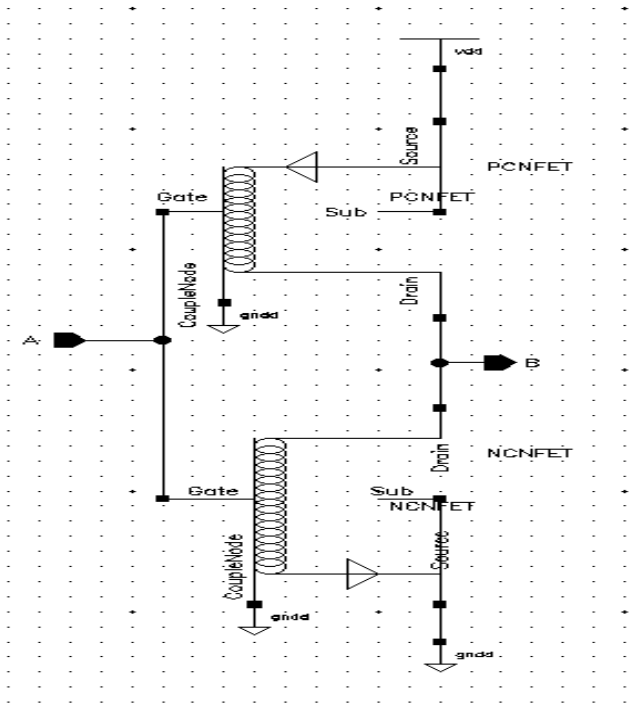

Fig. 5 CNTFET based NOT gate

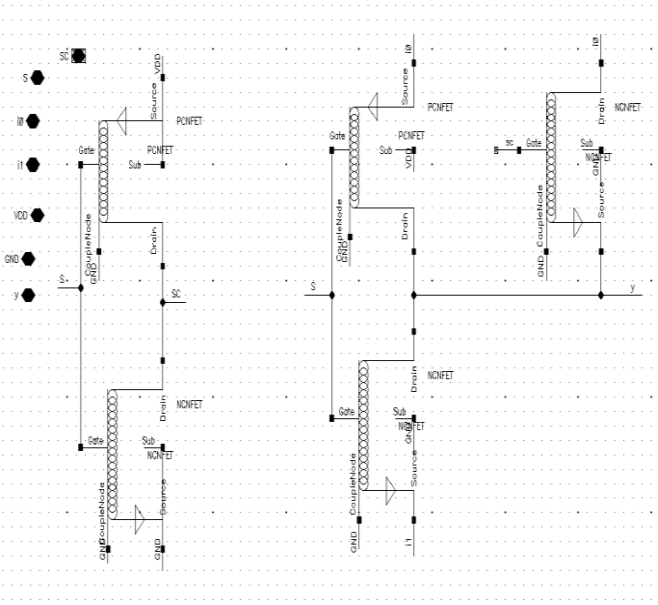

Fig. 6 CNTFET based 2 to 1 MUX

The circuits have been implemented with fewer transistors with a basic idea of GDI logic but produce full swing logic with changes to it. These figures are incorporated into Figures 1, 2 and 3 to produce corresponding adder circuits. The N-bit architecture of the suggested ALU is depicted in Figure 8. It utilizes enhanced full adders for minimal area, power usage, and delay features. In this case, A and B represent inputs with N bits, S represents the selection line containing two inputs, and OUTPUT represents the final Arithmetic Logic Unit (ALU).

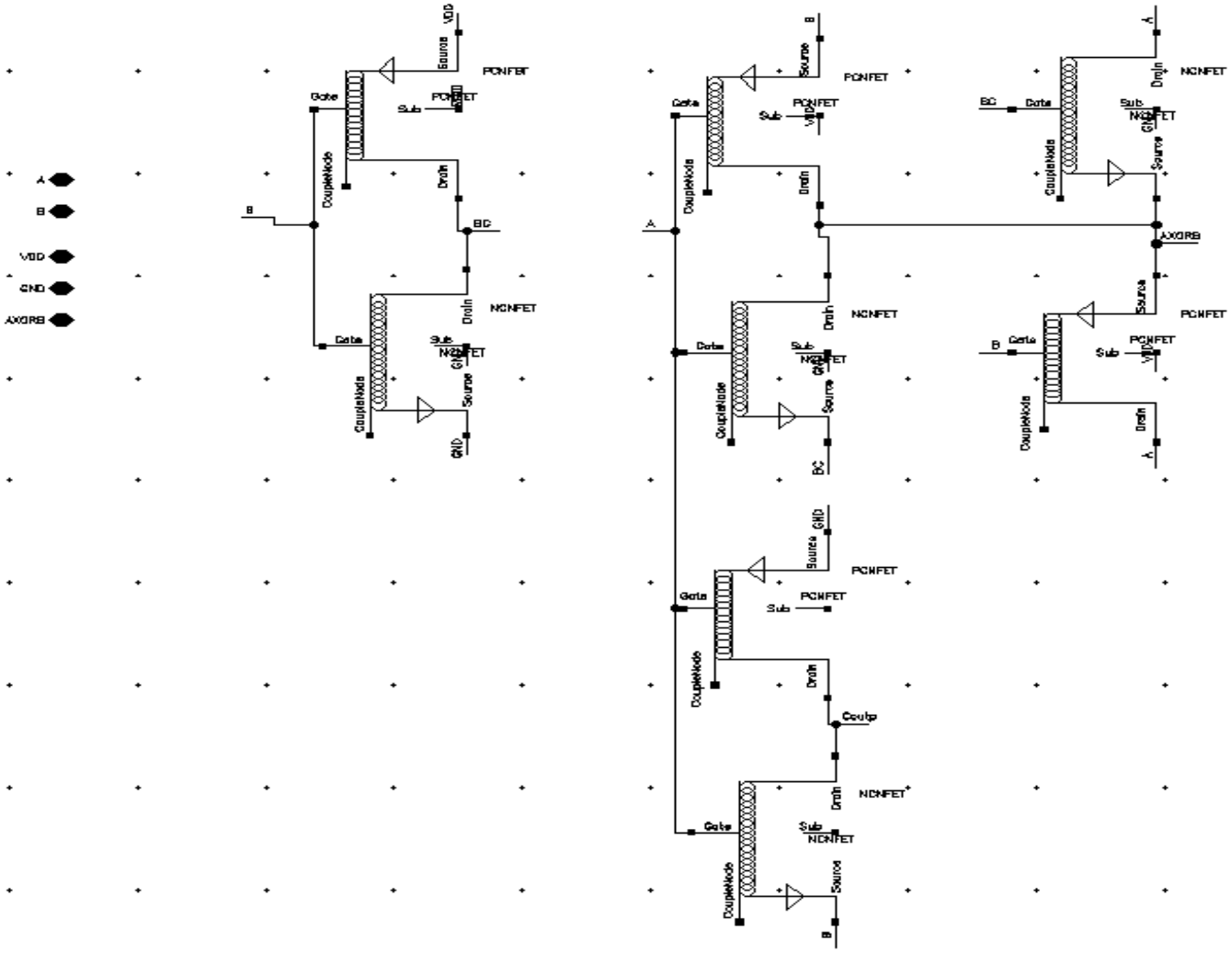

Fig. 7 CNTFET based XOR-AND gate

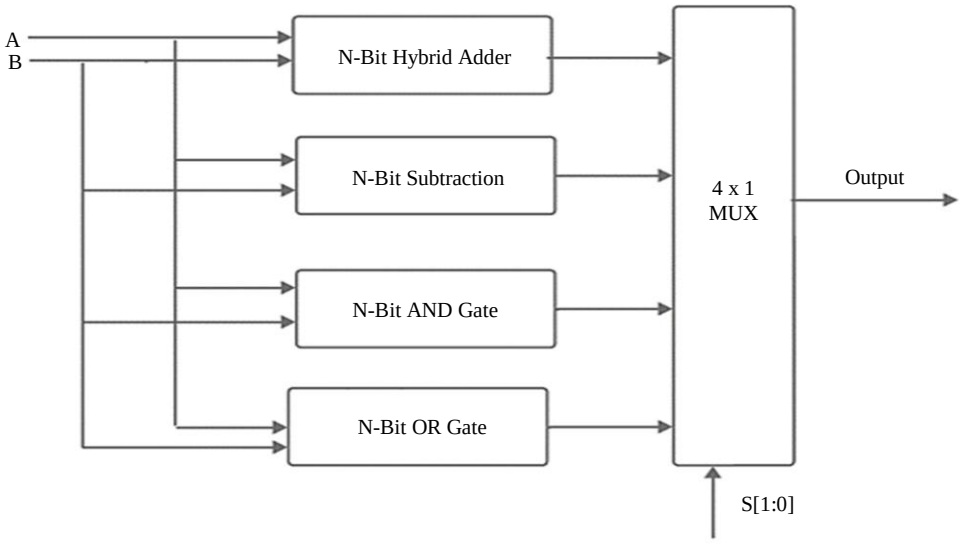

Fig. 8 Representation of proposed N-bit delay controllable reconfiguration ALU

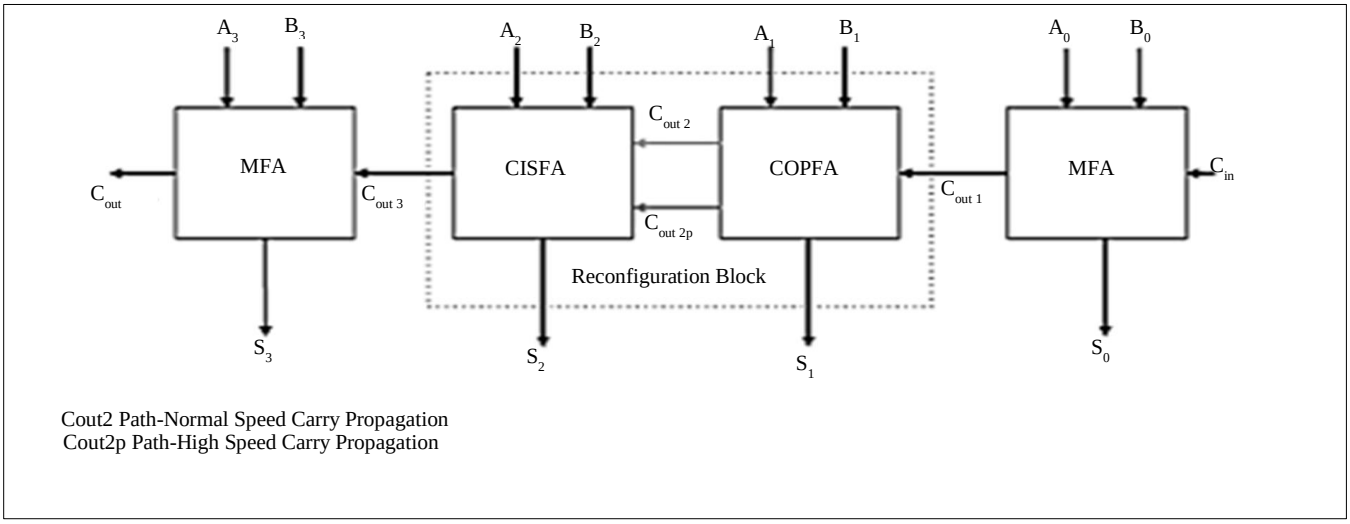

Fig. 9 Block schematic representation of 4-bit proposed adder

Table 1. Operations related to the proposed ALU

Function	Selection Inputs
Addition	00
Subtraction	01
AND gate	10
OR gate	11

Table 1 details the stages involved in each potential selection combination within the recommended Arithmetic Logic Unit (ALU).

3.1. Proposed Delay Controllable Reconfigurable Adder

The latency difficulties associated with conventional adders have been successfully resolved using the CISFA-COPFA combination. The Modified Full Adder (MFA) and MUX21 (Multiplexer 2:1) components in fundamental adders have been substituted with a CISFA-COPFA) combination. This replacement leads to a substantial reduction in the size, power consumption, and latency when compared to alternative methods. Figure 9 depicts the schematic representation of an adder that can be controlled to introduce delays. It mitigates the issues arising from the carry propagation paths. In addition, the delay-controllable addition can be developed by substituting the intermediary phases with COPFA and CISFA components. The technical functioning of the 4-bit delay control adder is demonstrated in Figure 10. The 4-bit delay controlled adder incorporates "the reconfiguration block" consisting of the CISFA and COPFA components. The reconfiguration block serves to develop the N-bit suggested addition through the repetition of several reconfiguring blocks. Moreover, the quantity of reconfiguring blocks will be determined by the total length of the N-bit proposed addition. The suggested adder uses M=(N-2)/2 reconfiguring blocks for an N-bit size. Figure 11 depicts the schematic representation of an N-bit adder that can be controlled to introduce delays.

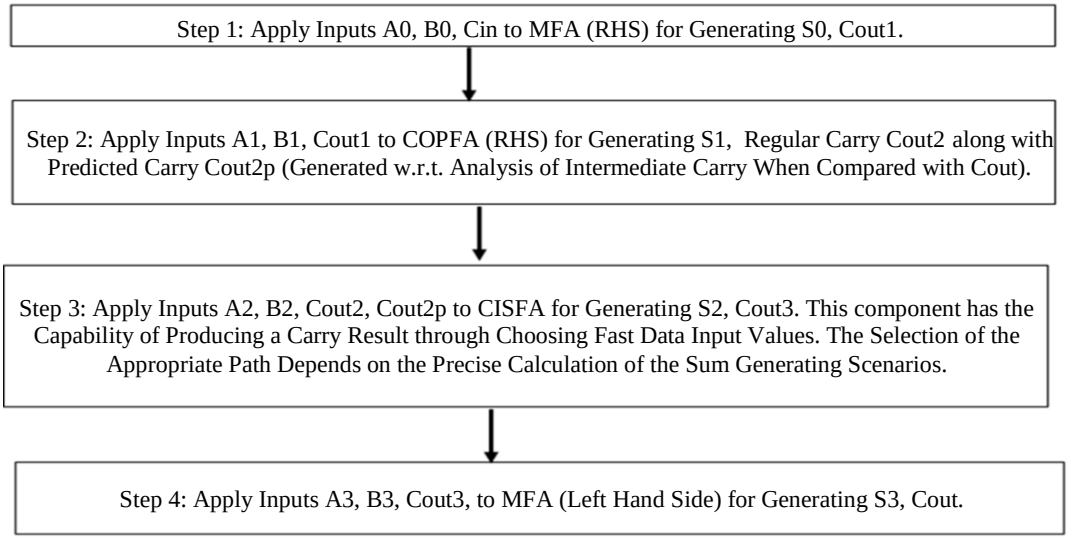

Fig. 10 Methodology of proposed Adder

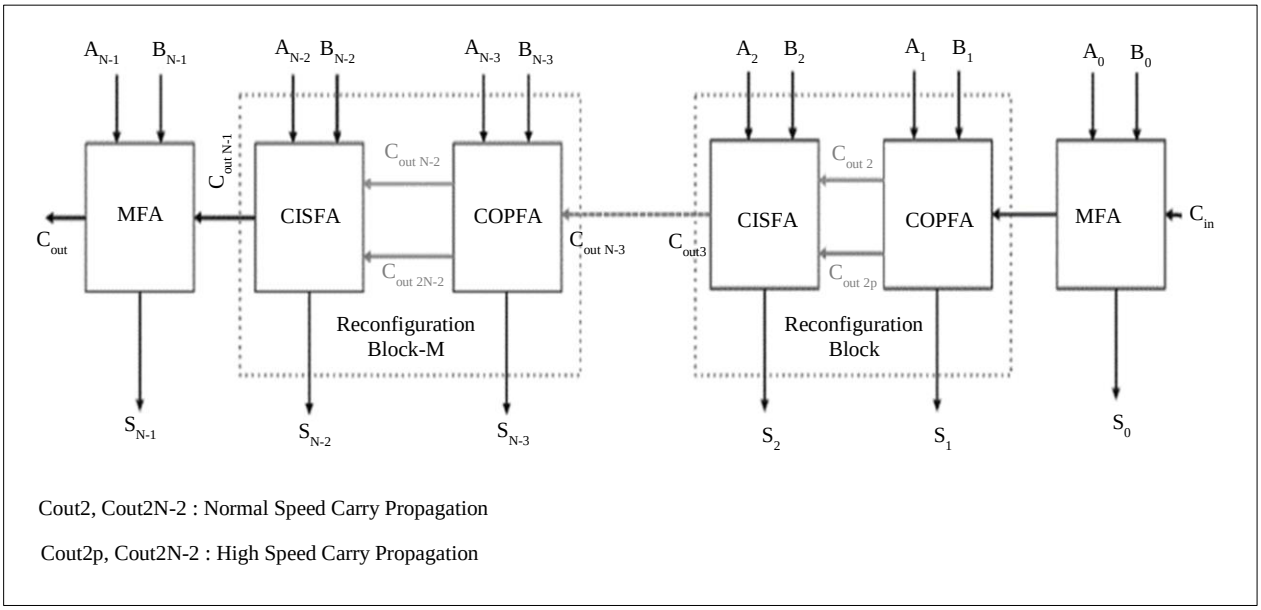

Fig. 11 Block schematic representation of proposed N-bit adder

3.2. Proposed N-bit Delay Controllable Reconfiguration Subtractor

The subsequent subsection offers a thorough analysis of suggested subtractors formed by implementing the twos complement adds technique. Therefore, complete subtractors are unnecessary when performing subtraction operations. Figure 12 depicts the schematic depiction of the subtractor, which is obtained by applying the twos complement operation to the proposed adder. The process of subtraction had been derived from the concept of addition. The primary full adder includes a control line because it functions as the first input, the input carry (CIN). The input A0 has been promptly sent to the adder. While the carry's initial value turns 1, the input B is first fed to the inverter, generating B as the output. The matching complement of B0 is represented as B0′. Hence, the process can be represented as A in addition to the complement of B0. The 2's complement subtraction of two integers A and B is computed using the formula A + B' + Cin. Whenever CIN equals 1, it indicates that the mathematical operation being performed on the four-bit data is subtraction. Figure 13 depicts the schematic representation of an N-bit adder that can be controlled to introduce delays. The technical functioning of the 4-bit delay control subtraction is demonstrated in the following manner, as shown in Figure 14:

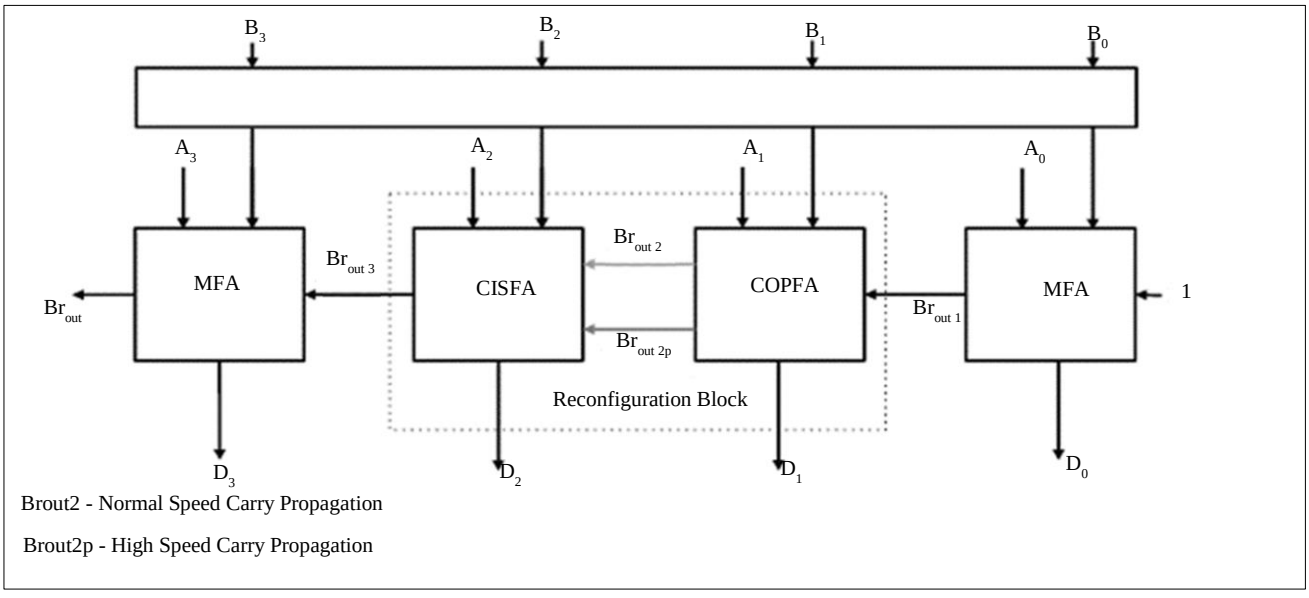

Fig. 12 Block schematic representation of 4-bit proposed subtractor

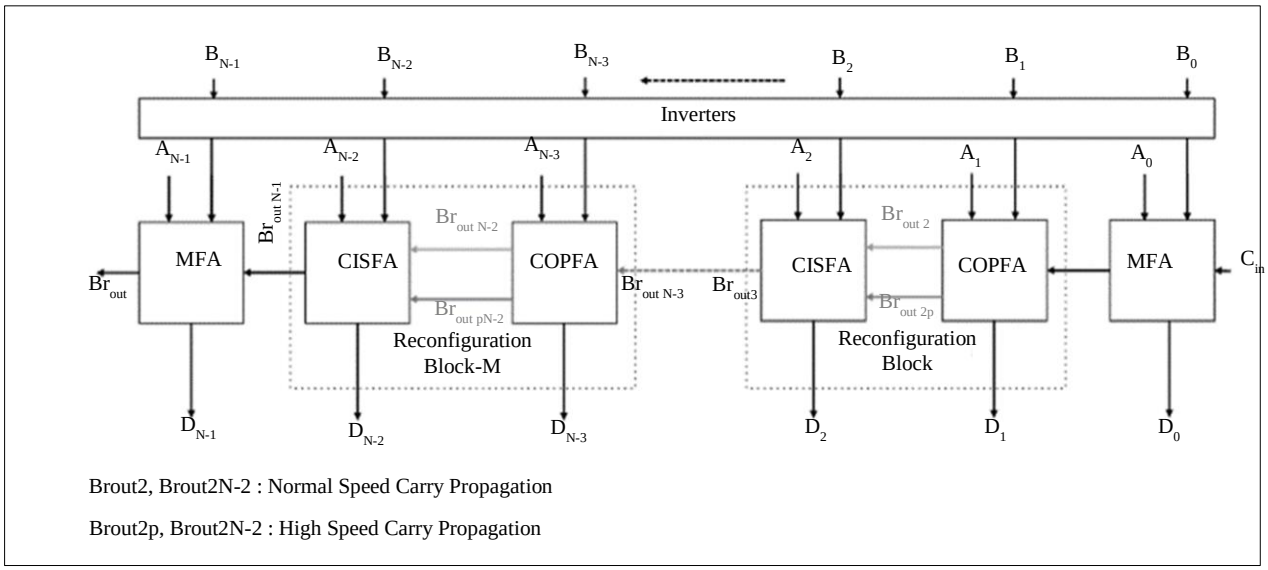

Fig. 13 Block schematic representation of n-bit proposed subtractor

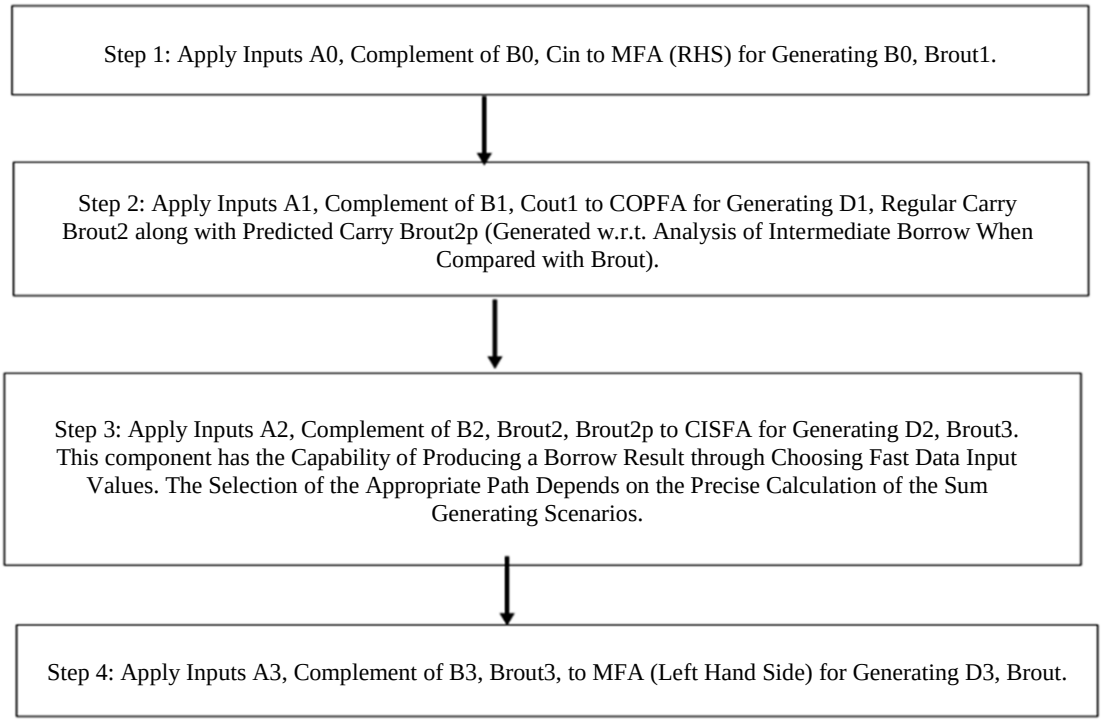

Fig. 14 Methodology of proposed subtraction

3.3. Design of 4-Bit OR Gate

The 4-bit Carbon Nanotube Field-Effect Transistor (CNTFET) OR gate is represented in Figure 15. The OR gates have been developed and implemented using Gate Diffusion Input (GDI) logic. The two inputs of the PCNFET and NCNFET are linked together in the OR gate to produce a single input, denoted as A. The PCNFET and NCNFET are correspondingly coupled to input B and VDD. Each CNTFET's drains have been connected to create the resultant node.

3.4. Design of 4-Bit AND Gate

Figure 16 illustrates the implementation of a 4-bit CNTFET AND gate. The AND gates have been developed and implemented using GDI logic. The inputs of the PCNFET and NCNFET are interconnected at the AND gate to create a single input labeled as A.

The PCNFET source is linked to the ground, whereas the NCNFET source is connected to input B. The drains of both CNTFETs are interconnected to create the output node.

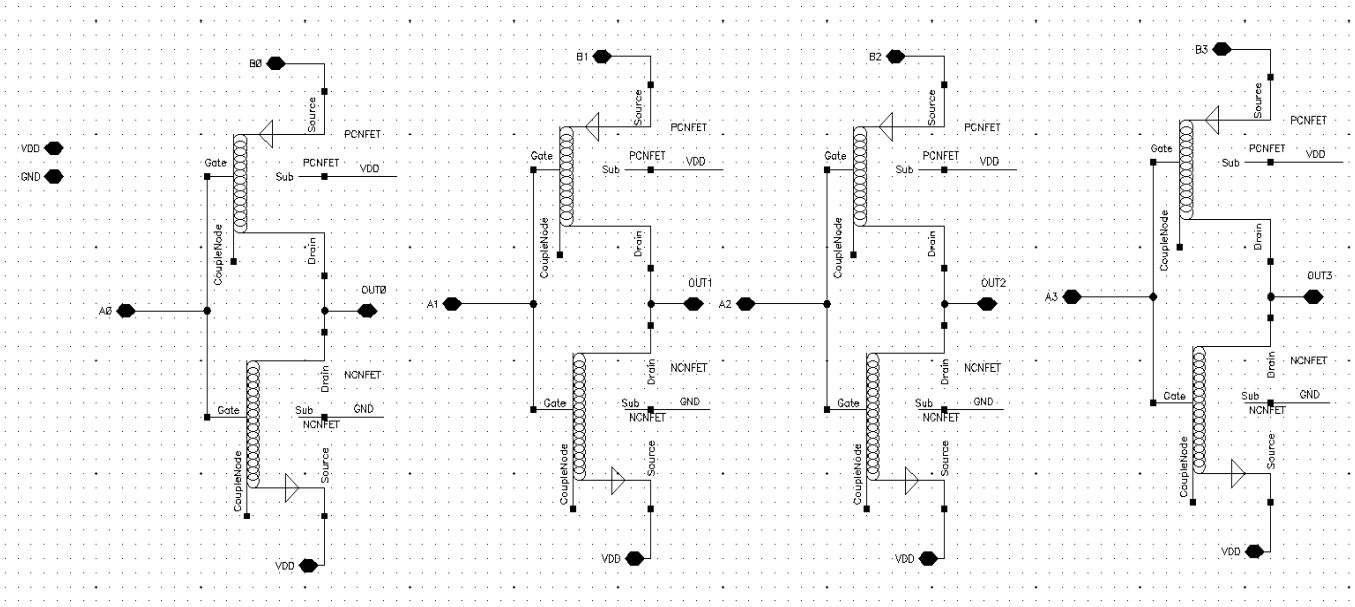

Fig. 15 Representation of a 4-bit OR gate

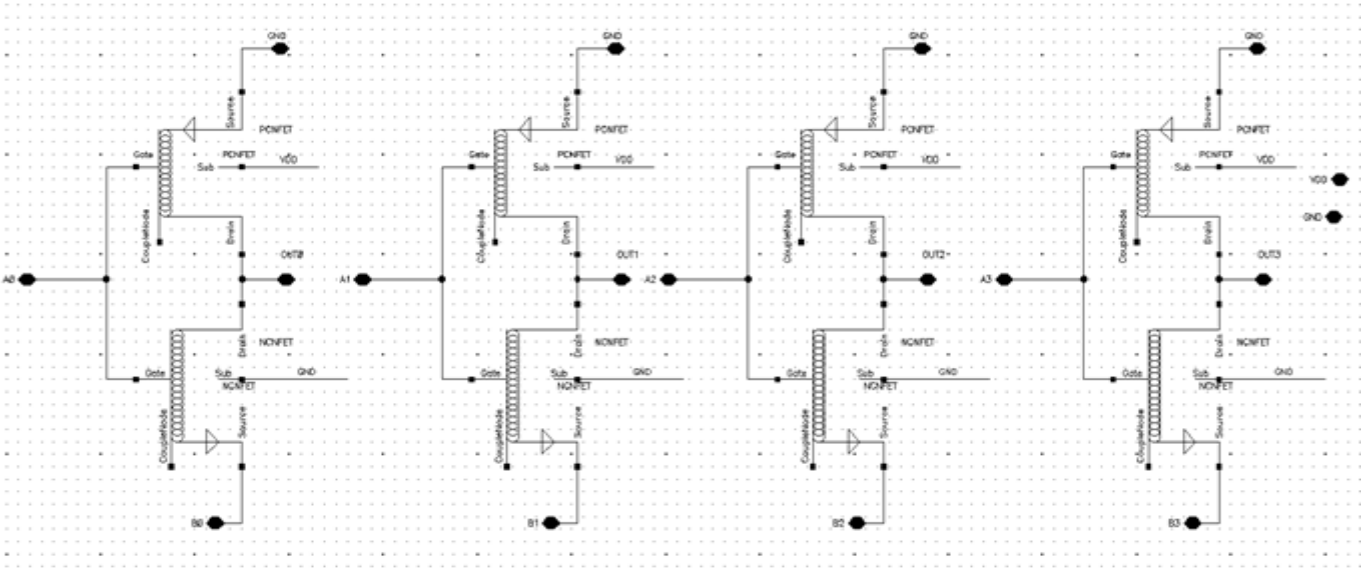

Fig. 16 Representation of a 4-bit OR gate

4. Simulation Results

The following section presents a comprehensive analysis of the simulation outcomes acquired using various variables that could potentially be utilised to showcase the proposed study's effectiveness. In addition, all of the intended tasks were executed and simulated, and the associated parameters were calculated using the cadence virtuoso tools on the corresponding FinFET and CNTFET technologies.

A comprehensive examination of the numerous simulation settings used in the conceptualization and development process of the suggested task employing the virtuoso tool is also offered. These parameters are displayed in Table 2.

Table 2. Simulation parameters

Name of the Parameter	Value
FinFET Technology (nm)	16
CNTFET Technology (nm)	16
FinFET Model	PTM
CNTFET Model	Stanford
Gate oxide thickness (Tox)	4e-09
CNTFET Channel Length (L_g)	3.2e-08
Mean path (L_{geff})	2e-07
the dielectric constant of gate oxide (K_{gate})	16
Chiral value (n1,n2)	(19,0)
Temperature during simulation	27 ^{0}C
Supply Voltage (V)	0.8

Table 3. Performance analysis of proposed ALU

Operational Circuit	FinFET			CNTFET		
	Power usage in nW	Delay in nS	PDP(x 10^{-18}) in Ws	Power usage in nW	Delay in nS	PDP(x 10^{-18}) in Ws
4- bit proposed adder	6.94	9.21	63.92	5.74	8.44	48.44
4-bit proposed subtractor	7.72	11.22	86.62	6.29	10.59	66.61
4-bit ALU	12.83	46.98	602.75	11.06	42.95	475.02

Table 4. Variation of proposed reconfigurable ALU output parameters w.r.t supply voltage

Voltage (V)	FinFET			CNTFET		
	Power usage in nW	Delay in nS	PDP(x 10^{-18}) in Ws	Power usage in nW	Delay in nS	PDP(x 10^{-18}) in Ws
0.8	12.83	46.98	602.75	11.06	42.95	475.02
0.9	14.09	43.57	613.90	13.08	39.97	522.81
1	15.96	40.85	651.97	15.97	36.05	575.72

Table 5. Variation of proposed reconfigurable ALU output parameters w.r.t change in temperature

Temperature variation (^{0}C)	FinFET			CNTFET		
	Power usage in nW	Delay in nS	PDP(x 10^{-18}) in Ws	Power usage in nW	Delay in nS	PDP(x 10^{-18}) in Ws
-25	9.18	41.08	377.11	7.9	37.78	298.46
0	10.87	43.87	476.87	9.96	39.84	396.81
25	12.69	46.79	593.77	11.01	42.11	463.63
50	13.98	49.07	685.99	14.01	45.92	643.34

Table 6. Variation of proposed reconfigurable ALU output parameters w.r.t existing architecture

	[22]	[24]	[25]	Proposed ALU
Power Consumption (nW)	24.63	14.64	17.21	11.06
Delay (nS)	117.2	87.3	88.2	42.95
PDP(x 10^{-18}) in Ws	2886.64	1278.07	1517.92	475.07

The proposed 4-bit Arithmetic Logic Unit (ALU) circuitry had been successfully built and assessed with CADENCE virtuoso software, with the Stanford - CNTFET operational characteristics described in Table 3. This study examines several measures to assess the effectiveness of the suggested designs and compares them with state-of-the-art techniques. The three factors are average energy use, propagation delay, and Power Delay Product (PDP). The proposed delay controllable reconfigurable 4-bit adder, subtractor and ALU are simulated using FinFET and CNTFET technologies employing the settings in Table 2. The corresponding outcomes are tabulated in Table 3. The findings indicate that the power consumption of the CNTFET based proposed delay controlled reconfigurable 4-bit addition, subtraction and ALU is compared to that of the FinFET based arithmetic units. The power consumption of the CNTFET 4-bit adder is 20% lower than that of the FinFET 4-bit adder. The delay period of the CNTFET4-bit proposed Adder has been reduced by 9% compared to the FinFET-derived Adder. The power consumption of the CNTFET 4-bit subtraction is 9% lower than that of the FinFET 4-bit subtraction. The delay period of the CNTFET4-bit proposed subtraction has been reduced by 6% compared to the FinFET derived subtraction. The power consumption of the CNTFET 4-bit ALU is 16% lower than that of the FinFET 4-bit ALU. The delay period of the CNTFET4-bit proposed ALU has been reduced by 10% compared to the FinFET derived ALU. The simulations were performed using a 16 nm technology node with CADENCE SPECTRE. Table 4 evaluate the effects of supply voltage as well as temperature fluctuation on power use, delay, and PDP. Table 5 illustrate the impact of temperature fluctuations on the power consumption of an Arithmetic Logic Unit (ALU). Power usage in FinFET technology increases linearly with temperature. Elevated temperatures result in an increase in the flow of electric current due to the presence of minority carriers and their level of concentration. As a result, there is a direct correlation between temperature and power consumption, meaning that power demand increases in tandem with rising temperatures. However, the ALU made from Carbon Nanotubes (CNTs) maintains a consistent power consumption because of the very low resistivity in the CNT channel, reduced parasitic capacitance, and lower current leakage in CNT-based architectures. The power consumption of the proposed CNTFET 4-bit ALU is atleast 32% lower than that of the existing 4-bit CMOS logic based ALUs. The delay period of the CNTFET4-bit proposed ALU has been reduced by 50% compared to the existing ALUs.

5. Conclusion

This study suggests a suitable design for an Arithmetic Logic Unit (ALU) that incorporates both CNTFET and FinFET technologies. A comparison study compared the obstacles and efficiency of employing CNTFET technology in developing nano-electronic circuits to FinFET circuits. The results show that a proposed delay-controllable reconfiguration ALU designed with Carbon Nanotubes (CNT) beat its counterparts in terms of power usage latency and Power-Delay Product (PDP). The power utilization of the proposed CNTFET 4-bit ALU is at least 32% lower than that of existing 4-bit ALUs. The suggested CNTFET 4-bit ALU has a 50% lower delay time than current ALUs. This increase is seen over a wide range of supply voltages, from 0.8V to 1V. Throughout the temperature range ranging from -25°C to 50°C, the CNTFET adder has lower power utilization and delay than the FinFET version, which contains the ALU, as demonstrated. The facts presented above suggest that CNTFET is growing as a viable replacement for FinFET in the progress of nanoelectronic components.

Conflicts of Interest

This section is compulsory. A competing interest exists when a secondary interest, such as financial gain, influences professional judgment concerning research validity. We require that our authors reveal any possible conflict of interest in their submitted manuscripts. If there is no conflict of interest, authors should state that The author(s) declare(s) that there is no conflict of interest regarding the publication of this paper.

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References

[1] Saeid Seyedi, and Nima Jafari Navimipour, "Designing A New 4: 2 Compressor Using an Efficient Multi-Layer Full-Adder Based on Nanoscale Quantum-Dot Cellular Automata," *International Journal of Theoretical Physics*, vol. 60, no. 7, pp. 2613-2626, 2021. [CrossRef] [Google Scholar] [Publisher Link]

[2] Takamoto Watanabe, "All-Digital VCO-ADC TAD Using 4CKES-Type in 16-nm FinFET CMOS for Technology Scaling with Stochastic-ADC Method," *2021 28th IEEE International Conference on Electronics, Circuits, and Systems (ICECS)*, pp. 1-4, Dubai, United Arab Emirates, 2021. [CrossRef] [Google Scholar] [Publisher Link]

[3] P. Saritha et al., "4- Bit Vedic Multiplier with 18nm FinFET Technology," *2020 International Conference on Electronics and Sustainable Communication Systems (ICESC)*, Coimbatore, India, pp. 1079-1084, 2020. [CrossRef] [Google Scholar] [Publisher Link]

[4] A. A. Sujata, and D. Lalitha, "Survey on Latest FinFET Technology and its Challenges in Digital Circuits and IC's," *International Journal of Electronics Engineering*, vol. 10, no. 2, pp. 577-585, 2018. [Google Scholar] [Publisher Link]

[5] Ayushi, and Er. Kailash Chandra, "Low Power and High Speed Mutliplier Deisgns using FinFET Technology," *International Journal of Advanced Research in Computer and Communication Engineering*, vol. 7, no. 2, pp. 143-146, 2018. [Publisher Link]

[6] Masoomeh Tirgar Fakheri, Keivan Navi, and Mohammad Tehrani, "A Novel Device to Implement Full Set of Three - Input Logic Gates Using a Naphthalene-Based Single-Molecule Field - Effect Transistor," *IEEE Transactions on Electron Devices*, vol. 68, no. 2, pp. 733-738, 2021. [CrossRef] [Google Scholar] [Publisher Link]

[7] Nandhaiahgari Dinesh Kumar, Rajendra Prasad Somineni, and CH. Raja Kumari, "Design and Analysis of Different Full Adder Cells Using New Technologies," *International Journal of Reconfigurable and Embedded Systems*, vol. 9, no. 2, 2020. [CrossRef] [Google Scholar] [Publisher Link]

[8] Wei-Xiang You, Pin Su, and Chenming Hu, "Evaluation of NC-FinFET Based Subsystem - Level Logic Circuits," *IEEE Transactions on Electron Devices*, vol. 66, no. 4, pp. 2004-2009, 2019. [CrossRef] [Google Scholar] [Publisher Link]

[9] Sina Bakhtavari Mamaghani, Mohammad Hossein Moaiyeri, and Ghassem Jaberipur, "Design of an Efficient Fully Nonvolatile and Radiation-Hardened Majoritybased Magnetic Full Adder Using FinFET/MTJ," *Microelectronics Journal*, vol. 103, 2020. [CrossRef] [Google Scholar] [Publisher Link]

[10] Mahdieh Nayeri, Peiman Keshavarzian, and Maryam Nayeri, "High-Speed Penternary Inverter Gate Using GNRFET," *Journal of Advances in Computer Research*, vol. 10, no. 2, pp. 53-59, 2019. [Google Scholar] [Publisher Link]

[11] Masoud Mahjoubi et al., "Two Efficient Ternary Adder Designs Basedon CNFET Technology," *Journal of computer and knowledge Engineering*, vol. 4, no. 1, pp. 25-34, 2021. [CrossRef] [Google Scholar] [Publisher Link]

[12] M. Aalelai Vendhan, and S. Deepa, "Investigations on Performancemetrics of FINFET Based 8 - bit Low Power Adder Architectures Implemented Using Various Logic Styles," *Indian Journal of Science and Technology*, vol. 11, no. 24, pp. 1-22, 2018. [CrossRef] [Google Scholar] [Publisher Link]

[13] Anju Rajput et al., "Novel CMOS and PTL Based Half Subtractor Designs," *2021 IEEE International Symposium on Smart Electronic Systems (iSES)*, Jaipur, India, pp. 165-168, 2021. [CrossRef] [Google Scholar] [Publisher Link]

[14] Farzin Mahboob Sardroudi, Mehdi Habibi, and Mohammad Hossein Moaiyeri, "CNFET-Based Design of Efficient Ternary Half Adder and 1-Trit Multi-Plier Circuits Using Dynamic Logic," *Microelectronics Journal*, vol. 113, 2021. [CrossRef] [Google Scholar] [Publisher Link]

[15] Yogesh Shrivastava, and Tarun Kumar Gupta, "Designing of Low-Powerhigh - Speed Noise Immune CNTFET 1-Trit Unbalanced Ternary Subtractor," *Journal of Circuits, Systems and Computers*, vol. 31, no. 5, 2022. [CrossRef] [Google Scholar] [Publisher Link]

[16] Trapti Sharma, and Laxmi Kumre, "CNTFET - Based Design of Ternary Arithmetic Modules," *Circuits, Systems, and Signal Processing*, vol. 38, no. 10, pp. 4640-4666, 2019. [CrossRef] [Google Scholar] [Publisher Link]

[17] E. Ramkumar et al., "Design and Analysis of Low Power and Highspeed FinFET Based Hybrid Full Adder/Subtractor Circuit(FHAS)," *2020 IEEE International Symposium on SmartElectronic Systems (iSES)(Formerly iNiS)*, Chennai, India, pp. 281-284, 2020. [CrossRef] [Google Scholar] [Publisher Link]

[18] Pegah Zakian, and Rahebeh Niaraki Asli, "An Efficient Design of Low-Power and High-Speed Approximate Compressor in FinFET Technology," *Computers & Electrical Engineering*, vol. 86, 2020. [CrossRef] [Google Scholar] [Publisher Link]

[19] Farnaz Sabetzadeh, Mohammad Hossein Moaiyeri, and Mohammad Ahmadinejad, "A Majority-Based Imprecise Multiplier for Ultra-Efficient Approximate Image Multiplication," *IEEE Transactions on Circuitsand Systems I: Regular Papers*, vol. 66, no. 11, pp. 4200-4208, 2019. [CrossRef] [Google Scholar] [Publisher Link]

[20] V. M. Senthil Kumar, and S. Ravindrakumar, "Design of an Area-Efficient Finfet-Based Approximate Multiplier in 32-nm Technology for Low-Power Application," *Soft Computing and Signal Processing*, pp. 505-513, Singapore, 2019. [CrossRef] [Google Scholar] [Publisher Link]

[21] Rashmit Patel, Yash Agrawal, and Rutu Parekh, "A Novel Slice-Based High-Performance ALU Design Using Prospective Single Electrontransistor," *IETE Journal of Research*, vol. 68, no. 2, pp. 1115-1124, 2022. [CrossRef] [Google Scholar] [Publisher Link]

[22] N. Shylashree et al., "Design and Analysis of High-Speed 8-bit ALU Using18 nm FinFET Technology," *Microsystem Technologies*, vol. 25, no. 6, pp. 2349-2359, 2019. [CrossRef] [Google Scholar] [Publisher Link]

[23] Jency Rubia J, and Babitha Lincy R, "Design of Low Power 4 Bit ALU Using 32 nm FinFET Technology," *International Journal of Pure andApplied Mathematics*, vol. 120, no. 6, pp. 8089-8100, 2018. [Publisher Link]

[24] Sudha Vani Yamani, N. Usha Rani, and Ramesh Vaddi, "Design and Performance Benchmarking of Hybrid Tunnel FET/STT-MTJ-Based Logic In-Memory Designs for Energy Efficiency," *IEEE Transactions on Magnetics*, vol. 58, no. 4, pp. 1-11, 2022. [CrossRef] [Google Scholar] [Publisher Link]

[25] Talha F. Canan et al., "Fine-Grain Reconfigurable Logic Circuits for Adaptive and Secure Computing Via Work-Function Engineered Schottky Barrier FinFETs," *IEEE Journal on Exploratory Solid-State Computational Devices and Circuits*, vol. 7, no. 2, pp. 150-158, 2021. [CrossRef] [Google Scholar] [Publisher Link]