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Original Article

A Novel Approach to Fault Recognition in Multi-level Inverters through Artificial Neural Networks

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Abstract *- This paper presents a novel methodology for detecting open and short circuit faults in multi-level inverters using a combination of time-frequency analysis, simulation, and experimental investigations. The proposed approach integrates the Discrete Wavelet Transform (DWT), Artificial Neural Networks (ANNs), and the back-propagation training technique to achieve accurate fault recognition. The utilization of DWT enables the extraction of fault-related features from the time-frequency domain, enhancing fault detection capabilities. These features are then utilized as inputs to an ANN, trained using the Back Propagation Training technique, to classify different fault conditions. Moreover, a LabVIEW real-time fault diagnosis model is developed to validate the effectiveness of the proposed approach through experimental implementation. This model provides a practical framework for real-time fault detection and diagnosis in multi-level inverters, contributing to improved reliability and operational efficiency of power electronics systems. By combining advanced signal processing techniques with artificial intelligence, the proposed methodology offers a comprehensive solution for fault recognition in multi-level inverters, addressing the challenges of modern power systems. The experimental validation underscores the effectiveness and feasibility of the proposed approach in real-world applications, highlighting its potential for enhancing the reliability and performance of multi-level inverter-based power systems.*

Keywords *- Artificial Neural Networks, Back propagation training, Discrete Wavelet Transform, Fault detection, Multi-level inverters.*

1. Introduction

Multi-level Inverters have emerged as key components in modern power electronics systems due to their ability to generate high-quality output waveforms with reduced harmonic distortion, lower switching losses, and enhanced efficiency compared to conventional two-level inverters. However, like any complex electrical system, multi-level inverters are prone to faults that can compromise their performance, reliability, and safety.

Faults in multi-level inverters can manifest in various forms, including open-circuit faults, short-circuit faults, device failures, and voltage unbalances. These faults can occur due to factors such as aging of components, thermal stress, manufacturing defects, environmental conditions, and operational anomalies. Detecting and diagnosing these faults accurately and promptly is crucial for preventing system failures, minimizing downtime, and ensuring the safety of personnel and equipment. Fault analysis in multi-level inverters involves the identification, localization, and characterization of abnormal conditions or deviations from normal operation.

Traditional fault analysis techniques often rely on mathematical models, circuit simulations, and analytical methods to predict fault behaviour and assess the impact on system performance. However, these approaches may have limitations in capturing the complexity of fault dynamics and real-time operational conditions. In recent years, there has been growing interest in employing advanced computational

intelligence techniques such as ANNs, fuzzy logic, genetic algorithms, and machine learning algorithms for fault analysis in multi-level inverters. These techniques offer the advantage of learning from data, adaptability to changing operating conditions, and robustness against noise and uncertainties. By leveraging these intelligent techniques, researchers aim to develop more accurate, efficient, and reliable fault detection and diagnosis systems for multi-level inverters [1-3].

Open circuit faults occur when there is an interruption in the current path, leading to an open circuit condition in one or more semiconductor devices (such as Insulated Gate Bipolar Transistors - IGBTs or Metal-Oxide-Semiconductor Field-Effect Transistors - MOSFETs) or passive components (such as capacitors or resistors) within the multi-level inverter circuit.

Open circuit faults can result from factors such as device aging, thermal stress, manufacturing defects, or external disturbances. When an open circuit fault occurs, the affected phase or voltage level may experience a voltage drop or complete loss of output, leading to waveform distortion, reduced system efficiency, and potential damage to other components if not promptly detected and mitigated. Short circuit faults occur when there is an unintended connection or low impedance path between different points in the multi-level inverter circuit, leading to excessive current flow.

Short circuits can occur between power semiconductor devices, between phases, or between phases and ground. These faults can result from insulation breakdown, device failure, conductor damage, or external factors such as environmental conditions or mechanical stress. Short circuit faults pose serious safety hazards, as they can lead to overcurrent conditions, excessive heating, component damage, and even catastrophic failures if not promptly addressed. Detecting and mitigating open circuit and short circuit faults in multi-level inverters is crucial for ensuring system reliability and safety.

Various techniques are employed for fault detection and diagnosis, including model-based methods, signal processing techniques, and intelligent algorithms such as ANNs and fuzzy logic. By continuously monitoring system parameters such as voltages, currents, and temperatures and employing advanced fault detection algorithms, it is possible to detect and mitigate open circuit and short circuit faults in multi-level inverters effectively, thereby enhancing system resilience and performance [4-7].

Diode-clamped multi-level inverters, also known as Neutral-Point Clamped (NPC) inverters, are one of the earliest types of multi-level inverters. They utilize clamping diodes to establish multiple voltage levels between the DC input and output terminals. By connecting several voltage sources in series, each with its clamping diode network, diode-clamped inverters can synthesize stepped output waveforms with reduced harmonic content. However, their main drawback is the limited number of voltage levels, which affects their output waveform quality and efficiency.

Capacitor-clamped multi-level inverters, also known as flying capacitor inverters, employ capacitor voltage balancing techniques to achieve multiple voltage levels. These inverters are capable of offering stepped output voltages with better waveform accuracy by constantly altering the voltages across flying capacitors linked to the DC input and output terminals. Capacitor-clamped inverters have higher voltage resolution than diode-clamped inverters and are ideal for medium-voltage applications. However, they required complex algorithms for controlling capacitor voltage balancing, which increases system complexity and cost [8, 9].

Cascaded H-bridge multi-level inverters are made up of numerous H-bridge modules connected in series, each capable of producing different voltage levels. Cascaded H-bridge inverters can generate highly precise output waveforms with minimum harmonic distortion by separately managing each H-bridge module's switching states. These inverters are scalable and modular, allowing for a simple extension to suit higher voltage levels [10].

Hybrid multi-level inverters combine features of different multi-level inverter topologies to achieve enhanced performance and flexibility. These inverters may integrate diode-clamped, capacitor-clamped, or cascaded H-bridge modules to exploit the advantages of each topology while mitigating their drawbacks. Hybrid multi-level inverters offer improved voltage resolution, reduced switching losses, and enhanced reliability compared to single-topology inverters [11].

1.1. Literature Review

Multi-level inverters, like any other complex electronic system, are prone to malfunctions that can disrupt operations and jeopardize system reliability. As a result, failure diagnosis and fault tolerance procedures are crucial for ensuring that multi-level inverters operate continuously and reliably in critical applications [12].

Artificial Neural Networks (ANN) and machine learning approaches have emerged as effective tools for fault detection and tolerance in multi-level inverters. These methods take advantage of neural networks' innate capacity to learn complicated patterns from data and create correct predictions, resulting in effective defect detection, classification, and mitigation [13].

However, one of the most difficult aspects of fault identification in multi-level inverters is the complexity of failure patterns and their manifestations in the system. Multi-level inverters are made up of several power electronic

components that operate at different voltage levels, making it difficult to distinguish fault signals from normal performance without advanced diagnostic procedures. Furthermore, faults have the potential to display nonlinear behaviours and interactions, which complicates the detection process. To successfully identify fault signals and separate them from normal operation, complex signal processing algorithms and feature extraction techniques are required.

Switch faults in multi-level inverters can result from factors such as device aging, thermal stress, manufacturing defects, and external disturbances. These faults can manifest as open circuit or short circuit conditions in the power semiconductor switches, leading to voltage imbalance, harmonic distortion, and potential system instability. Detecting switch faults promptly and accurately is crucial for maintaining the reliability and safety of multi-level inverter systems.

Switch faults can lead to voltage imbalances among the different voltage levels generated by the multi-level inverter, resulting in distorted output waveforms and reduced system efficiency. Switch faults can introduce higher harmonic components in the output voltage, leading to increased Total Harmonic Distortion (THD) and potentially causing interference with other electrical equipment connected to the system.

Severe switch faults may result in system instability, leading to voltage fluctuations, current surges, and potential damage to connected loads or other components within the power distribution network. Switch faults can pose safety hazards to personnel and equipment, especially in high-power applications where the failure of a single switch can result in catastrophic consequences such as electrical fires, equipment damage, or personnel injury. Addressing switch faults in multi-level inverters requires effective fault detection, diagnosis, and mitigation strategies to minimize their impact and ensure the continued operation of the system with optimal performance and reliability [14, 15].

Switch reliability is paramount in CHB multi-level inverters, as these switches are responsible for controlling the flow of current and voltage in the system. Any malfunction or failure of the switches can lead to voltage imbalances, harmonic distortion, and potentially catastrophic system failures. Characterizing switch failure modes in CHB inverters presents several challenges, including the complex nature of switch operation, the dynamic operating conditions of the inverter, and the interaction between multiple switches within each H-Bridge cell.

Additionally, switch failures may exhibit transient behaviour or intermittent faults, making them difficult to detect and diagnose. Fault detection is essential for ensuring the reliable and safe operation of multi-level inverters. Open circuit faults, if left undetected, can lead to voltage imbalances, increased harmonic distortion, and potential damage to other system components. Prompt detection of these faults allows for timely mitigation actions to be taken, minimizing downtime and preventing further damage.

Open circuit faults occur when there is an interruption in the current path within the inverter circuit, leading to voltage imbalances and distorted output waveforms. Traditional fault detection methods may not be sufficient to detect open circuit faults due to their complex and dynamic nature.

By leveraging advanced signal processing techniques, machine learning algorithms, and data-driven approaches, this research aims to develop effective fault detection algorithms capable of identifying open circuit faults in multi-level inverters. The proposed algorithms will enhance system reliability by enabling timely intervention and preventive maintenance actions, thereby minimizing downtime and ensuring the continued operation of multi-level inverter-based power systems [16-19].

However, their reliability can be compromised by switch faults, which may occur due to aging, thermal stress, or manufacturing defects. Assessing the performance degradation of multi-level inverter systems under various switch fault scenarios is crucial for ensuring system reliability and maintaining optimal operation. Switch faults in multi-level inverters can lead to several performance degradation issues, including increased harmonic distortion, voltage imbalance, and reduced efficiency. The severity of these degradation effects depends on factors such as fault type, fault location, and fault duration.

In assessing performance degradation, it is essential to consider the impact on key system parameters, such as total harmonic distortion, output voltage ripple, and system efficiency. Simulation studies and experimental investigations can provide valuable insights into how different switch fault scenarios affect these parameters under various operating conditions. Furthermore, fault-tolerant control strategies and mitigation techniques can be developed and evaluated to minimize the impact of switch faults on system performance. These strategies may include reconfiguration of the inverter topology, fault detection and isolation algorithms, and adaptive control schemes.

This knowledge can inform the development of robust fault detection, diagnosis, and mitigation strategies, ultimately enhancing the reliability and resilience of multi-level inverter-based power systems in diverse applications. Grid-connected multi-level inverter systems play a vital role in modern power distribution networks, enabling the integration of renewable energy sources, voltage regulation, and power quality improvement. However, switch failures within these systems can have significant implications for grid stability and power

quality. Investigating the impact of switch failures on these critical aspects is essential for ensuring the reliability and performance of grid-connected multi-level inverter systems [20-23].

Switch failures in multi-level inverters can result in voltage fluctuations, harmonic distortion, and imbalance in grid-connected currents, potentially leading to instability in the power grid. The consequences of switch failures may include increased power losses, reduced system efficiency, and compromised power delivery to consumers. By systematically investigating the impact of switch failures on grid stability and power quality, researchers can assess the vulnerability of grid-connected multi-level inverter systems to different fault scenarios.

Simulation studies and experimental evaluations can help quantify the extent of voltage and current distortions, assess transient responses, and identify potential grid instability issues resulting from switch failures. Furthermore, advanced control strategies and fault management techniques can be developed to mitigate the impact of switch failures on grid stability and power quality.

These strategies may include fault detection and isolation algorithms, real-time monitoring systems, and adaptive control schemes to ensure seamless operation and minimize disruptions to the power grid. Understanding the complex interplay between switch failures, grid stability, and power quality is essential for designing robust and resilient grid-connected multi-level inverter systems. By addressing these challenges, researchers and engineers can contribute to the development of more reliable and efficient power distribution networks, facilitating the widespread adoption of renewable energy sources and enhancing overall grid resilience in the face of evolving energy demands and environmental concerns [24-26].

The following objectives have been formulated to identify faulty switches in multi-level inverters effectively:

- Develop a novel methodology integrating time-frequency analysis, DWT, ANNs, and Back Propagation to detect open and short circuit faults in multi-level inverters accurately.
- Extract fault-related features from the time-frequency domain using DWT to enhance fault detection capabilities.
- Train ANNs using Back Propagation to classify different fault conditions based on extracted features.
- Validate the proposed approach through experimental implementation using a LabVIEW real-time fault diagnosis model.
- Contribute to improved reliability and operational efficiency of multi-level inverter-based power systems by combining advanced signal processing techniques with artificial intelligence for fault recognition.

2. Proposed Fault Recognition System for Multi-Level Inverter

At the hardware level, a DC power supply is used when combined with a five-level multi-level cascaded inverter and an NI USB interface, all of which have been integrated with an induction motor. At the software level, LabVIEW is used to implement the provided fault recognition system, which is illustrated in Figure 1. The system operates by employing LabVIEW for various tasks. Firstly, LabVIEW is used for performing DWT analysis, facilitating feature extraction from the system's operation. These extracted features are then employed as inputs for an ANN trained with fault patterns. Subsequently, LabVIEW's Graphical User Interface (GUI) is leveraged for fault diagnosis. Through the GUI, the system identifies faulty switches within the multi-level inverter. This fault diagnosis is conducted based on the patterns recognized by the ANN, enabling accurate identification of faulty components.

2.1. Fault Analysis of Five-Level Inverter

Figure 2 illustrates the structure of a cascaded five-level inverter comprising two bridges, denoted as Bridge A and Bridge B. Each bridge consists of four power switches. The inverter operates based on Sinusoidal Pulse Width Modulation (SPWM) techniques to generate a five-level output voltage waveform. SPWM involves modulating the width of the pulses in a sinusoidal manner to approximate the desired output waveform. By combining the outputs of both bridges, the cascaded five-level inverter achieves a higher number of voltage levels, allowing for improved output waveform quality and reduced harmonic distortion compared to traditional two-level inverters.

2.2. Open Circuit Fault Analysis

Figure 3 depicts the open circuit analysis of a five-level inverter, focusing on the scenario where the S1A switch experiences an Open Circuit (OC) fault. The magnified voltage waveforms illustrate the normal operating condition alongside the faulty condition resulting from the switch fault. During normal operation, the voltage waveform exhibits expected characteristics. However, upon the occurrence of the S1A switch fault, noticeable deviations in the voltage waveform are observed, indicating the fault. Additionally, the inference of changes in current during the system's starting phase and subsequent operation after the fault occurrence are discussed, providing insights into the dynamic behaviour of the inverter under fault conditions.

2.3. Short Circuit Fault Analysis

Figure 4 illustrates the short circuit analysis of a five-level inverter, specifically focusing on the scenario where the S1A switch experiences a short circuit fault. The magnified view contrasts the normal current waveform with the significantly increased current value observed during the Short Circuit (SC) fault, surpassing the normal current level by more than tenfold.

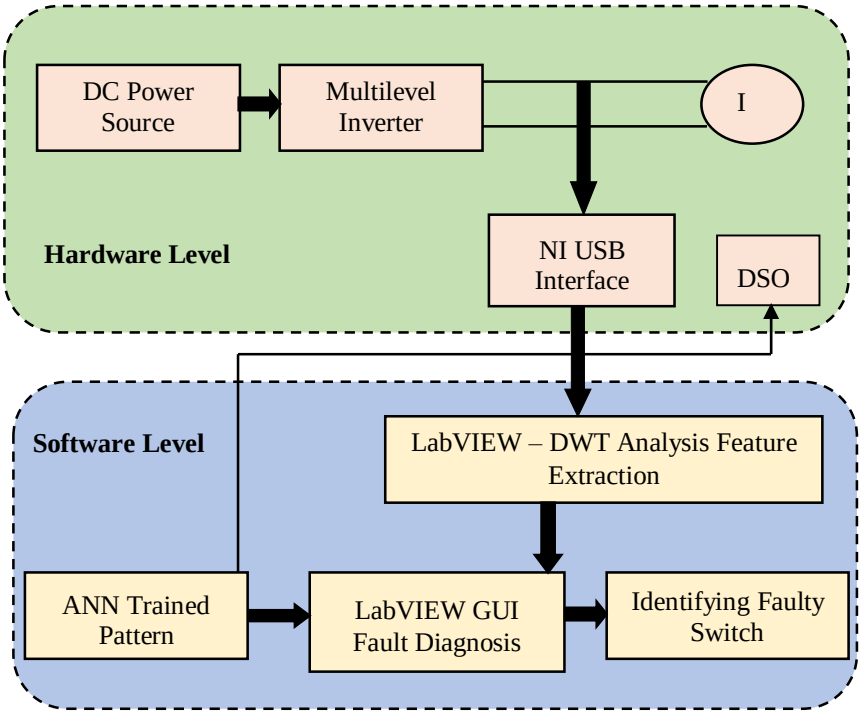


Fig. 1 Fault recognition for multi-level inverter

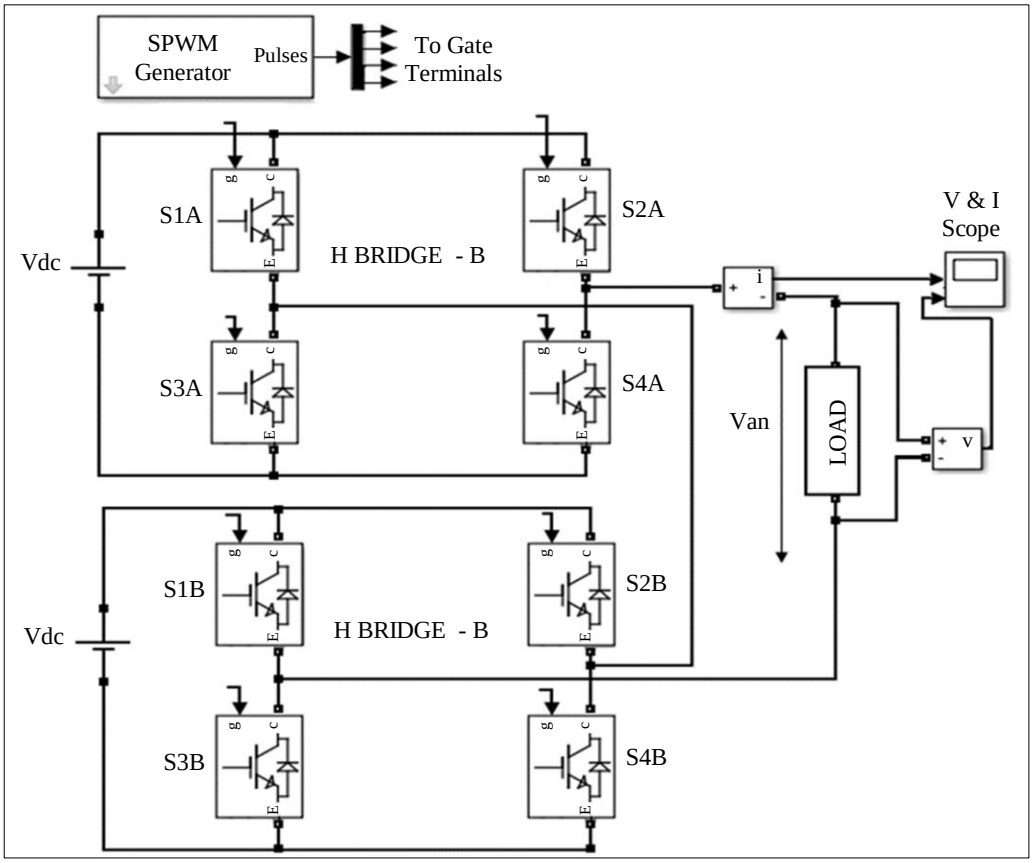


Fig. 2 Structure of cascaded five-level inverter

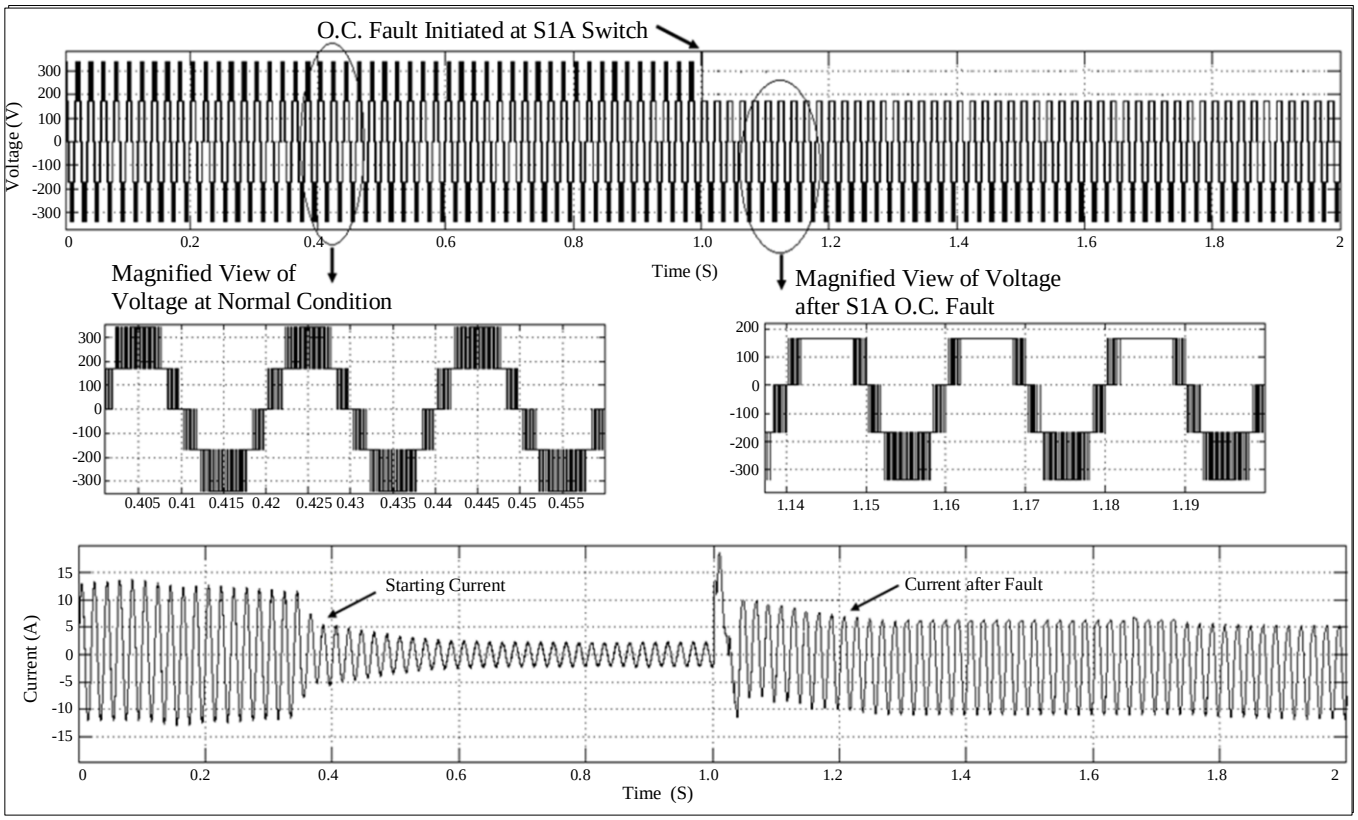


Fig. 3 Open circuit analysis of five five-level inverter

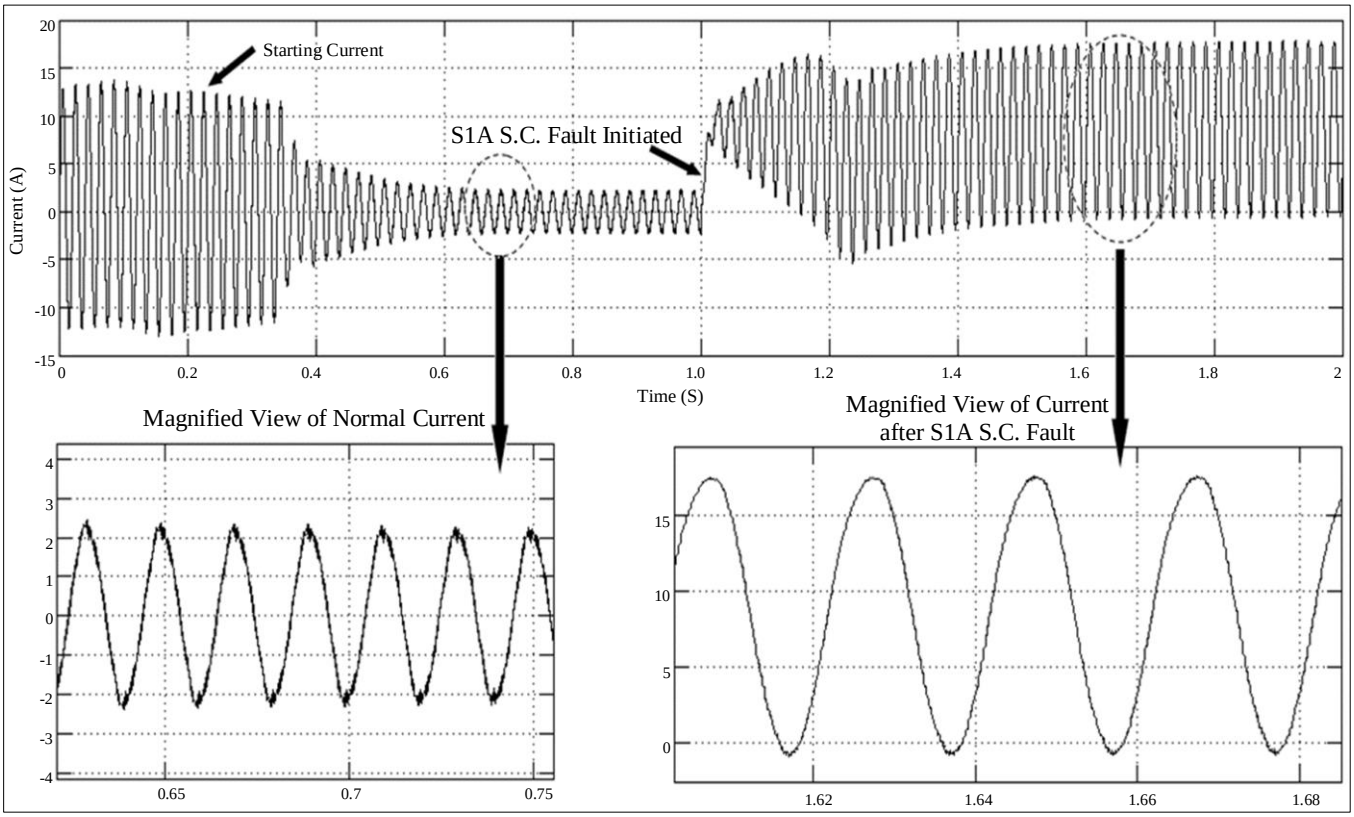


Fig. 4 Short circuit analysis of five five-level inverter

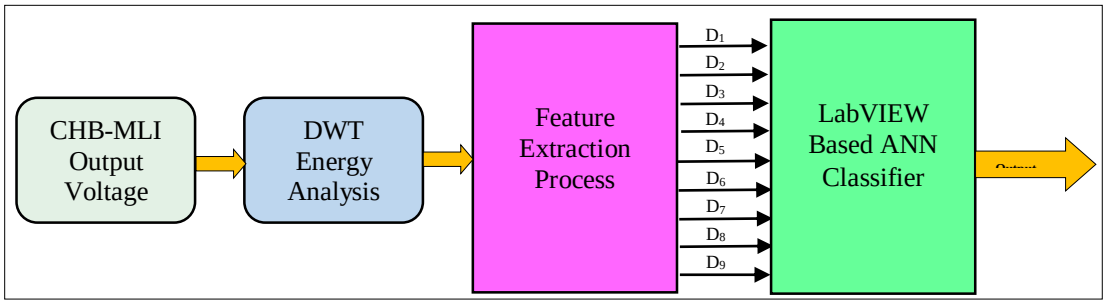


Fig. 5 Extraction of voltage signal using DWT

3. Signal Processing with DWT

In Figure 5, the process of extracting voltage signals using DWT from a CHB-MLI is depicted. The DWT energy analysis is conducted to assess the characteristics of the voltage signal. This analysis allows for the identification of relevant features extracted from D1 to D9, which capture essential information regarding the fault conditions present in the system.

Subsequently, a LabVIEW-based ANN classifier is employed to analyse the extracted features and classify the fault conditions accurately. The ANN utilizes a back-propagation training technique to learn from the extracted features and identify patterns associated with various fault scenarios in the multi-level inverter.

Through the integration of DWT-based signal processing techniques and ANN-based pattern recognition algorithms, the proposed approach offers a robust and efficient method for fault diagnosis in multi-level inverter systems. By leveraging LabVIEW for implementation, the system provides a user-friendly interface for real-time monitoring and diagnosis, contributing to enhanced reliability and operational efficiency of power electronics systems.

The novel defect detection algorithms function by detecting important features in output voltage data, which are subsequently methodically extracted from the raw data to produce diagnostic information. Time and frequency characteristics of voltage signals must be analysed together for effective problem diagnosis. The method of extracting features from an output voltage signal using the DWT is shown in Figure 6.

The procedure describes the output of an equation involving differential variables, a(n), at multiple decomposition levels using DWT-based multi-resolution signal analysis of statistics. The initial data sequence is designated as b0[n] as the signal achieves convergence with quadrature mirror filters indexed by i and j.

It is separated at scale 1 into an informational component, also represented by the symbol b1[n], and an estimation component, b1[n]. At the following scale, the predicted vector b1[n] is further divided into b2[n] and c2[n], and so on. Equations (1) and (2) provide a mathematical quantification for this layered decomposition.

$$b_p[q] = \sum i[n-2q] b_{p-1}[n] \tag{1}$$

$$c_p[q] = \sum j[n-2q] b_{p-1}[n] \tag{2}$$

In Daubechies 4 wavelet decomposition, spanning from D1 to D9, Multi-Resolution Analysis (MRA) is employed to scrutinize signal characteristics. Standard deviation emerges as a pivotal metric, serving as a gauge for signal energy and power transitions within the decomposition process. As the signal undergoes successive levels of decomposition, its energy distribution across various frequency bands is analysed.

This facilitates the identification of significant features and patterns, aiding in fault diagnosis and signal interpretation. Through MRA, Daubechies 4 wavelet decomposition enables a comprehensive understanding of the signal's behaviour at different scales, offering insights crucial for effective analysis and decision-making in diverse applications, which is expressed in Equation (3).

$$STD = \sqrt{\frac{1}{S_n - 1} \sum_{j=1}^{S_n} [h_n(j) - R_n]^2} \tag{3}$$

In this case, S_n indicates the vector's temporal span and R_n its average value. The analysis of energy levels in discrete wavelet transform multi-resolution analysis signals is crucial for detecting and diagnosing potential failures in inverters, aiding in predictive maintenance strategies.

3.1. DWT - MRA Analysis

Figure 6 showcases an extensive portion of the DWT spanning from D1 to D9, facilitating MRA of informative signals. This analysis identifies significant components within the signals, enabling a comprehensive understanding of their characteristics across various decomposition levels. Table 1 illustrates the DWT - MRA decomposition analysis.

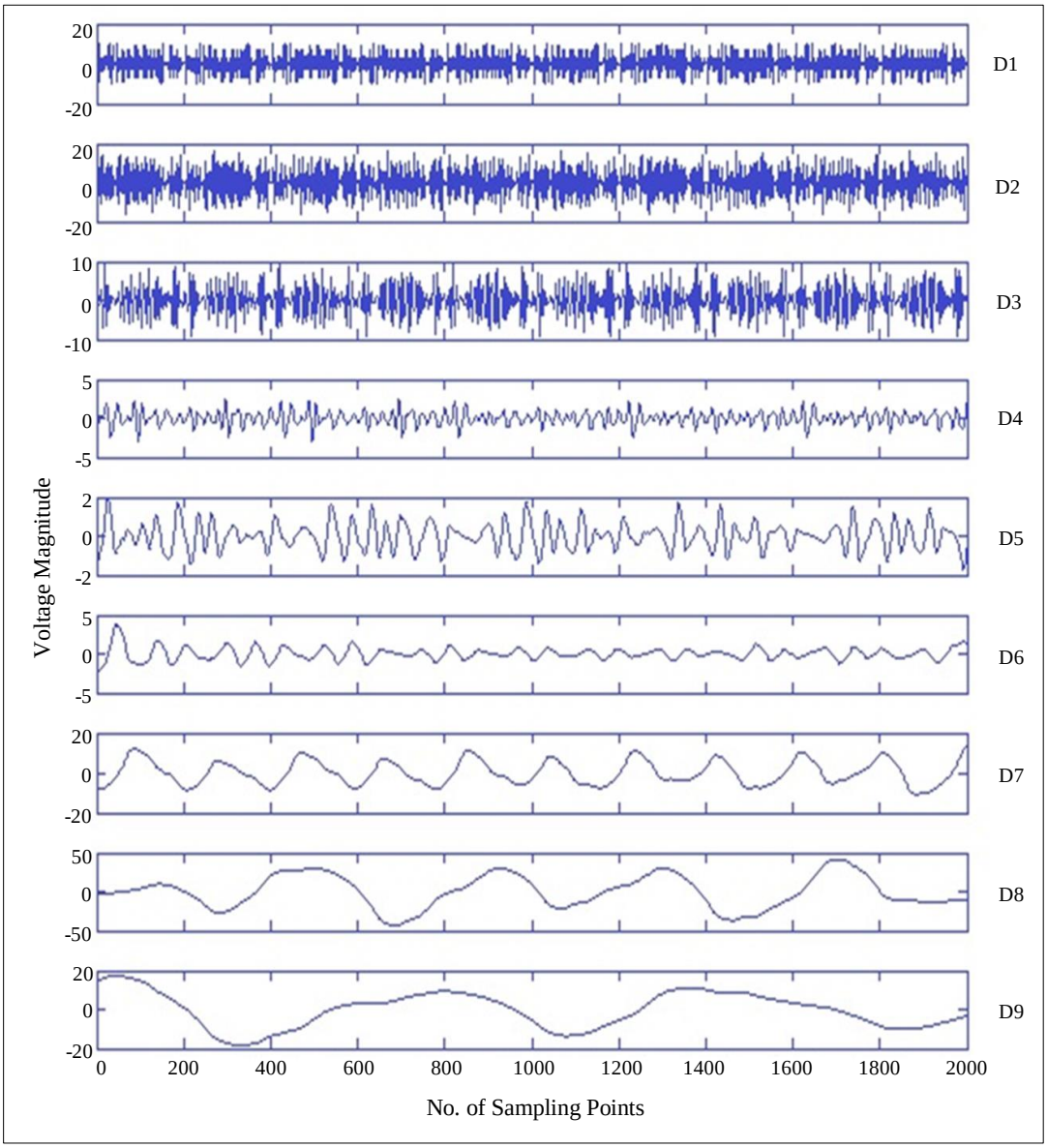


Fig. 6 DWT - MRA decomposition analysis

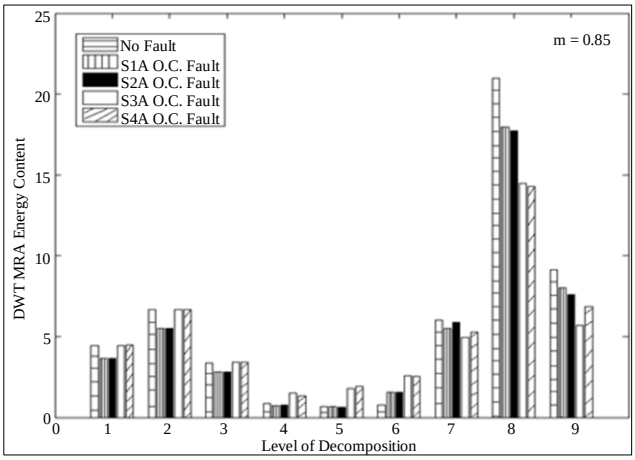


Fig. 7 Open circuit faults with different energy levels

Table 1. Operating frequency at various band levels

DWT Extraction Features	Operating Frequency (kHz)
D1	7-12
D2	2-7
D3	0.25-2
D4	0.01-0.25
D5	0.005-0.01
D6	0.00025-0.005
D7	0.00005-0.00025
D8	0.000025-0.00005
D9	0.0000075-0.000025

In Figure 7, open circuit faults are depicted with differing energy levels, ranging from the S1A switch to the S4A switch. Meanwhile, Figure 8 illustrates short circuit faults also exhibiting varying energy levels from the S1A switch to the S4A switch. These visual representations provide insights into the diverse magnitudes of faults occurring across different switches, aiding in the understanding of fault characteristics and their potential impact on the system's performance and reliability.

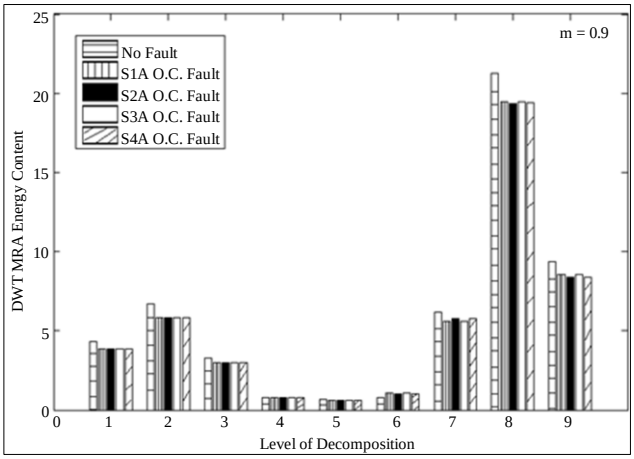


Fig. 8 Short circuit faults with different energy levels

4. Experimental Validation and ANN Analysis

4.1. Experimental Setup

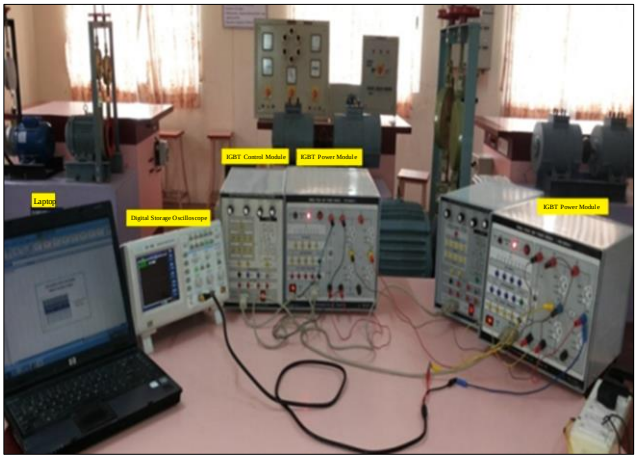
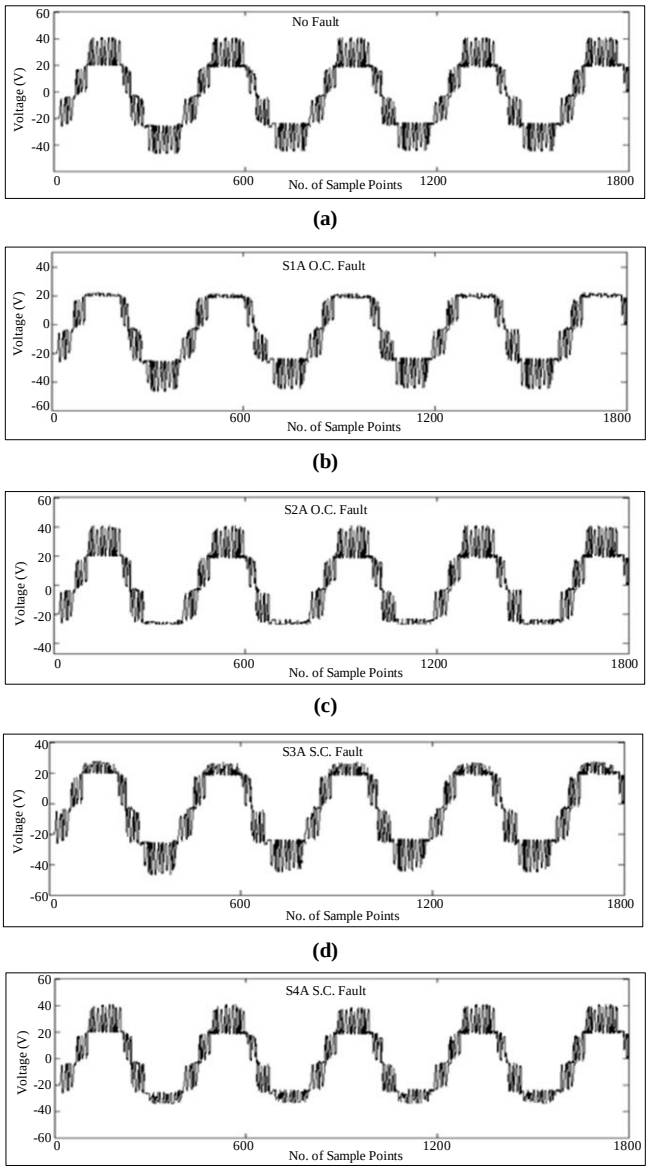


Fig. 9 Experimental setup of MLI with load

The experimental setup for five-level MLI includes a load, Insulated Gate Bipolar Transistor power module, firing circuit, Digital Storage Oscilloscope (DSO), and a laptop for MATLAB-ANN training. This configuration allows for comprehensive testing and optimization of MLI performance, facilitating research and development in a real-time fault recognition system. Figure 9 illustrates the real-time output signals of a five-level output voltage in different scenarios: (a) No fault, (b) S1A - Open Circuit (OC) fault, (c) S2A - OC fault, (d) S3A - Short Circuit (SC) fault, and (e) S4A - SC fault. These signals provide insights into fault detection and system response for comprehensive analysis and mitigation strategies.



(a) **(b)** **(c)** **(d)** **(e)**

Fig. 10 (a) Five-level output voltage - No fault, (b) S1A - OC fault, (c) S2A - OC fault, (d) S3A - SC fault, and (e) S4A - SC fault.

4.2. DWT Analysis Based on LabVIEW Approach

Figure 10 shows LabVIEW DWT analysis performed to the output voltage pattern of a five-level MLI with standard deviation used for fault diagnosis. The accompanying plot illustrates the standard deviation variations, aiding in fault identification and system monitoring. In Figures 11 and 12, LabVIEW employs DWT and ANN analysis to identify a faulty switch within the MLI system. The analysis provides a faulty switch meter indicating the severity of the fault.

It generates a detailed report for efficient troubleshooting and maintenance, enhancing the reliability and performance of the MLI system.

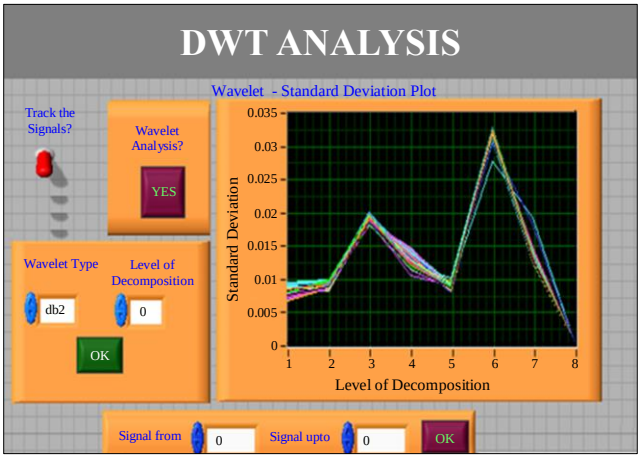


Fig. 11 LabVIEW DWT analysis based on the output voltage

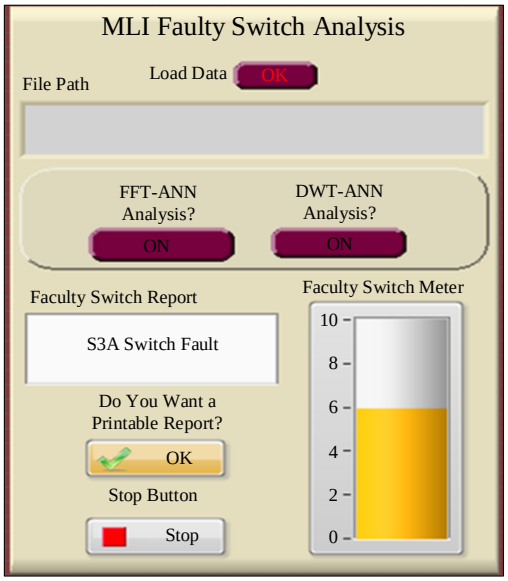


Fig. 12 LabVIEW DWT ANN analysis to identify a faulty switch

4.3. ANN Approach to Identify Faulty Switch

Figure 13 showcases a back-propagation feed-forward network used for various applications, including pattern recognition and function approximation. Table 2 outlines the specifications of this ANN. The neural network comprises nine input nodes, 18 nodes in the hidden layer, and nine nodes in the output layer.

It employs a learning rate (η) of 0.1 and undergoes 2500 iterations of training. During training, it utilizes 200 values, while 150 test input values are employed. The convergence criteria are defined as 0.01. Figure 14 illustrates the process of identifying the minimum MSE during the training phase of the ANN. This is a critical step in ensuring the network's accuracy and effectiveness in learning the desired patterns or relationships within the data. Figure 15 displays the MSE during the training process, indicating the disparity between the actual output and the desired output. The goal-based approach ensures that the network's performance steadily improves over epochs, ultimately reaching a predefined threshold. Monitoring MSE throughout epochs aids in assessing the network's convergence and determining if further training iterations are necessary for optimal performance.

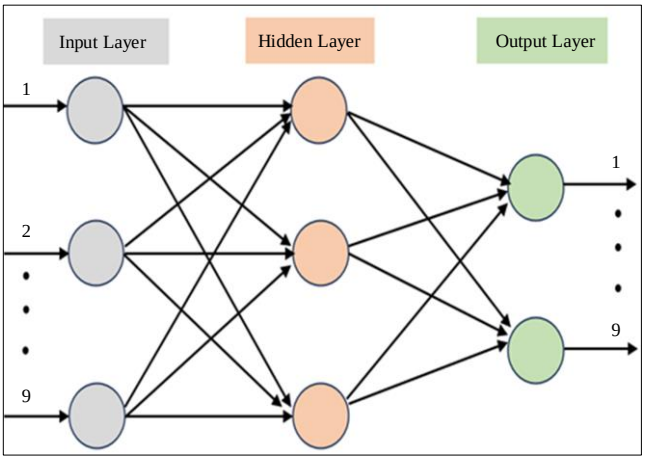


Fig. 13 Back propagation feed-forward network

Table 2. Major parameters of Artificial Neural Network

Parameters	Values
Number of input layer	9
Number of hidden layers	18
Number of the output layer	9
Value of learning rate (η)	0.1
Number of iterations	2500
Number of training patterns	200
The number of tested values considered	150
Overall convergence criteria	0.01

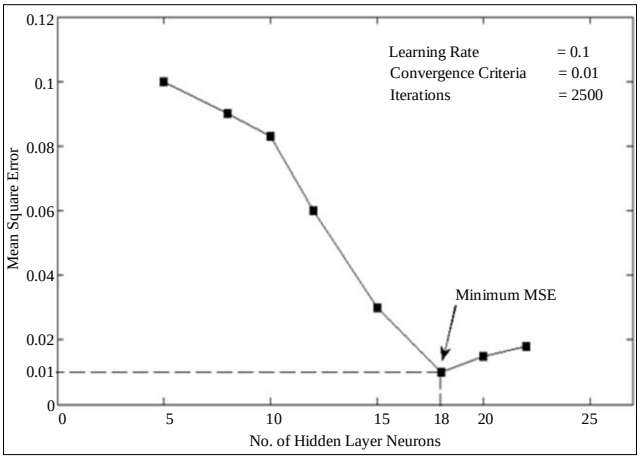


Fig. 14 Identification of a minimum mean square error

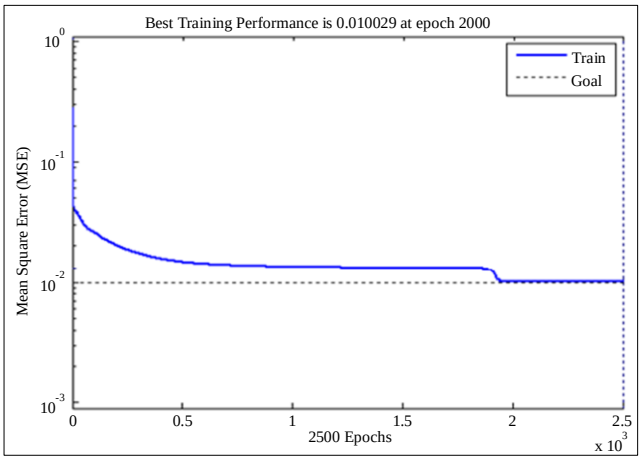


Fig. 15 Mean square error train and goal based on epochs

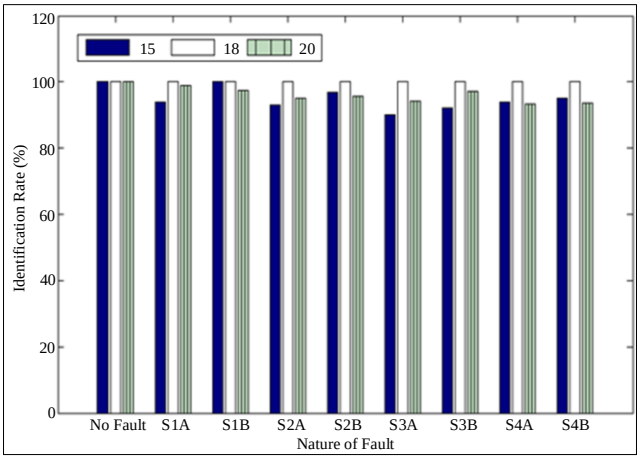
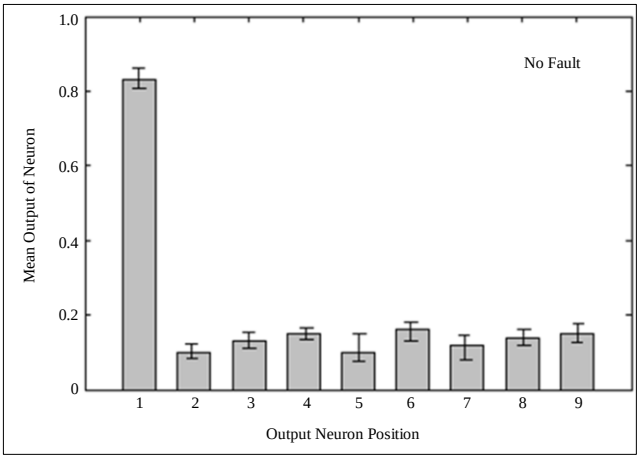
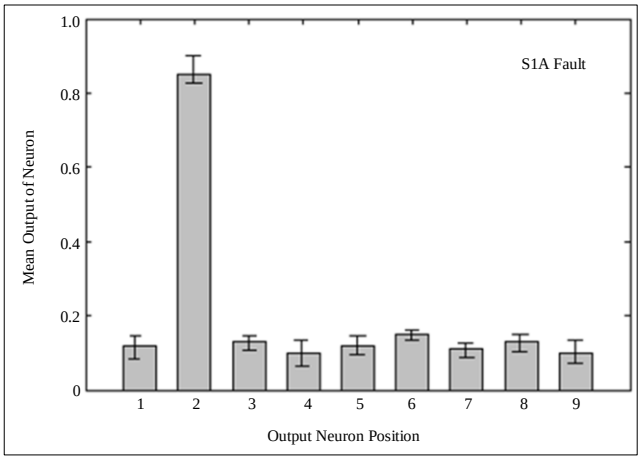


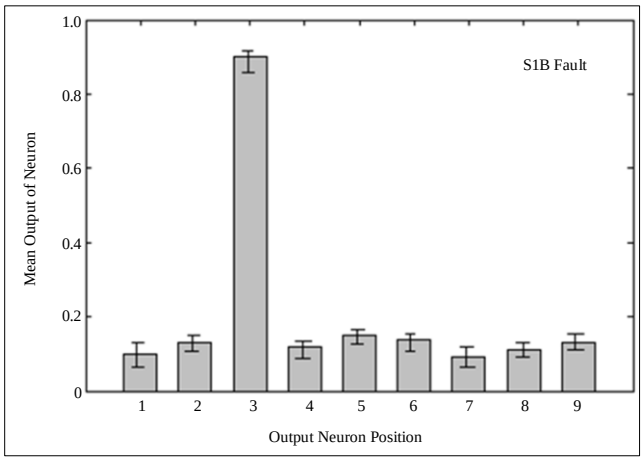
Fig. 16 Faulty switch identification based on the number of hidden layers



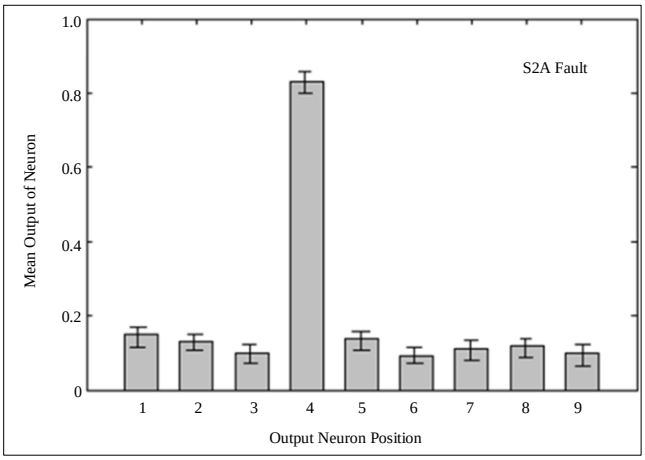
(a)



(b)



(c)



(d)

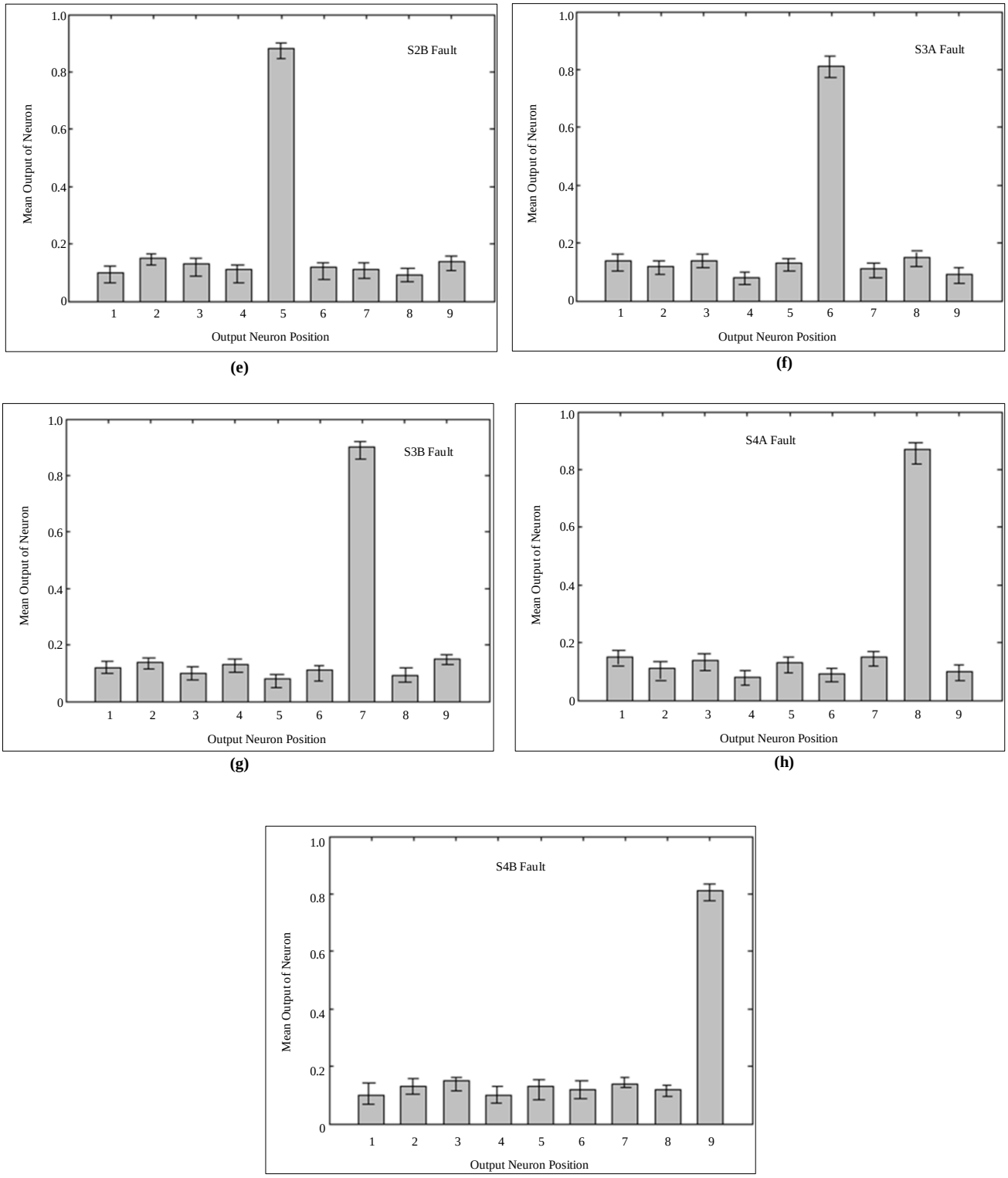


Fig. 17 (a) - (i) Identification of faulty switch based on a mean output of a neuron

Figure 16 illustrates the faulty switch identification based on a number of hidden layers. Figure 17 illustrates the identification of a faulty switch based on the mean output of neurons corresponding to various conditions: (a) to (i) represent the mean output under no fault, open circuit, and short circuit conditions, aiding in fault diagnosis.

5. Conclusion

The integration of Discrete Wavelet Transform, Artificial Neural Networks, and Back Propagation Training presents a robust methodology for detecting open and short circuit faults in multi-level inverters. By extracting fault-related features from the time-frequency domain using DWT and leveraging ANN classification trained with Back Propagation, accurate fault recognition is achieved. The developed LabVIEW real-time fault diagnosis model validates the effectiveness of the approach, offering a practical framework for real-time fault detection and diagnosis. This methodology holds promise for enhancing the reliability and operational efficiency of multi-level inverter-based power systems. Future research could explore extending this methodology to other types of faults, refining the fault classification accuracy, and integrating it into broader power system monitoring and control frameworks. Overall, this work contributes to advancing fault recognition in multi-level inverters, addressing crucial challenges in modern power systems.

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