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Original Article

Design and Investigation of Hetero Vertical TFET with Source Pocket for Work Function Engineering and Analog Performance Enhancement

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Abstract - *To provide a high-efficiency device, this article presents a Vertical SiGe Tunnel Field Effect Transistor (Hetero-VTFET), including and not including a source pocket. For perhaps the first time, a group IV miscible alloy SiGe is exploited in the source to improve carrier tunnelling through a source (SiGe)-channel (Si) Hetero-junction. To establish an optimal Hetero-VTFET design, work function engineering and hetero-junction structure tuning are used. The simulation results carried out using the TCAD Silvaco tool are used to analyze the behaviour of developed Hetero-VTFETs. The proposed optimal structure has a higher I_{ON}/I_{OFF} ratio ($>10^{14}$), a lesser subthreshold swing (<25 mV/Dec), and a high I_{ON} current in the 10^{-5}A/μm range.*

Keywords - *Vertical Tunnel Field Effect Transistor, Source pocket, Low supply voltage, Ambipolarity, Subthreshold slope.*

1. Introduction

Holistic scaling, which requires both device size and voltage to be reduced, has been proven to be a successful means of lowering power dissipation. However, this aggressive scaling of Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) with time leads to physical limits owing to various short channel effects. Scaling both size and voltages at the same time results in a scaled on-state current and a higher leakage current, which is unfavourable. As a result, decreasing both power dissipation and leakage current at the same time remains a complex problem [1]. In order to get a low off-state current, one of the most critical criteria is to reduce the device's Sub-threshold Swing (SS) at room temperature. A normal Field-Effect Transistor's (FET) SS, on the other hand, is restricted to 60mV/decade. The SS is a temperature-dependent variable because the current generation mechanism in a typical FET is dependent on thermionic emission.

To overcome these issues, researchers are looking for alternatives to MOSFETs that could be used in the near future. Because of their unique features, Tunnel Field-Effect Transistors (TFETs) are being viewed as a potential alternative for MOSFETs. TFETs look promising as they can operate at ultra-low supply voltages, while on the other, instead of thermionic emission, TFETs use Band-To-Band Tunnelling (BTBT) method to generate current [2-6]. The gate modulates the channel surface potential in TFETs to govern its control over BTBT tunnelling. BTBT reduces the temperature sensitivity of the SS, allowing the SS to be below 60 mV/decade in TFETs, and therefore, the leakage current in TFETs is lower than that in FETs.

Although TFETs have a low off-state current, they have a lower on-state driving current (I_{ON}) than FETs due to their poor BTBT efficiency [7, 8]. On the source side, using hetero-structure materials with a short bandgap is amongst the most often utilised strategies for I_{ON} enhancement. Using a lower bandgap material at the source side tunnelling junction lowers the tunnelling barrier, resulting in a lower threshold voltage (V_T) and better I_{ON} [9-13].

It is observed that source pocket-designed TFETs have improved subthreshold properties than regular TFETs [14, 15]. Materials having lower bandgaps like germanium and InAs are predominantly employed in the source region of a Si-TFET to form a hetero-junction, reducing the tunnelling width and increasing the drain current at the cost of a substantial increase in Ioff (10^{-12}A) significantly more than the maximum value attained in traditional Silicon based TFETs [16]. However, it has been demonstrated that staggered hetero-junctions at the source-channel interface based on III–V

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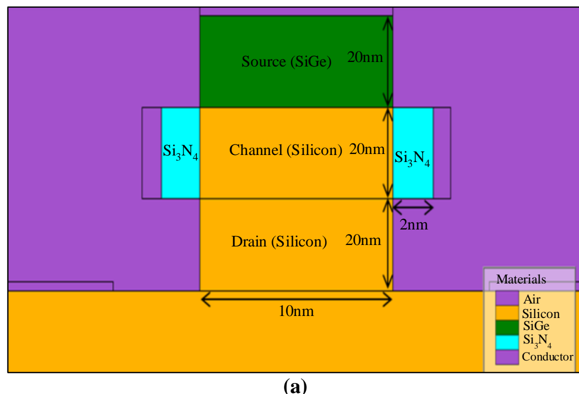
materials are ideal for low-voltage operation while balancing power consumption and performance [17]. In light of the preceding, this study presents a V-TFET based on SiGe/Si staggered hetero-junctions for low-power enactment. The widely accessible commercial platform SILVACO ATLAS TCAD simulation tool was utilized to examine the enactment of a SiGe/Si staggered hetero-junction vertical TFET, including and not including a source pocket. The suggested SiGe/Si V-TFET's hetero-junction fabrication feasibility is suggested in light of recent progress in the fabrication of SiGe on pure silicon substrates [18-20].

This work proposes a Hetero-VTFET [3, 21-23] device structure and presents a comprehensive analysis of how changes in the design parameters of a device affect the performance of the proposed structure. This article focuses on the critical device design parameters that are closely linked with Hetero-VTFET. The results obtained from rigorous simulations in TCAD have been the metrics of the proposed Hetero-VTFET design. The suggested structure is studied using device parameters and work function engineering to modulate the performance and drain current characteristics simultaneously. The study is assigned into three sections: the first portion provides an introduction, the second section contains device parameters and computations from simulation results, the third section discusses the findings, and the last section includes the conclusions.

2. Device Parameters and Simulation Results

Figures 1(a) and 1(b) show a cross-sectional view of the Hetero-VTFET device with and without a pocket. Silicon is used for the channel region, and Silicon Nitride (Si_3N_4) is used as a dielectric layer due to its high dielectric constant value. The TCAD simulation of the proposed vertical TFETs in the investigation included models like the Lombardi mobility model, Bandgap narrowing, Field-dependent mobility, Shockley-Read-Hall generation-recombination, Auger recombination model, and Fermi-Dirac statistics. To enhance drain current and fabrication compliance of the proposed vertical TFETs, a high-k Si_3N_4 material with a relative permittivity of 9.3 is employed as the gate oxide [3]. Table 1 lists the many parameters that were used in the simulation.



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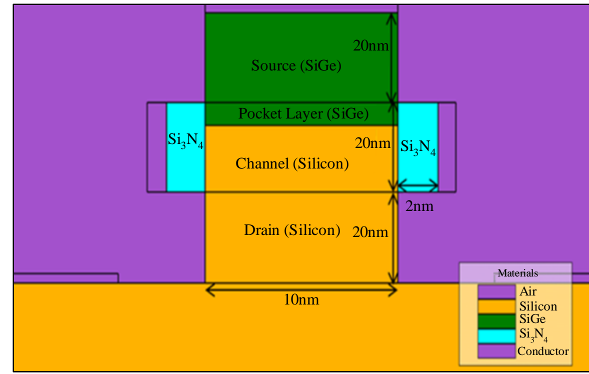

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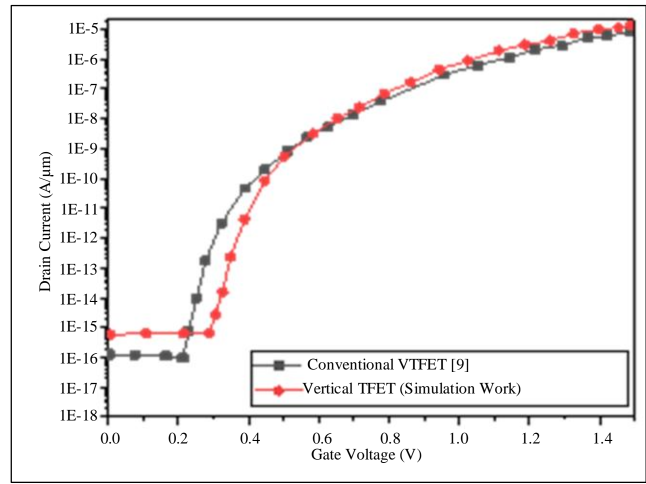


(c)

Fig. 1 (a) Cross-sectional view of a vertically grown SiGe Vertical Tunnel Field Effect Transistor without source packet (Hetero-VTFET WSP), (b) Schematic view of hetero-VTFET with source pocket (Hetero-VTFET SP), and (c) Calibrated output characteristic of the simulated Vertical TFET in comparison with the conventional vertical TFET [14].

Table 1. Device design values considered for the designed hetero-VTFET with and without source pocket

Design Parameter	Hetero-VTFET with Pocket	Hetero-VTFET without Pocket
Source Doping Concentration N_s[p type]	2e19 cm^{-3}	2e19 cm^{-3}
Channel Doping Concentration N_{ch}[p type]	5e16 cm^{-3}	5e16 cm^{-3}
Drain Doping Concentration N_d [n type]	5e18 cm^{-3}	5e18 cm^{-3}
Source, Channel and Drain Length	20 nm	20 nm
Pocket Length (SiGe)	5 nm	-
Gate Dielectric Permittivity of Si_3N_4	7.5	7.5
Thickness of Channel	10 nm	10 nm
Metal Gate Work Function	4.3 (eV)	4.3 (eV)
Gate Dielectric Width (tox)	2 nm	2 nm

3. Results and Discussion

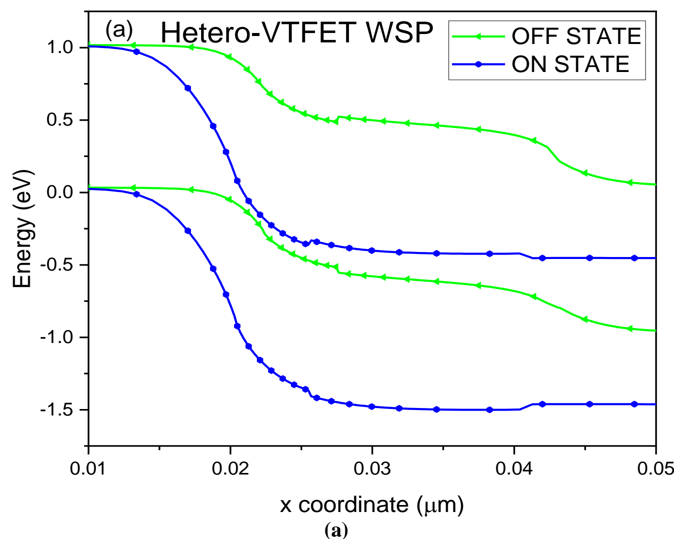
Various aspects of the Hetero-VTFET structure have been studied, including the energy band diagram, gate work-function variation, metal gate length variation, oxide length variation, electric field, and potential and described in depth in this part. For our suggested V-TFET architectures, we first calibrated the models utilised for simulation utilizing the Silvaco TCAD tool.

The measured data presented in [18] was compared to the TCAD simulation result of Hetero-Vertical TFET. We see a reasonable alliance between the two outcomes, indicating that the chosen models are acceptable. The non-ideal observed features of the conventional Hetero-VTFET device with an oxide width of 2 nm can be ascribed to a modest mismatch between the simulation and experimental outcomes in Figure 1(c).

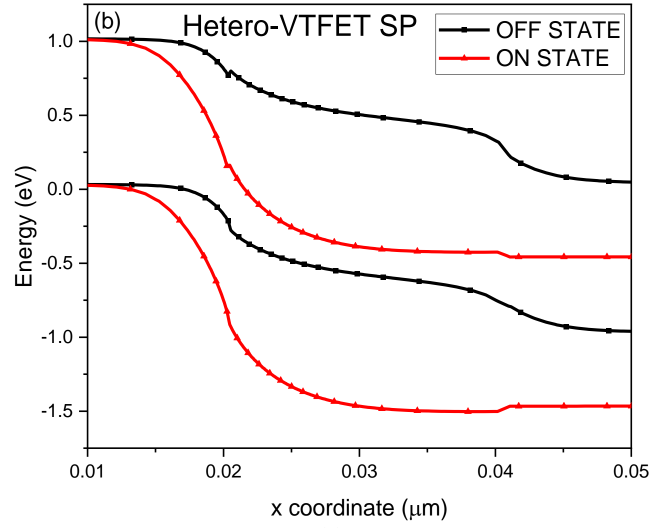
3.1. Energy Band Diagram

The energy band diagram of Hetero-VTFET with and without source pockets in off-state and on-state is displayed in Figure 2. For off-state conditions, the gate voltage and drain voltage are set at V_{GS}=0V and V_{DS}=1V, whereas in on-state-these-voltages are taken as V_{GS}=V_{DS}=1V. Tunnelling does not work at zero gate bias (off-state), which means that electrons cannot move from the source to the channel through it.

There is a big band bend when the gate bias is positive in the ON state. This means that when the source has electrons in its valence band, it lines up with empty states in its conduction band. When electrons move from the source's valence band to the channel's conduction band, they tunnel through. As shown in Figure 2. When the source and the channel are connected, the SiGe/Si makes a staggered hetero-junction at this point. Figures 2(a) and 2(b) show that the tunnelling via source/channel hetero-junction is boosted by putting a positive voltage on the gate.



(a)

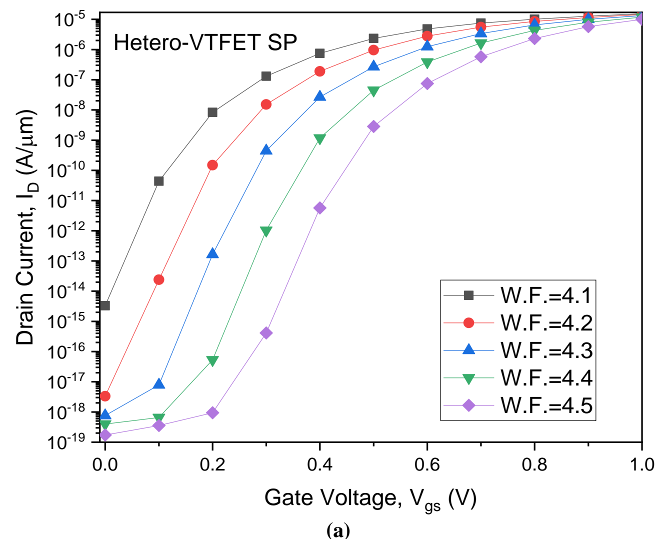


(b)

Fig. 2 (a) Energy band diagram of Hetero-VTFET WSP in the OFF-state and ON-state, and (b) Energy band diagram of Hetero-VTFET SP in the OFF-state and ON-state.

3.2. Gate Work Function Variation

The metal gate work factor is a major factor in the determination of the device's characteristics. To see how the work function affects the device's performance, change the gate work function at a time while keeping the other parameters at the same value. There is also a separate analysis of the effect of the work functions of both structures on the drain current analysed in the figure suggested below. Outcomes comparing the transfer and output outcomes of the new Hetero-VTFETs with and without pockets to see which one is better are shown in Figures 3(a) and (b), respectively. The ION/IOFF ratios of 2.39×10^{14} and 8.65×10^{12} are attained for SiGe/Si heterojunction-based VTFET SP and VTFET WSP, respectively. Figure 3 depicts the output characteristics for which the drain voltage (Vds) is kept at 1V and the Gate Voltage (VGS) is varied from 0 to 1 V.



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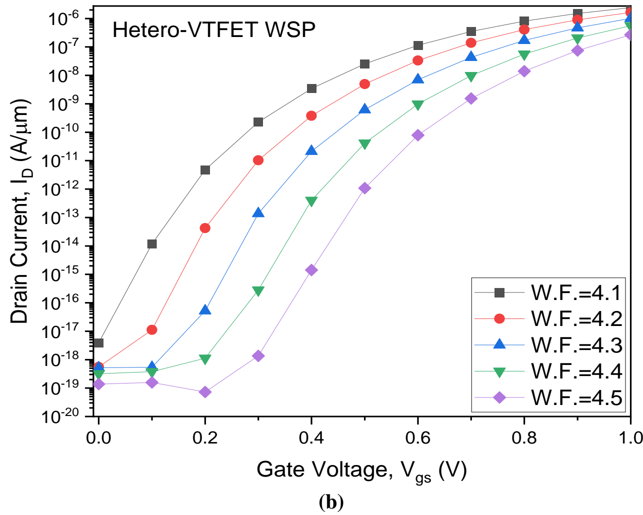
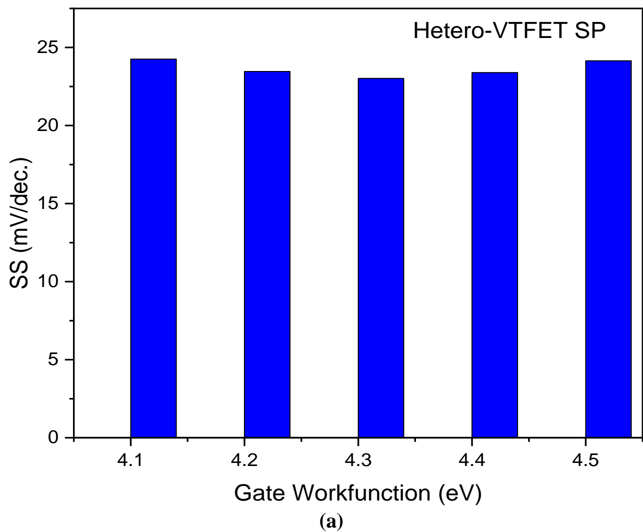


(b)

Fig. 3 I_{DS} -V_{GS} characteristics of (a) Hetero-VTFET SP, and (b) Hetero-VTFET WSP with variation in gate work function.



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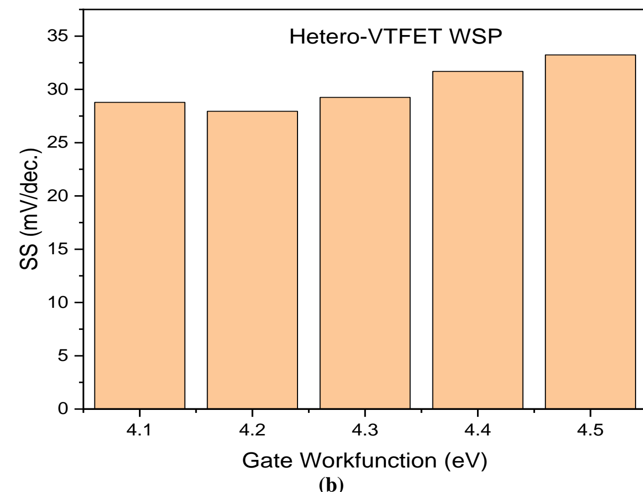
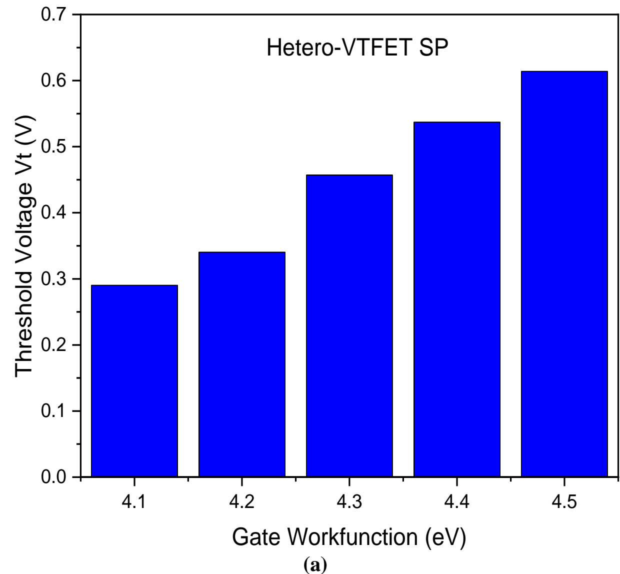


(b)

Fig. 4 Variation of Subthreshold slope (SS) of (a) Hetero-VTFET SP, and (b) Hetero-VTFET WSP with respect to gate work-function at V_{gs} =1V and V_{ds}=1 V.

Hetero-VTFETs with and without pockets are shown in Figure 5. They are analysed using different parameters, such as I_{ON}, I_{OFF}, as well as threshold voltage (V_T) and SS. In the case of Hetero-VTFET SP and WSP, the SSs are 24 mV/decade and 34 mV/decade, respectively. The gate work function is 4.5 eV for WSP and SP, both. We can see that the Hetero-VTFET SP is better than the Hetero-VTFET WSP in terms of both the I_{ON}/I_{OFF} ratio and the SS. When the Hetero-VTFET SP is turned on, it is worth noting that its ON current is higher than that of the Hetero-VTFET WSP.



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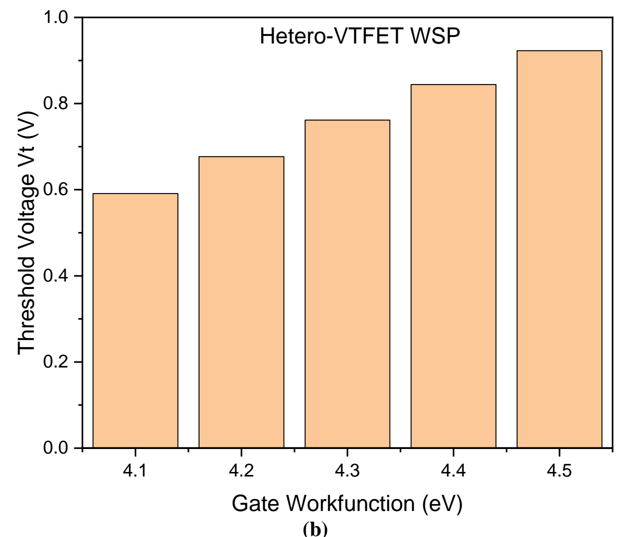


(b)

Fig. 5 Variation of threshold voltage (a) Hetero-VTFET SP, and (b) Hetero-VTFET WSP as a gate work function.

There is, however, a big difference between the SS in the Hetero-VTFET SP and the Hetero-VTFET WSP. IOFF is also found to be almost the same for both Hetero-VTEFTs. This means that the Hetero-VTFET SP structure has a higher ION/IOFF ratio than the Hetero-VTFET WSP structure, even

though both Hetero-VTEFTs have almost the same OFF-state current for almost all the time. The Hetero-VTFET SP device has better subthreshold performance than the Hetero-VTFET WSP device. This proves the SP device to be more promising than the WSP device for low-power applications. When you use Hetero-VTFET SP, you can get the same amount of I_d at a lower gate voltage than with Hetero-VTFET WSP. This makes Hetero-VTFET SP a preferred option for low-voltage and low-power applications.

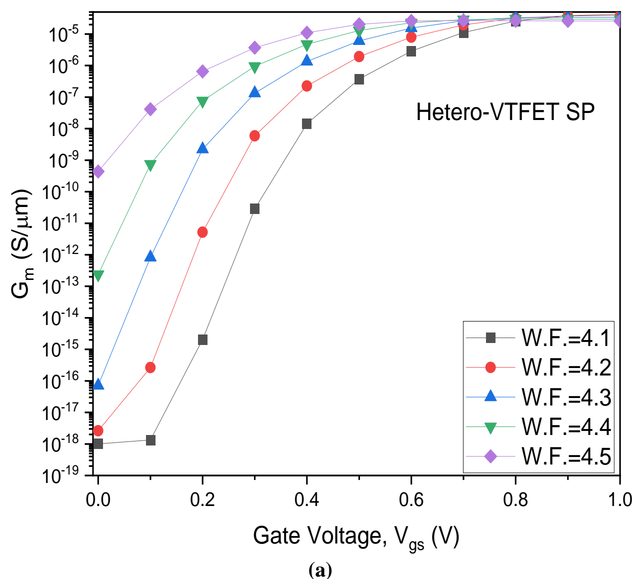
3.3. Analog/RF Analysis

In this segment, we lay a comparison of various analog Figures of Merits (FoMs) such as Transconductance (g_m), gate-to-drain Capacitance (C_{GD}), Gate-to-Source Capacitance (C_{GS}) of both Hetero-VTFET SP and Hetero-VTFET WSP. In Figure 6(a), you can see transconductance (g_m) characteristics of vertical TFETs, including and not including a pocket, of two Hetero-VTFET architectures. It is observed from Figure 6(a) that g_m of Hetero-VTFET SP is reasonably greater than that of Hetero-VTFET WSP with the maximum transconductance of 72 µS in Hetero-VTFET SP and 54 µS in Hetero-VTFET WSP.

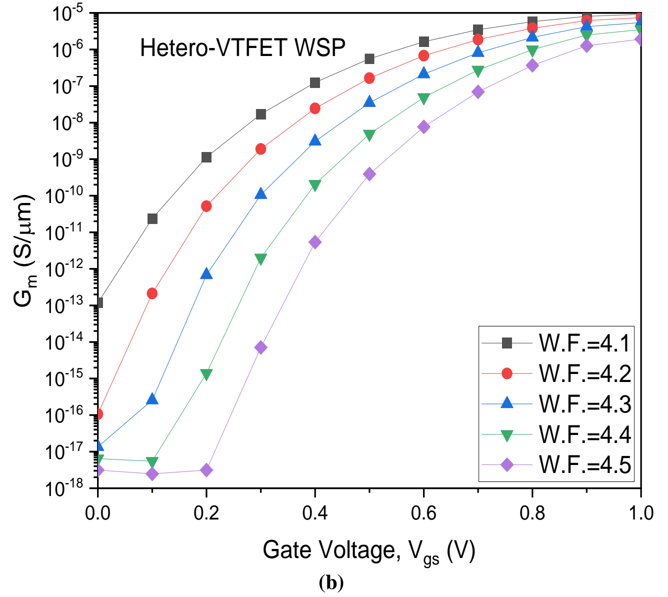
Hetero-VTFET SP has a larger g_m value than Hetero-VTFET WSP, which indicates that the device's capacity to convert gate voltage to drain current is superior in this arrangement. The vertical TFET-WP has a substantially larger g_d than the V-TFET-WSP, including and not including pockets, respectively, in terms of output conductance. There is a greater ability to convert voltage at the drain to current at the drain in the V-TFET-WSP structure as a result of this.

3.3.1. Transconductance Variation

The variation of the transconductance with the variation of the gate work function of Hetero-VTFET WSP and Hetero-VTFET WP is shown in Figure 6.



(a)



(b)

Fig. 6 Transconductance characteristics of Hetero-VTFET WSP and Hetero-VTFET SP with variation in gate work function

3.3.2. Capacitance Variations

Figure 7 displays the comparative plot of gate capacitance along the Gate-to-Source Voltage (V_{GS}) of VTFET WSP and VTFET WP. Total gate capacitance is a sum of Gate-to-Drain Capacitance (C_{GD}) and Gate-to-Source Capacitance (C_{GS}). Also, Intrinsic Gate Capacitance (C_{GG}) is an important parameter for the radio frequency figure of merits of any TFET transistor. Contrary to traditional Metal Oxide Semiconductor Field Effect Transistors, in TFETs, C_{GD} is denoted as parasitic or Miller capacitance, which is much larger than C_{GS} [24], as shown in Figure 7 for both the suggested TFET devices.

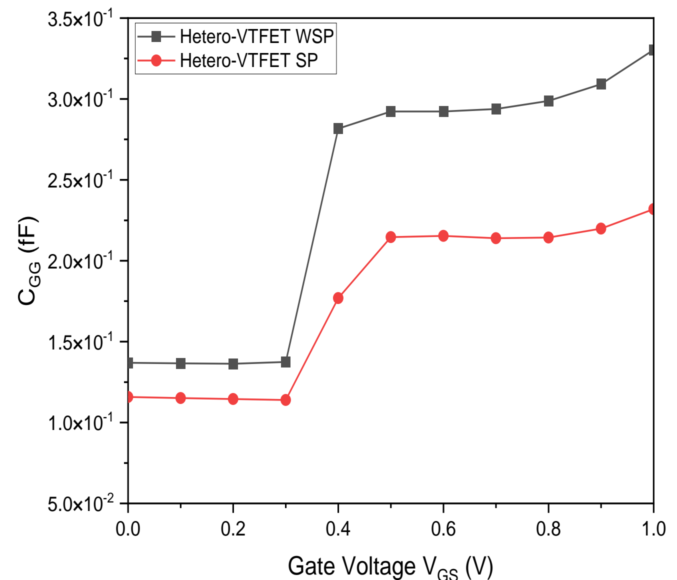


Fig. 7 Comparative plot of gate capacitance (C_{GG}) along gate-to-source voltage (V_{GS}) of Hetero-VTFET WSP and Hetero-VTFET WP

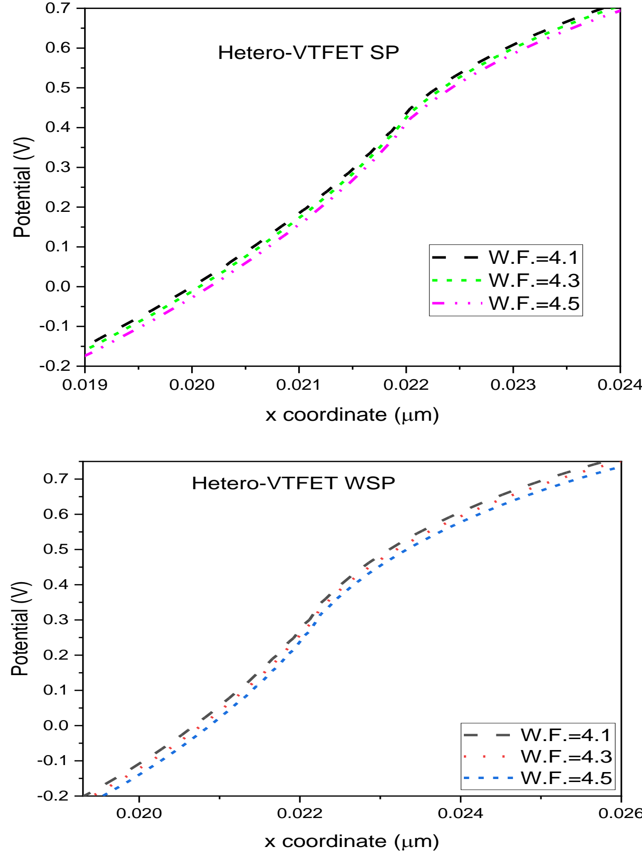


Fig. 8 Surface potential curves of Hetero-VTFET SP and Hetero-VTFET WSP with variation in values of gate work function

Figure 7 shows the comparison of the Cgg for two proposed devices. The Cgd of the Hetero-VTFET WSP is found to be larger than that of the Hetero-VTFET SP, as reported by Uchida et al. [22]. Hetero-VTFET SP with a smaller C_{GG} has superior circuit-level performance because of smaller parasitic effects, which were explored subsequently. Hetero-VTFET WSP has a higher C_{GG} value than Hetero-VTFET SP, even though the C_{GS} values in Figure 7 appear to be virtually identical for the two devices.

3.4. Surface Potential

The variation of the surface potential with the gate work function is plotted in Figure 8. It is observed that larger values of the gate work function result in lower surface potential at the source-channel interface. This is because the energy level difference between the source's valance band and the channel's conduction band reduces as the gate work function grows. The decreasing energy level difference results in a greater tunnelling barrier, which reduces the surface potential. The surface potential varies with the gate capacitance of the device.

Figure 8 shows the comparison of the surface potential for two proposed devices. The potential of the Hetero-VTFET WSP is found to be larger than that of the Hetero-VTFET SP. Figure 8 shows the comparative plot of surface potential with respect to a gate work function in which we found that as we increase the gate work function of both hetero-junctions structures the surface potential starts falling.

4. Conclusion

The article discusses the DC and RF characteristics of V-TFETs based on SiGe/Si hetero-junctions, including and not including source pockets. The simulation results demonstrate that the VTFET with Source Pocket (SP) structure has a lower SS ((~23 mV/decade), a lower threshold voltage (0.28 V), and a higher ION/IOFF ratio (~ 10^{14}) than the V-TFET without pocket being included (WSP) structure's corresponding values (~32 mV/decade, 0.59 V, and ~ 10^{12}). Due to the proposed device's extremely low OFF-state current, both devices exhibit a higher ION/IOFF ratio on the order of (~10^{12}) than previous heterojunction-based TFETs.

The Hetero-VTFET-SP structure suggested here offers superior thermal stability to the structure with no pocket included. The analog/RF research demonstrates that the SP structure of Hetero-VTFET outperforms the WSP structure of Hetero-VTFET. Additionally, we demonstrate that our proposed SiGe/Si heterojunction-based Hetero-VTFET SP device has superior analogue performance parameters compared to certain previously reported results for alternative TFET designs.

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