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Original Article

Design and Performance Evaluation of a 2.4 GHz High Efficiency Power Amplifier Using GaN HEMT for 5G Applications

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Abstract *- This study presents a highly efficient Doherty Power Amplifier (DPA). The design uses 10W GaN High-Electron-Mobility Transistors (CG2H40010F) for their characteristics, such as high breakdown voltage and power density. Advanced Design Software (ADS) was used to conduct the design. The design configuration employed a pair of individual Power Amplifiers (PAs) and connected them via a Wilkinson Power divider (WPD), which also facilitates the transmission of power towards the charge. The Doherty Power Amplifier (DPA) has been designed to offer high efficiency, output power, and wide bandwidth, in addition to expanding power back-off levels. It operates within the 2.0–2.8 GHz frequency range. The DPA topology replaces the previous quarter-wave transformer with a Wilkinson Power Combiner (WPD). Simulation results show a fractional bandwidth of 33.33%, a saturated output power of 44 dBm, and a higher gain of approximately 15 dB. Furthermore, Drain efficiency (Deff) and Power-Added Efficiency (PAE) stand at approximately 85% and 95%, respectively. After linearization, the design produced an output power of 39.171 dBm using a 100 MHz, 6.5 dB PAPR 5G NR DL signal at 2.4 GHz. Additionally, it achieved an ACLR of -56.88 dB for the adjacent channel. The outcomes of this study indicate that the proposed DPA achieves excellent drain efficiency, providing a solution for increasing DPA bandwidth while maintaining linearity. The intrinsic features of GaN devices, which allow for higher frequency operation and wider bandwidth, make this design ideal for 5G applications.*

Keywords *- Doherty Power Amplifier, GaN HEMTs transistor, Power added efficiency, Drain efficiency, Wilkinson Power Divider.*

1. Introduction

Modern wireless communications networks offer a wide range of services that fulfil the demands of the expanding number of mobile users. The services include video calling, video streaming, internet browsing, and downloading. The recent expansion of wireless systems is increasing demand for high-performance transceivers, resulting in the implementation of fifth-generation communication technologies [1, 2].

Parallel to the increase in the number of mobile users, there has been an increase in demand for higher data rates (at least 100 times higher than 4G LTE networks), lower latency (around one millisecond), lower energy consumption, improved reliability and security, and higher scalability. Hundreds of Gigabit-per-second (Gbps) and even Terabit-per-second (Tbps) lines are projected to become a reality in the near future [3, 4]. High data rates result in large modulation bandwidths. As a result, spectrally efficient signal modulation techniques are required to use the given bandwidth for the communications standard properly. This category includes modulation systems such as Quadrature Amplitude Modulation (QAM), Wideband Code Division Multiple Access (W-CDMA), and Orthogonal Frequency Division Multiple Access (OFDMA). These modulation methods generate signals with a large dynamic range and fast shifting envelope, resulting in a high peak-to-average-power ratio [5, 6].

High PAPR requires the power amplifier to be backed off from the most efficient point into a region where the power efficiency drops sharply to match the linearity requirements of specific communications standards [7]. Working in the power amplifier's back-off area results in lower efficiency since a considerable portion of the provided power is turned to heat. To preserve the signal's time-varying envelope, power

amplifiers with high linearity are required. High efficiency at the average power of the amplified signal is also necessary to avoid heat concerns in the base station transmitter and save operational costs.

Meeting these requirements simultaneously poses a formidable challenge in power amplifier design due to the delicate balance between various design parameters. Efficiency and linearity are the two primary considerations. The trade-off between efficiency and linearity is a common challenge in power amplifier design. Operating power amplifiers in class A or AB modes may result to high linearity at back-off level. Enhancing linearity is possible at various levels, such as gadget, circuit, and system. At the level of gadget, linearity could be enhanced by utilising field-plated HEMT structures similar to those found in GaN devices [8, 1].

To meet the multi-standard demands, it is imperative to develop a wireless transmitter that is both efficient and high-gain while also utilising a low-cost power amplifier. Typically, power amplifiers designed for battery-operated devices should be very efficient and linear throughout a wide power range. This is crucial in order to facilitate an accurate and efficient exchange of data between the RF transmitter and receiver.

Modern power amplifiers should be designed to achieve high efficiency with a large output Power Back-Off (PBO); well-known efficiency enhancement techniques include Doherty Power Amplifiers (DPA), Envelope Elimination and Restoration (EER), Envelope Tracking (ET), Linear Amplification using Nonlinear Components (LINC), and Chireix out-phasing [9, 10]. The Doherty power amplifier is widely employed to solve these restrictions since it has a simple design, high efficiency, and good linearity.

Doherty PAs can contribute to efficiency optimisation by ensuring linearity at maximum output power while delivering a high gain. In places where PAPR is low, the Doherty PA can significantly reduce PA heating by improving the efficiency of the drain, allowing for significant PAPR modulation at a high average output power. This prolongs the length of the PA (by increasing ACLR) and increases the maximum average output power due to improved PA outcomes and results [11].

In [11], Kaan Koca et al. present a wideband high-efficiency Doherty Power Amplifier (DPA) from 2.2 GHz to 2.8 GHz for LTE applications, increasing the operating spectrum to include LTE Band-7 and Wi-Fi frequencies. To increase back-off efficiency without sacrificing bandwidth, the proposed design structures included symmetric load-matching networks for broadband DPAs. However, it is important to note that methods aimed at enhancing back-off efficiency often result in reduced bandwidth. In addition, implementing a Klopfenstein taper network and symmetric load-matching networks introduced complexity to the DPA design. The measured findings revealed a great saturated output of 47 dBm power with 79% efficiency, but the back-off power is about 6 dB, which is low relative to modern communication. In contrast, the approach technique has a fractional bandwidth of around 24%.

In [12], A differential cascade architecture for both the carrier and peaking amplifiers of a 2.4 GHz Doherty power amplifier based on 22 nm CMOS technology is presented. The design, which aimed to maximise output power while maintaining reliability, achieved a power-added efficiency of 42.5% at 3.3 V supply voltage and 25.2% at 6 dB back-off power. However, the back-off power proved insufficient for the needs of current communication networks.

As mentioned in [13], Yuki Takagi et al. used harmonic suppression techniques at the second and third harmonics, as well as impedance optimisation at the fundamental frequency, to construct an Asymmetric Doherty Power Amplifier (ADPA) at 2.19 GHz. The simulation results provided a saturated output power of 46.3 dBm, and a drain efficiency of 72.1%, but the design had a low PAPR of approximately 8 dB. Furthermore, the design used load modulation with unequal saturation powers and a harmonic suppression technique structure, which implies complexity and high cost.

In [14], an asymmetric DPA design is presented and analysed by B. Wang et al. In order to enhance efficiency and power back-off levels. By employing this asymmetric method, the DPA was able to achieve 44% efficiency, which is very low compared to other methods, as well as 7 dB power back-off. Aritra Banerjee's study in [15] describes a high-efficiency multi-mode outphasing Radio Frequency (RF) amplifier built on 45nm CMOS technology. In a high-powered single-level approach, this power amplifier produces a peak output power of 31.6 dBm at 2.4 GHz, while drain efficiency is 49.2%.

The study highlights the importance of efficiency enhancement techniques in outphasing power amplifiers to maintain performance across different power levels and signal types. However, the technique introduced complexity and high cost. Furthermore, implementing multi-mode outphasing in RF power amplifiers indicates a limit of bandwidth expansion in outphasing systems due to the inverse cosine operation, making linearization through DPD problematic for signals with a wider modulation bandwidth.

As mentioned in [16], Shichang Chen et al. presented a reactance compensated three-device Doherty power amplifier for back-off range extension. The simulation results revealed a minimum drain efficiency of 41% spanning a frequency range of 2.0 GHz to 2.6 GHz at an 8 dB back-off range, with a saturation power of more than 43.6 dBm and a drain efficiency greater than 53%. The design also effectively prevents reverse power leakage by utilising shunt $\lambda/4$ lines and offset lines in the peaking PAs. However, the addition of the

compensating reactance in the load modulation network introduced a potential complexity that may increase design manufacturing and cost.

In [17], Ingchang Nan et al. presented a broadband Doherty power amplifier with a dual frequency matching circuit. The strategy focuses on enhancing bandwidth and efficacy at the Power-Generated Back-Off (OBO) by solving bandwidth restrictions commonly associated with DPAs. The simulation results show a frequency range of 2.4 GHz to 3.7 GHz, with a saturated output power of over 42 dBm. The drain efficiency ranges from 61.2% to 68.4%, whereas the 6dB back-off efficiency varies from 49.7% to 61.4%. The new modulation method involves replacing the quarter-wavelength transmission line with a dual-frequency matching circuit. However, the power back-off achieved is below 6dB, which is considered lower for current communication technologies. Additionally, the efficiency is relatively insufficient compared to other methods.

As mentioned in [18], Ardit Veshaj et al. presented a 20 W GaN Doherty power amplifier that operates between 2.8 and 3.6 GHz. The simulation resulted in a saturated output power of 42 dBm and a drain efficiency of 47%. In addition, the amplifier maintains an efficiency of over 42% at 6 dB power back-off within the frequency range, with a small signal gain of 10 dB. In comparison to other approaches, the efficiency and power back-off obtained are quite low. Also, the design used multistage Transmission Lines (TL) as a combiner, which may introduce complexity.

Joonhyung Kim's study in [19] presents a highly efficient asymmetric class-F−1/F GaN doherty amplifier. The design work uses derived basic current models to assess improvements in signal performance, such as output power and efficiency. A 2.4-GHz GaN Class-F −1/F DPA was developed and built with a peak output power of 44 dBm and a peak drain efficiency of 86.7%. However, asymmetrically, using class F-1/F necessitates complicated load-matching optimisation for varied device sizes.

As mentioned in [20], Ahmed M. Abdulkhaleq et al. presented a three-way Doherty power amplifier that employs class-F amplifiers. The design used three GaN HEMT transistors (6W, 25W, and 45W), resulting in an ideal power output of 76W at 3.4-3.8 GHz. The simulation outcomes mentioned a gain of 12.5 dB over the frequency range, with a maximum power output of 48.8 dBm. Furthermore, the drain efficiency at 13 dB OBO is calculated to be 55%. However, the design employed a three-way Doherty power amplifier construction, implying both complexity and expensive costing. Based on the previously related works, it is evident that the majority of power amplifier designs prioritise either size, cost, technology, bandwidth, back-off efficiency, or power-added efficiency. For current wireless communication systems, there is a need for power amplifiers that can effectively balance all these parameters. Some of the evaluated work has been done using CMOS technology. While the topic of class-E PA topology is undeniably important and warrants thorough exploration, it was not included within the scope of this particular study.

This decision was made to maintain a focused approach and ensure a comprehensive analysis of the chosen subject matter. However, recognising the significance of class-E PA, it is important to acknowledge the valuable contributions made in this area by other researchers. Notable works such as [21, 22] provide extensive insights and are recommended for readers seeking detailed information on this topic. Several domains benefit from and employ Doherty power amplifier designs that use CMOS technology. CMOS technology DPA design finds widespread use in mobile communication devices such as LTE, WCDMA, OFDM, RADAR, and transceivers. In terms of drawbacks, this technique has moderate power, moderate gain, and low power-added efficiency.

The typical output of a Doherty power amplifier is 35% PAE and a gain of less than 10 dB. This problem can be effectively addressed by leveraging GaN HEMT technology, which is currently in high demand and widely used. GaN HEMT offers numerous advantages, such as high electron mobility, high efficiency, high power, and so on. This technology's performance is impressive when compared to CMOS technology for power amplifier design. A Doherty power amplifier utilising GaN technology offers significant advantages, such as high gain and power-added efficiency.

This study proposes the design of a two-way GaN HEMTs Doherty power amplifier employing Wilkinson power divider and combiner network. Optimisation approaches are employed to enhance efficiency at various power levels, improve gain, and ensure sufficient bandwidth. The design and simulations presented in this paper were conducted using ADS (software). The rest of the work includes Section 2, which briefly describes the system design and optimisation choices as well as the design process for the DPA; Section 3, simulations, results discussions, and comparisons of the design performance relative to other DPAs. Finally, the conclusion is drawn in Section 4.

2. System Design and Optimization

W. H. Doherty first created the Doherty Power Amplifier (DPA) in 1936 at Bell Telephone Laboratories in Whippany, New Jersey [23]. As previously stated, Doherty allows for an improvement in output power while simultaneously expanding the input power envelope.

The device achieves this by maintaining a constant saturation level, leading to high efficiency. The Doherty power amplifier combines two amps in parallel. The upper amplifier is referred to as the main or carrier amplifier, and the lower amplifier is the auxiliary or peaking amplifier. The

primary amplifier is biassed at class AB, while the auxiliary amplifier is biassed at class C.

Doherty's structure is a two-way power amplifier that divides input signals into carrier and peaking active devices. It includes a power splitter, an impedance inverter, and an impedance transformer [24]. A DPA's performance is assessed using a variety of characteristics, including output power, gain, and efficiency, all of which have significance in evaluating system efficiency. Output power Pout is the power provided to an external load (typically 50Ω) at a specific frequency f or a frequency range B = [$fLow$, $fHigh$], and is represented as [23]:

$$P_{out} = P_{out(f)} = \frac{1}{2} Re\{V_{out}.I*_{out}\}; f \in fLow, fHigh] \quad (1)$$

Understanding the parameter gain is essential when it comes to designing a DPA. The calculation involves evaluating the power produced to the power consumed and expressing it as the ratio, as follows [23]:

$$G = 10log_{10}\left(\frac{P_{out}}{P_{in}}\right) \quad (2)$$

Where an amplifier's gain (G) in decibels, output power (Pout), and input power (Pin) in watts. Additionally, bandwidth should be taken into account when designing a DPA. As defined in reference [8], fractional bandwidth refers to:

$$BW(\%) = \frac{\Delta f}{fc} \quad (3)$$

The entire bandwidth is represented by Δf, while the centre frequency is denoted by fc. The centre frequency is typically determined by calculating the average of the higher and lower frequencies, resulting in:

$$fc = \frac{f_H + f_L}{2} \quad (4)$$

It is essential to consider the Power-Added Efficiency (PAE) and Drain Efficiency (DE) when assessing DPA performance. The PAE showcases the PA's capability to convert DC power into RF power. The calculation involves subtracting the RF input power, P_{in}, from the RF output power, P_{out}, and then dividing the result from the DC power, P_{dc}, as follows [23]:

$$PAE = \frac{P_{out} - P_{in}}{P_{dc}} \quad (5)$$

The Drain Efficiency, or DE, is calculated by determining the ratio of Radio Frequency (RF) generated to Direct Current (DC) dissipated, as outlined in the formula [23]:

$$DE = \frac{P_{out}}{P_{dc}} \quad (6)$$

The role of linearity in DPA design is vital, as it guarantees that the device's output will change in direct proportion to any variations in the input. Linearity is becoming increasingly important in modern RF communication systems. The evaluation of linearity typically involves displaying the power output in relation to the source power on a scale based on logarithms to determine the third-order Intercepted Point (IP3) value. Field-plated HEMT structures, such as those seen in GaN devices, are commonly used to improve linearity. Additionally, incorporating digital predistortion is a widely accepted method to fulfil the linearity demands of communication systems. Utilising memory Polynomial Digital Predistortion (DPD), the linearization process achieved ACLR values that met the necessary criteria for the associated communications systems [25].

2.1. Design Process

The Doherty PA conventional design process is ideal for restricted bandwidth amplification. The Doherty concept explains that the primary and auxiliary amplifiers function ideally as current generators, incorporating an impedance transformer and a power supply splitter. As the amplifier's bandwidth increases, it becomes more difficult to compensate for the main and peaking output reactance.

Additionally, wideband impedance transformers, input power dividers, input matching, and output combiners are recommended. The impedance inverter that connects the main and peaking amplifiers contributes significantly to the Doherty amplifier's narrow bandwidth. Figure 1 displays the structure representation of the proposed design. Wilkinson power is used in place of the impedance inverter.

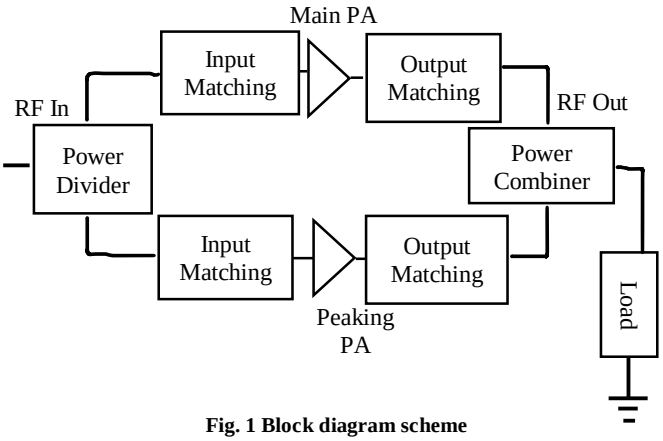


Fig. 1 Block diagram scheme

2.2. Stability Analysis

Verifying the stability of an RF amplifier is crucial, which may be done using stability factor K. To function as an RF power amplifier, a transistor's stability factor K must be larger than 1. When K is less than one, the gadget works as an oscillator. Figure 2 shows the set-up of stability analysis, while Figure 3 displays the simulation findings.

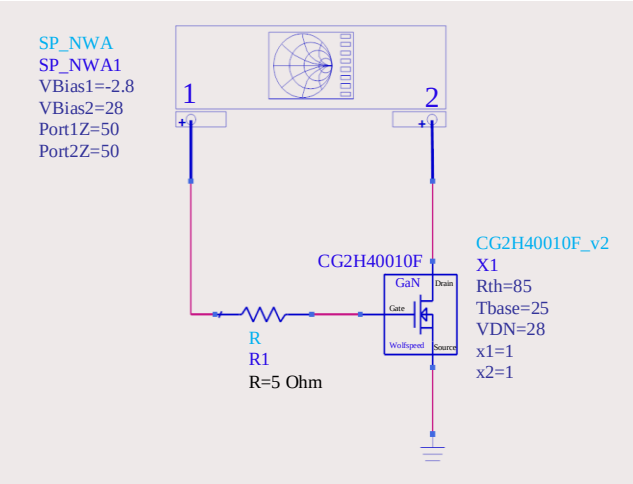


Fig. 2 Stability analysis set-up

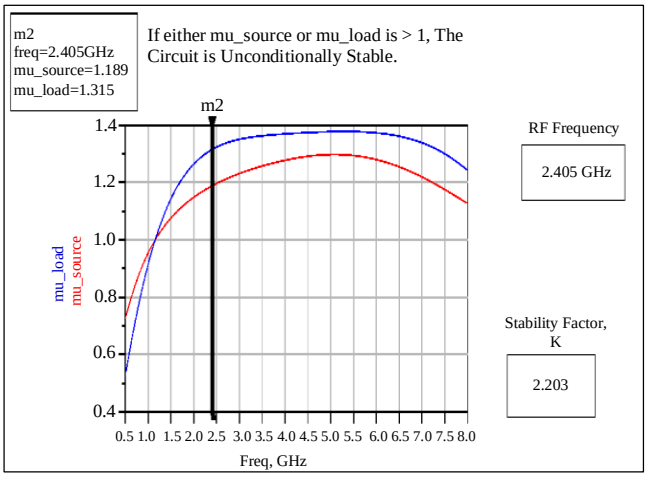


Fig. 3 Simulation results of stability analysis

2.3. Load Pull Analysis

The term “load pull” is commonly used to describe the systematic variation of the impedance presented to a Device under Test (DUT), typically a transistor. This process is employed to evaluate the performance of the DUT and the conditions required for optimal performance within a network. The concept of load-pull involves the manipulation of impedance at the load port.

However, it is also possible to vary the impedance at any of the ports of the Device under Test (DUT), typically the source. This process is commonly referred to as source-pull. According to the device datasheet, the values of Zsource and Zload corresponding to the frequency centre of 2.0 GHz are 16.7 - j*0.60 and 18.3 + j*5.94, respectively.

The ADS tool provides a set-up for calculating a transistor’s real input and output impedances. These values differ for maximum gain, PAE, and power. The impedance that yields the highest PAE is chosen for the matching network architecture. The ADS load pull arrangement for determining input and output impedances is shown in Figure 4. The simulation results reveal that the input and output impedances are 6.9 + j*0.904 and 13.306 + j*12.608, respectively. These values are used to design the matching network.

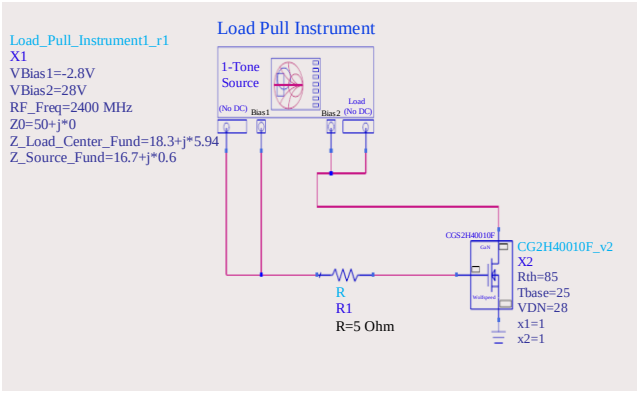


Fig. 4 Loadpull analysis set-up

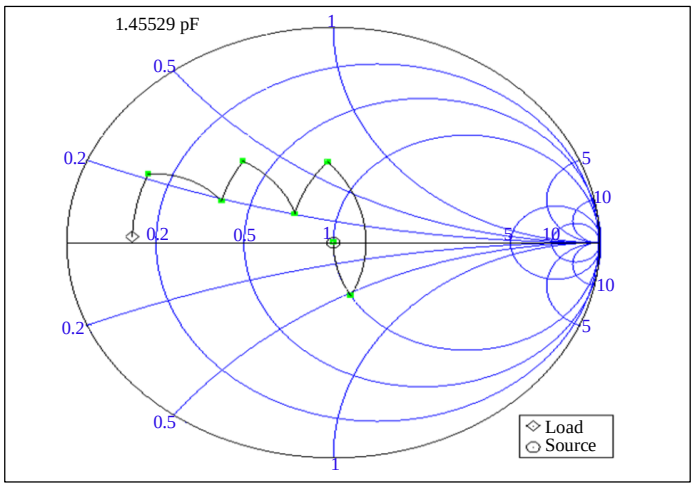
2.4. The DPA Matching Network Design

The Doherty Power Amplifier (DPA) requires the creation of a single Power Amplifier (PA) based on the Cree CG2H40010F chip. This is the design utilised for both the main and auxiliary power amplifiers, which are built within the DPA. This Cree CG2H40010F chip is an advanced 28 V rail-powered Gallium Nitride (GaN) High Electron Mobility Transistor (HEMT). It offers a versatile choice for a variety of RF and microwave applications.

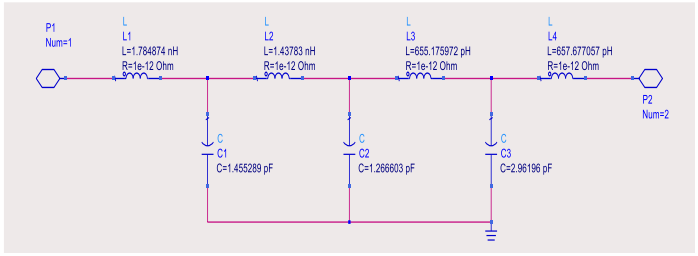
The component specifications for this single PA indicate that it can achieve 18 dB small-signal gain at 2.0 GHz, an optimum power supply of 17 W, as well as a maximum of 70% efficiency at saturated points [26]. The basic PA consists of a connecting source system, a component (transistor), and a combining system. Transformer matching, lumped element combining, and transmission line matching are some of the approaches available for creating matching networks. In this work, a microstrip transmission line, due to the fact that it is reasonably simple to manufacture and has favourable performance characteristics, is utilised for both input and output matching networks.

Initially, ideal network matching was created and eventually transformed into microstrip-matched circuits. The input-matched circuit was designed using a Smith chart, as depicted in Figure 5(a). The network schematic is shown in Figure 5(b). The same method is used for the output matching circuit. Figure 6(a) shows the converted input matching into a microstrip-matched circuit.

The appropriate output matching network was optimised using ADS software, which includes transmission lines for terminal transmission lines, open and short-circuits stubs, series capacitors for coupling, and a biasing circuit. Figure 6(b) shows the output matching converted into a microstrip matching network.

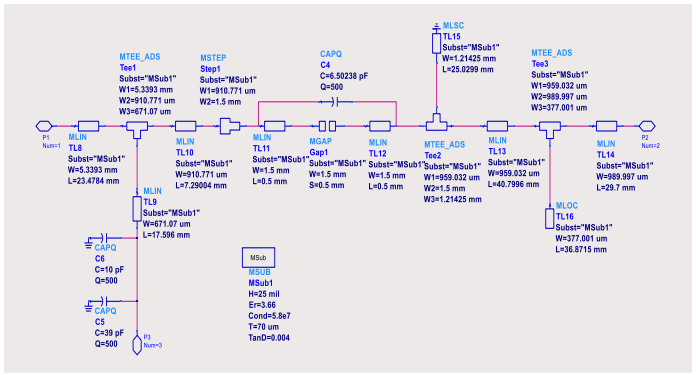


(a)

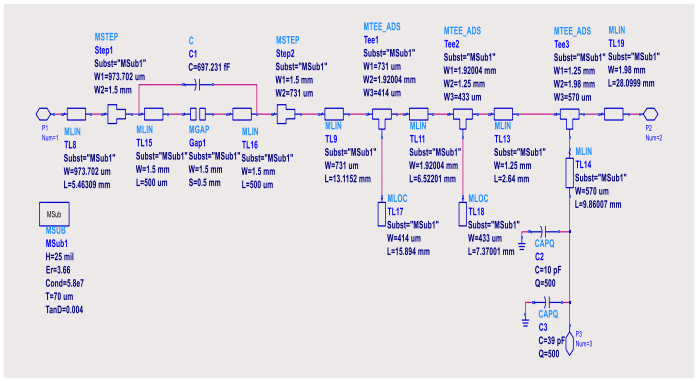


(b)

Fig. 5 Design process of matching networks: (a) Smith chart process, and (b) Network schematic.



(a)



(b)

Fig. 6 Matching network design: (a) Input matching network, and (b) Output matching network.

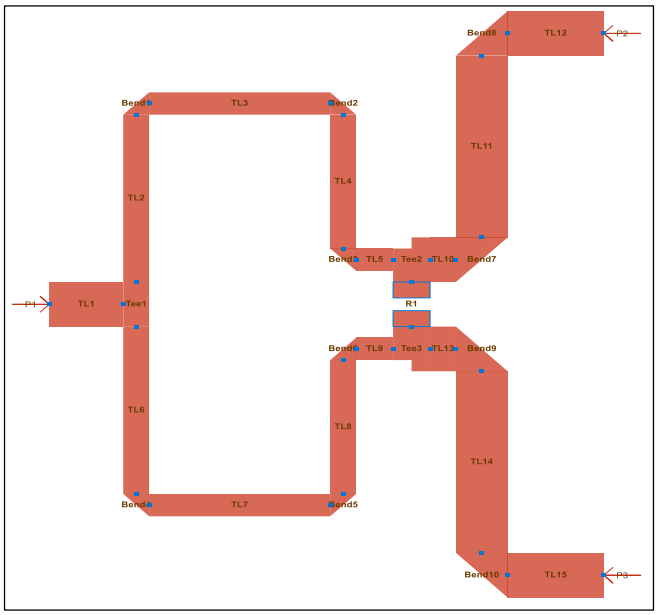
2.5. Power Splitter/Combiner Design

A power divider is required in a Doherty Power Amplifier (DPA) to guarantee that the input RF power is evenly distributed between the main and auxiliary amplifiers. The outputs of these amplifiers are combined at a resultant point using a power combiner. In this design, the Wilkinson power divided is used for dividing the power at the source and combining it at the endpoint. Initially, a planar model of a Printed Circuit Board (PCB) (shown in Figure 7(a)) is designed and analysed to achieve the desired performance. Then, it is converted to the schematic model structure shown in Figure 7(b). For Electromagnetic simulation, a substrate made of Rogers's 4350 material was employed. It has a dielectric coefficient (εr) of 3.66 and a thickness of 25mil.

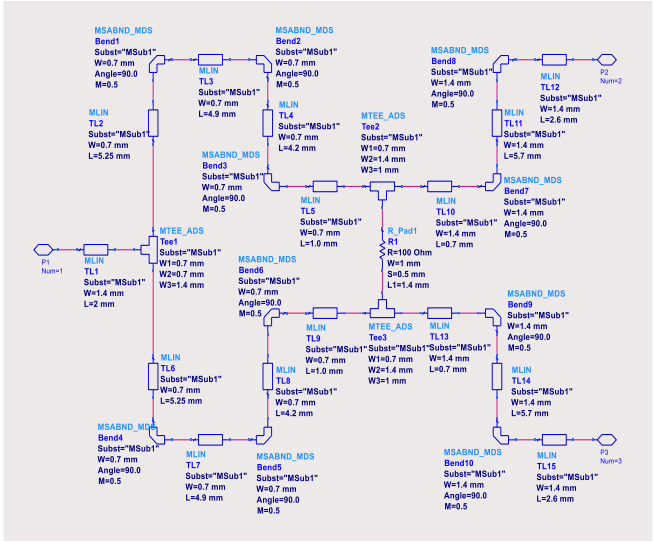
2.6. Schematic of the DPA

The Doherty Power Amplifier (DPA) depicted in Figure 8 is constructed using microstrip transmission line components, employing a couple of the same CG2H40010F components. Both the principal and peaking amplifiers get their bias using a 28V drain voltage and a gate voltage of -2.8V.

Rogers 4350 is the Microstrip Substrate (MSub) employed in the overall Doherty Power Amplifier design, with a corresponding dielectric coefficient εr=3.66, a thickness H=25 mil, an electric conductance Cond=5.8e7, a copper thin T=70um, and a loss tangent TanD=0.004. One-tone power (P_1tone power simulation) is used for the input signal.



(a)



(b)

Fig. 7 WPD design: (a) PCB power divider's layout, and (b) Schematic of WPD.

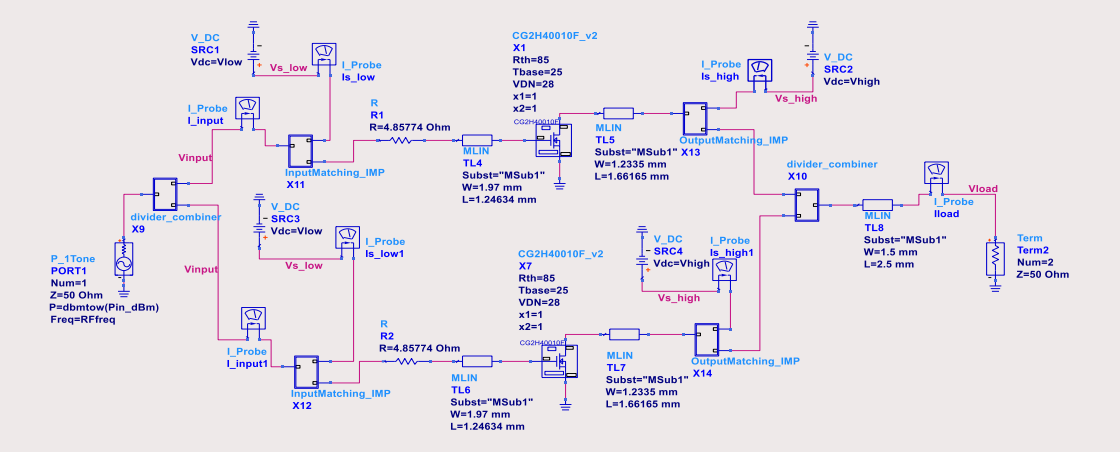
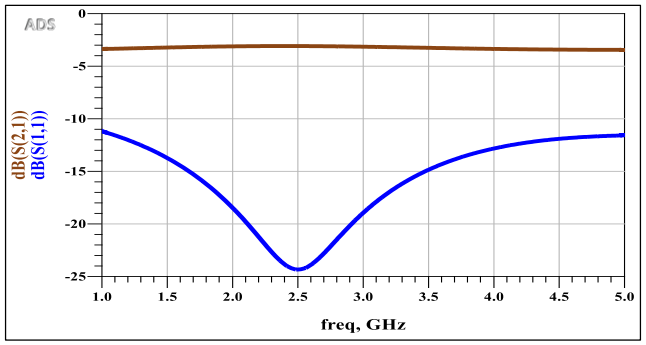


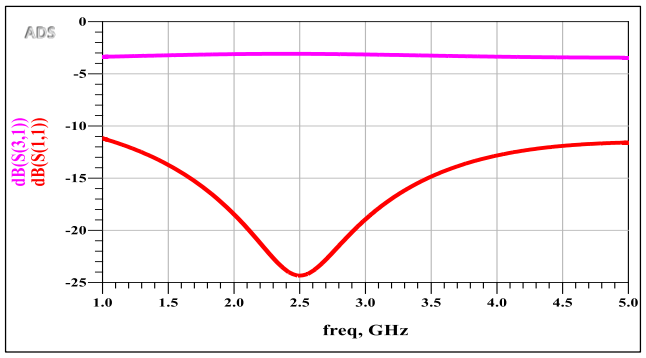
Fig. 8 Doherty power amplifier schematic diagram

2.7. Simulation Results and Discussion

This section presents the simulated results of the designed GaN DPA. Results of the S-parameters simulation for the Wilkinson, S-parameters simulation of DPA, gain and power delivered plots of the DPA Performance, Deff, and PAE plots of DPA, the output spectrum without and with DPD, and performance comparisons to recently reported DPA designs are all presented, respectively. The simulation outcomes of Wilkinson Power Divided are shown in Figure 9. The results for s-parameters indicate a reflection coefficient S11 below -11 dB over the entire frequency range, as well as forward transmission S21 and S31 of approximately -4 dB each.



(a)



(b)

Fig. 9 S-parameters simulation results of the Wilkinson: (a) S(2,1) and S(1,1) plot, and (b) S(3,1) and S(1,1) plot.

Figure 10 shows the simulation results for the DPA design's tiny signal performance. The input (S11) and output (S22) return losses are greater than -5 dB and -10 dB, respectively, within the frequency interval of 2.22 GHz to 2.68 GHz. They are also less than -10 dB for the rest of the band's frequency. The DPA's performances relative to gain (Gain_dB) and Power delivered (Pdel) are depicted in Figures 11(a) and 11(b), respectively.

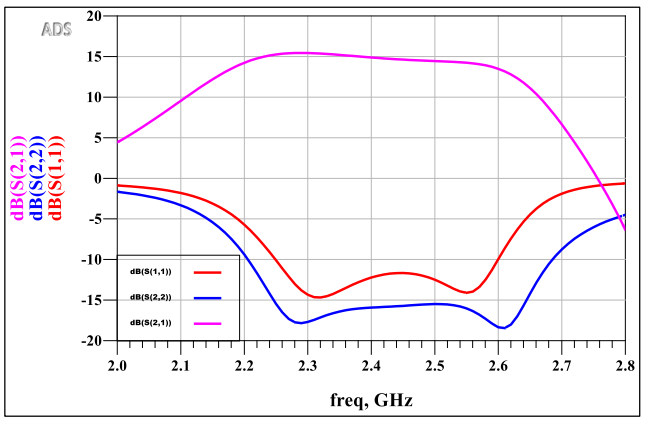
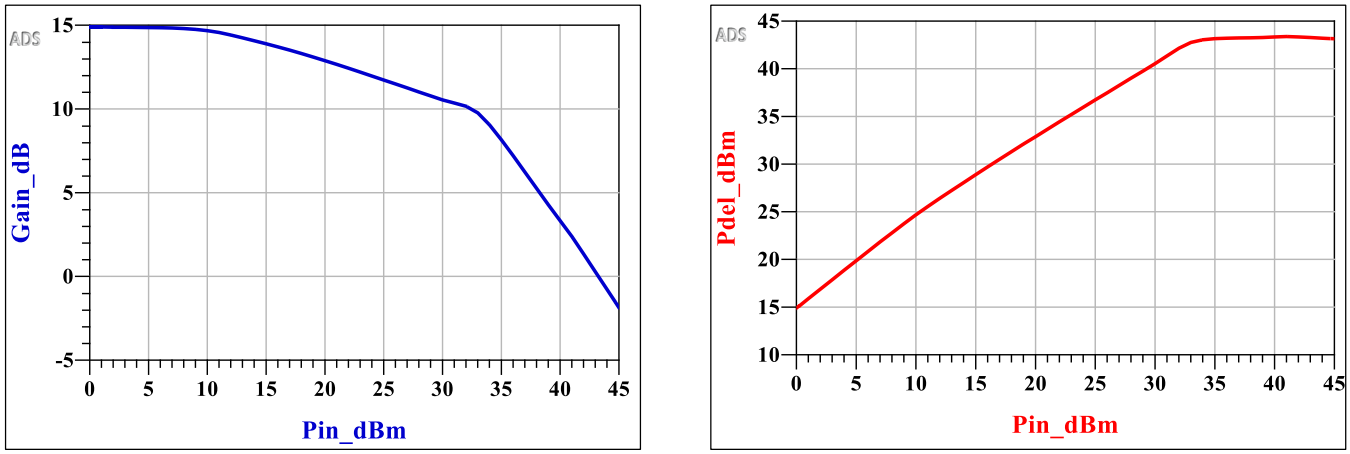


Fig. 10 S-parameters simulation results of the DPA

As depicted in Figure 11, plot (a) illustrates the relationship between large-signal gain and input power. At low input power levels, there is an initial gain of about 15 decibels (dB). However, when input power increases, the gain decreases owing to gain compression (1dB compression relationship). Furthermore, plot (b) shows the connection between the power provided and the source power, showing that a saturated output power of approximately 44 dBm is achieved. Figure 12 illustrates the simulated Drain Efficiency (Deff) and Power-Added Efficiency (PAE) of the amplifier. It shows that approximately 93% Deff and 85% PAE are achieved. Additionally, at an 11 dB backoff, the drain efficiency is between 20% and 75%. The proportional bandwidth of the designed DPA is 33.33%, based on a centre frequency of 2.4 GHz.



(a) (b)

Fig. 11 DPA's performance: (a) Gain plot, and (b) Power delivered plot.

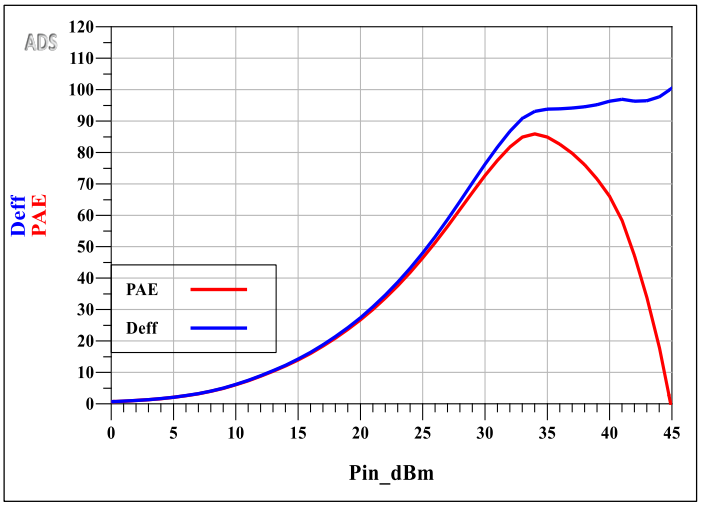


Fig. 12 Deff and PAE plot of DPA

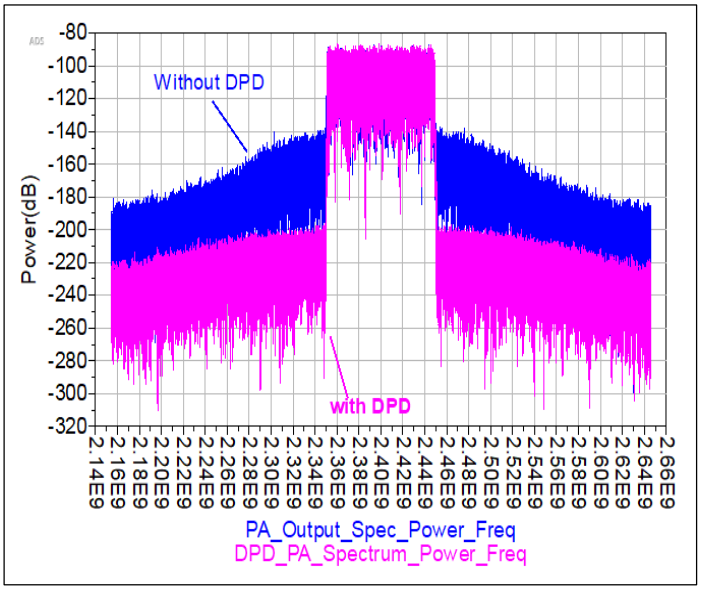


Fig. 13 The simulated output spectrum, both without and with DPD

Figure 13 depicts the observed output spectrum of a modulated signal before and after Digital Pre-Distortion (DPD). This investigation was conducted using the DPD-Explorer in ADS, which yielded an estimated power output of 39.17 dBm. The signal utilised is 5G NR DL with a modulation scheme of 256 QAM. The channel bandwidth is set to 100MHz. The crest factor reduction approach may reduce the PAPR of the modulated signal to 7.5 dB. Without DPD, the EVM PA output is -25.62 dB, whereas the ACLR PA output is -30 dB. With DPD, the EVM is increased to -55.72, and the ACLR is enhanced to -56.88 dB. The simulation results obtained in this study are compared to those from a previously conducted study, as depicted in Table 1. This work shows good performance compared to previous studies conducted in regard to gain, drain efficiency, and power-added efficiency. This is due to the use of the Wilkinson power divider as a combiner and GaN HEMT technology, with its characteristics such as higher breakdown voltage, bias voltage, power density, higher efficiency, better thermal properties, and more gain.

Table 1. Performance compared to recently reported DPA

Ref.	Frequency (GHz)	Gain (dB)	P_{out}sat (dBm)	Deff (%)	Deff@OBO (%)	OBO (dB)
[17]	2.4-3.7	13.6	42	68.4	49.7-61.4	6
[12]	2.4	20.1	30.7	42.5	25.2	6
[18]	2.8-3.6	10	44	76.5	44-56	6
[19]	2.4	9	44	86.7	68	6.5
[20]	3.4-3.8	12.5	48	70	50-60	13
This Work	2-2.8	15	44	95	20-75	11

OBO: *Output Backoff*

3. Conclusion

This study designs and simulates a Doherty Power amplifier employing a Wilkinson power splitter and combiner, as well as symmetric devices made of 10 W GaN-HEMT technology (CG2H40010F transistors). The design employs a simple process established by the fundamental Doherty scheme. The amplifier operates within the frequency band of 2.0 GHz-2.8 GHz and achieves an 11 dB backoff power.

Initially, a basic Power Amplifier (PA) is made to serve as the foundation for the DPA, which includes input and load power dividers and combiners. Microstrip transmission lines are used to build input and output matching networks for main and peak amplifiers. Simulation results demonstrated that using CG2H40010F transistors in the DPA produces an output power of more than 43 dBm, as well as a saturated Power Added Efficiency (PAE) greater than 80%, a Drain efficiency (Deff) of approximately 95%, and a gain of 15 dB. Comparative analysis with previous studies highlights superior performance in gain, backoff power, and PAE.

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