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Original Article

Design of Low-Power Low-Complexity High-Delay Flip-Flop

D. Srinivas[1], N. Siva Sankar Reddy[2], B. Rajendra Naik[3]

[1,2,3]*Department of ECE, College of Engineering, Osmania University, Telangana, India.*

[1]*Corresponding Author : sschandranaik@osmania.ac.in*

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Abstract - The *operation of deep sub-micron digital systems is dependent on power dissipation. Power is of the utmost importance in miniature systems. This work examines the use of traditional flip-flops. This work presents a unique master-slave flip-flop that combines fast speed with low power consumption. Master and slave latches make the flip-flop structure the most successful. In this paper, the flip-flop design uses 17 transistors in total to build master and slave circuits. The level of complexity, in particular, decreases with decreasing PMOS transistor count. This design produces a fast and compact flip-flop. The circuit in question employs a single clock. The proposed research has been modelled on the 45nm technology node. The present research includes PVT analysis to validate the reliability of the flip-flop. The proposed FF has a low power usage of at least 9.22%, less leakage power of at least 17.48%, and a clock-to-output delay of at least 68.37% when compared with the existing FFs.*

Keywords - *Power usage, Flip-flop, Delay, 45nm technology node, PVT analysis.*

1. Introduction

The proliferation of the IoT has led to a heightened need for SoC processors that operate at low voltages and consume little power. Instead of prioritizing speed effectiveness, current research efforts are concentrating on configuration area, power utilization, and leakage power usage [1]. A Flip-Flop (FF) has been the fundamental logic unit of digital VLSI, an extensively pipelined design that includes many FF-based designs. For instance, Internet of Things applications use conventional cells to synthesise low-power 32-bit microcontrollers with modest memory needs. In this arrangement, FF takes up more than 30% of the design space and consumes a significant amount of power [2]. As a consequence, FF is critical to the design's power efficiency and has a huge influence on the semiconductor industry.

The relevance of power efficiency has become increasingly important in the field of circuit construction. Researchers have successfully used a variety of techniques to reduce energy consumption. The major approaches used to reduce power usage include decreasing the source voltage using different VT library cells, using clock-gated techniques, using a multi-voltage structure with power switching, and allowing for both voltages as well as frequency scalability. Such advances might be used to design circuits. Using backend descriptions during the design process is crucial to enable the efficient storage and implementation of all cost-saving techniques [3]. In order to enhance efficiency, reduce energy consumption, and achieve smaller dimensions, designers must possess a comprehensive understanding of the minimum power consumption at every stage of the design process, including architectural and circuitry design elements [4, 5].

It is highly encouraged to carefully track and maintain the IC's power consumption from its original design through its final implementation. The key goal is for specialists to continuously engage at all stages of the design deployment procedure in order to maximize efficiency and capitalize on any possible opportunities to improve power efficiency. Investigators specializing in ICs should keep track of their power usage. These investigators face significant challenges in developing creative strategies to reduce energy usage and adhere to power management criteria in this specific discipline. The fundamental goal of this research is to increase the functionality of a semiconductor device by employing the flip-flop concept. The current design technique focuses on power optimization, seeking to reduce power leakage and dynamic power utilization in various design components. The standard methods [5, 6] discussed the reduction of the power utilization of design. The primary goal of this study is to achieve a minimal layout area design approach in the FF architecture with reduced voltage and power usage.

Section 2 conducted a literature survey on existing flip-flops. Section 3 presents a demonstration of the proposed flip-flop. Section 4 presents the simulation results of the proposed flip-flop, while section 5 concludes the discussion.

2. Review of Flip Flops Using Different Logics

Digital system architecture commonly employs a flip-flop as a fundamental storage component. Low-power electronic devices frequently employ flip-flops. In order to get an extended battery life, every gadget needs to exhibit minimal power consumption. To attain a high processing speed, it has become crucial to minimize the delay of the memory units [8].

Traditional flip-flops are those resembling the Set-Reset Flip-Flop (SRFF). Contrarily, as Figure 1 shows, the Transmission Gate Flip-Flop (TGFF) has become popular and practically viable. The higher clock load constitutes the system's main problem. The clock signals utilized by the two flip-flop logical structures are CLK and CLKbar. The signals, as mentioned above, improve the quantity of transistors overall in addition to the clock input load. The additional circuitry required to generate the CLK and CLKbar signals affects the entire architectural structure. As a result, there is a notable rise in dynamic power distortions, regardless of whether the data switching rate is minimal.

Currently, the VLSI sector is primarily concerned with the manufacturing expenses and the size of the chips. Almost all sectors in the digital domain require electronic devices that are both economical and compact. Therefore, it is essential to consider reducing the silicon footprint that CPUs occupy. The True Single Phase Clocking (TSPC)-based flip-flop architectural logic is used to minimize the load on the clock pulses. Irrespective of the constant input, as the demand on the clock grows, so does the power use in direct proportion.

TGFF has a larger clock loading issue because it uses only one clock that drives 12 transistors. Flip-flops, such as the Adaptive-Coupled Flip-Flop (ACFF) in Figure 2, the Topologically Compressed Flip-Flop (TCFF) in Figure 3, and the Logic structure Reduction Flip-Flop (LRFF) in Figure 4, demonstrate a significant increase in power usage due to clock overloading.

To provide TSPC capability, the ACFF design employs the differential latch instead of the usual SRFF structure. In this case, pass transistors replaced the transmission gate, coupled with two Level Restorer (LR) circuitry. The LR circuitry involves a form of parallel connection that incorporates one NMOS and one PMOS. The clock pulse actuated just four of the 22 transistors.

The ACFF slave's subsequent drop becomes much more visible. Data conflict issues can often cause latching difficulties. As the level of switching activity increases, by substituting the SRFF master with an extra multiplexer, we were able to reduce the clock burden and build a TSPC Flip-Flop (FF) architecture, referred to as TCFF. Using a conceptually reduced technique, a single clock input reduces energy consumption.

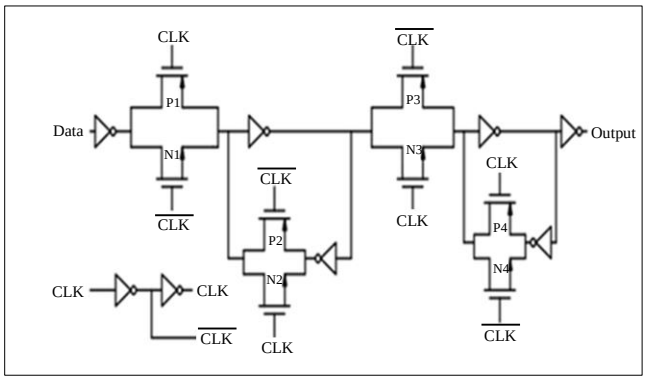

Fig. 1 CMOS implementation of TGFF [9]

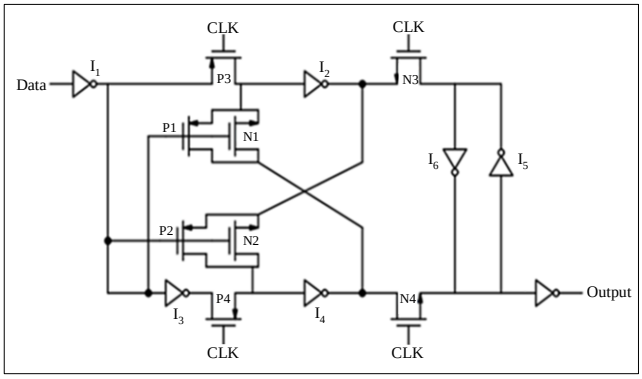

Fig. 2 CMOS based implementation of ACFF [10]

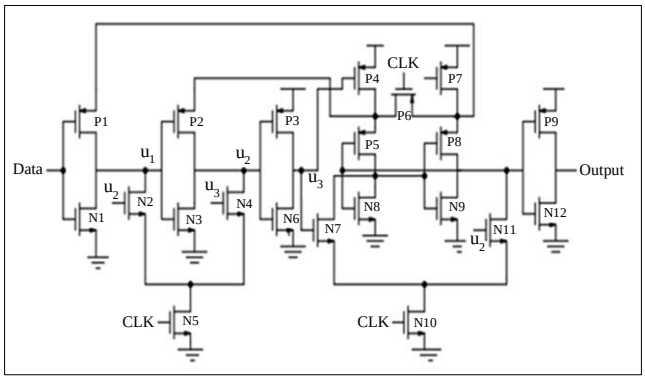

Fig. 3 CMOS based implementation of TCFF [11]

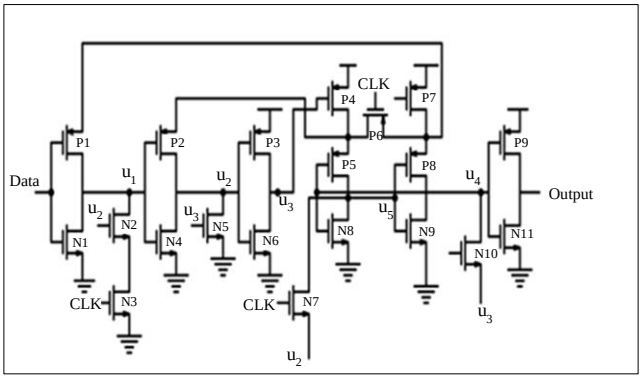

Fig. 4 CMOS based implementation of LRFF [8]

TCFF had fewer transistors than SRFF. LRFF is an upgraded variant of TCFF. The design employs Complementary-pass Transistor Logic (CPL) architecture. The CPL design is composed of a pass transistor that transmits the clock's pulse through the gate terminal, with terminals 2 or 3 serving as the signal drain. The slave side has two charging channels, each comprised of two pass transistors with a CPL design. It streamlines the process of charging nodes 4 and 5 to a logical high state, represented by "1". The paper outlined the development of a flip-flop known as the Conditional Clock Technique (CC-LCFF).

Lin et al. [12] proposed a real single-phase FF with minimal voltage and minimal power requirements. This design minimizes the total number of transistors by implementing a pass-transistor logic design approach. The use of optimization strategies has resulted in a novel flip-flop architecture that exhibits improved performance in numerous aspects, including speed, power usage, energy efficiency, and layout space. The suggested design uses 53.6% less power and 63.2% less energy than the standard transmission-gate-dependent flip-flop architecture, according to simulations. The authors developed and implemented shift-register architecture to enhance the efficiency characteristics of the suggested architecture.

Chenyu Yin et al. [13] introduced novel D flip-flop architecture. By prioritizing SEU fortifications above circuit speed, this construction enhances its SEU cutoff by a factor of 10 in comparison to conventional D flip-flops. Furthermore, a comparison with Dual Interlocked Cells (DICEs) revealed a reduction of 6 transistors in terms of space expense compared to the DICE architecture. When running according to the same settings, the average power usage and peak energy usage for the system remain 9.8% and 18.8% less, respectively, compared to the DICE circuits.

Park et al. [14] designed a Flip-Flop (FF) that uses a dual change-sensing technique to decrease the frequency at which the internal nodes change. Furthermore, the authors introduce a novel method to reduce short-circuit currents, specifically chosen to minimize energy consumption. The Dual Change-Sensing Flip-Flop (DCSFF), which has 24 transistors, uses the least amount of power when paired with regular flip-flops, no matter how much information is being processed. The DCSFF can reduce power by 98% and 32%, respectively, according to experiments using a 65 nm CMOS fabrication method.

Simultaneously, the data rate approaches both 0% and 100%, similar to a typical transmission-gated flip-flop. Furthermore, the power consumption of DCSFF is 26% less compared to the equivalent of change-sensing FF, although the data transmission speed is about 100%. The architectural approach of FF keeps on improving with the advancement of new process technologies, FF's architectural approach continues to improve.

Novel concepts are necessary to meet specific application criteria, which include minimal voltage, minimal power consumption, and inexpensive or high efficiency [12–21]. The goal of this research is to develop a design method that incorporates low voltage, minimum power utilization, and FF topology.

3. Proposed High-Speed, Low-Power Flip-Flop

Considering the limitations of earlier low-power flip-flop designs, a more advanced approach is suggested. This approach involves applying additional circuit architecture reduction techniques to ACFF implementations. The suggested design uses a mixed type of logical circuitry. The master level has a CMOS-style SR-latch, and the slave phase has a PTL approach to SRAM-based latching. This hybrid approach is used to decrease the entire complexity of the circuit. Figure 5 illustrates the presence of 17 transistors as per the suggested circuit architecture.

This MOS transistor design advises using the following transistor-level solutions to minimize the quantity of n-MOS devices. Pull-down circuit controls nMOS devices with a single signal, generally referred to as "N2." Figure 5 demonstrates that two separate paths responsible for discharging can utilize this signal. It is important to note that while the Clock Signal CLK remains in a high state, the transistor N1, which serves as the master latch, maintains the input phase. This scenario activates the NM14 transistor, which controls the slave latch. Therefore, the slave latch additionally functions as a means for discharging the primary latch.

Consequently, it could eliminate the needless duplication of a single n-MOS transistor under clock signal control, thereby simplifying the design. This method may lower not only power utilization and designing area but also reduce the amount of capacitance load connected with the clock. Typically, reducing the number of transistors to achieve a completely static architecture leads to a decrease in power consumption due to leakage. In our design, the overall transistor number is 17, which includes 8 pMOS devices and 9 nMOS devices. Only five transistors operate this flip-flop design, which utilizes a single-phase component of the clocking signal. In the FF circuitry architecture, the suggested design incorporates a combination of completely complementary logic and pass-logic transistors. It effectively accomplishes the goal of enhancing the delay value while minimizing circuit intricacy. Figures 5-9 illustrate the functionality of the suggested FF with various inputs, such as data input and clock input. The blue cross marks represent the OFF transistors, while the red lines indicate the pathways for discharging. Figure 10 illustrates the simulated waveforms of our method of operation. The FF structure operates effectively under all conditions, and each node has a complete voltage range.

4. Results and Discussion

The following part showcases the results of the proposed flip-flop architecture, including subsections that analyze the flip-flop's assessment based on several criteria. We have determined the performance parameters for the intended flip-flop and generated the calculated results using Cadence Virtuoso's 45 nm FINFET technology. The performance of the proposed flip-flop has been evaluated in comparison to similar devices using a 45 nm process.

A comprehensive study has been conducted to assess its power consumption, response time, susceptibility to process fluctuations, voltage variations, and stability properties. The temperature had been controlled to approximately 27°C by employing a power source operating at a supply voltage equal to 1 volt. Table 1 offers a succinct summary of the analytical features utilized. The investigation examines a variety of process characteristics, including supply voltage changes of 0.7 V to 1 V and temperatures ranging from -50°C to 75°C.

The subsequent sections examined the functional characteristics of the proposed flip-flop in comparison to the qualities of the existing flip-flops under evaluation. The size of MOS transistors is decided by maximizing the power-delay product and their efficiency at low supply voltage. Table 1 shows the physical dimensions of the MOS transistors in the recommended design, particularly the minimum size.

Table 2 shows a performance comparison between the proposed flip-flop and current flip-flops. Table 2 shows that the proposed FF consumes at least 9.22% less power, has at least 17.48% less leakage power, and has at least 68.37% shorter clock-to-output time than current FFs. Figure 11 shows that since the proposed flip-flop has fewer PMOS transistors and no contention problems, it uses less power in all process corners than conventional designs.

Figure 12 shows that, compared to conventional designs, the suggested flip-flop uses less power at different supply voltages between 0.7V and 1V. Figure 13 demonstrates that the suggested flip-flop consumes less power than conventional layouts across a temperature range of -25 °C to 75 °C.

According to PVT analysis, the figures indicate that the proposed flip-flop cell meets the power use requirements. Intrinsic variations in parameters, such as oxide layer alterations, line edge flaws, and probability dopant variations, greatly impact the functionality and yields of devices. We used a Monte Carlo computer model to evaluate the suggested flip-flop empirically. The simulation had a sigma total of three and 200 samples. Figure 14 shows Monte Carlo research examining power usage during flip-flop operation. The suggested flip-flop cell has 10% variations in power usage while switching.

Table 1. Simulation Configuration

Parameter	Value
CMOS Technology (nm)	45
Transistor Dimensions(W/L)	NMOS Transistors: 1/1 PMOS Transistors:2/1
Source Voltage (V)	1
Temperature ^{0}C	27

Table 2. Performance comparison of proposed FF w.r.t existing FFs

	[12]	[14]	[22]	[23]	[24]	Proposed FF
Power Consumption (pW)	371.61	348.81	390.91	403.92	449.18	267.3
Leakage Power (pW)	167.65	152.42	176.98	191.29	259.18	138.36
Clock to output (Q) (nS)	71.1	69.1	78.4	261.9	240.1	50.15
Power Delay Product x10^{-18} W/S	26.42	24.1	30.64	105.78	107.84	13.4

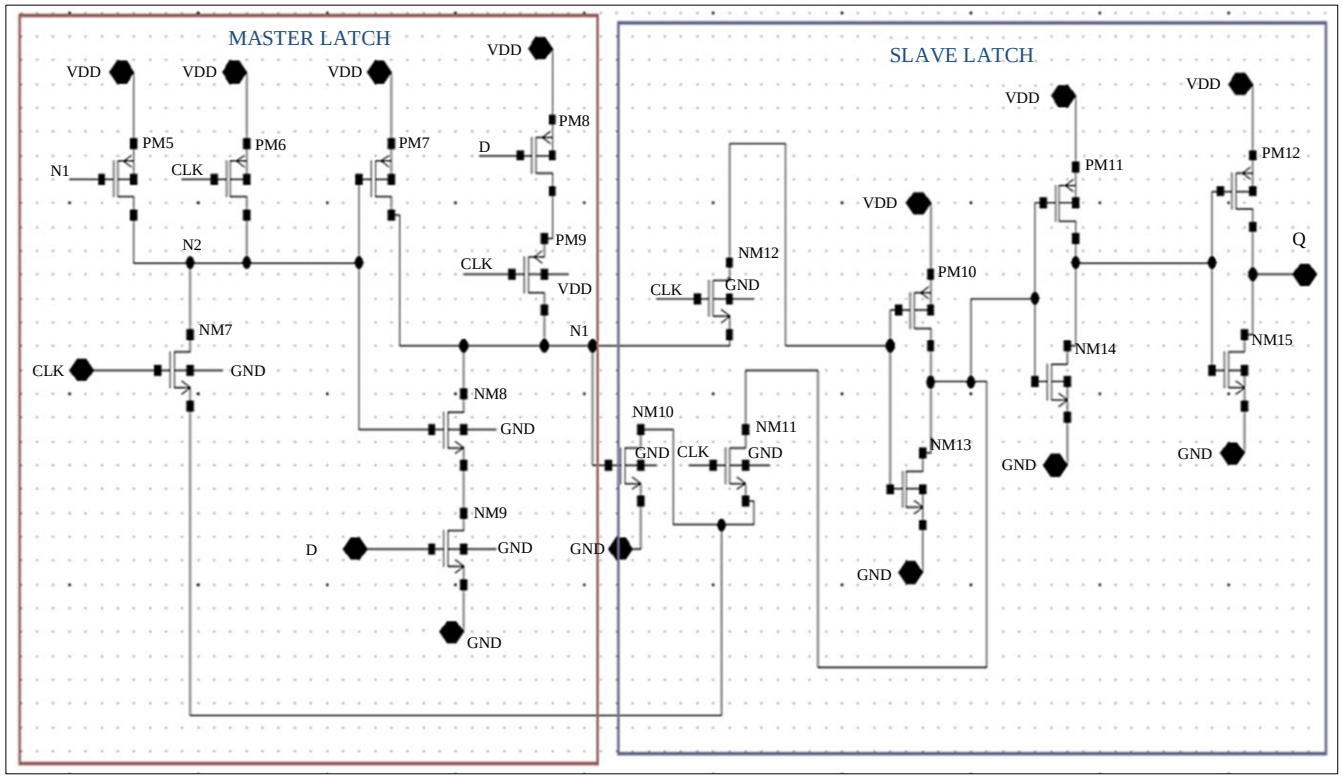

Fig. 5 Proposed high-speed, low-power flip-flop

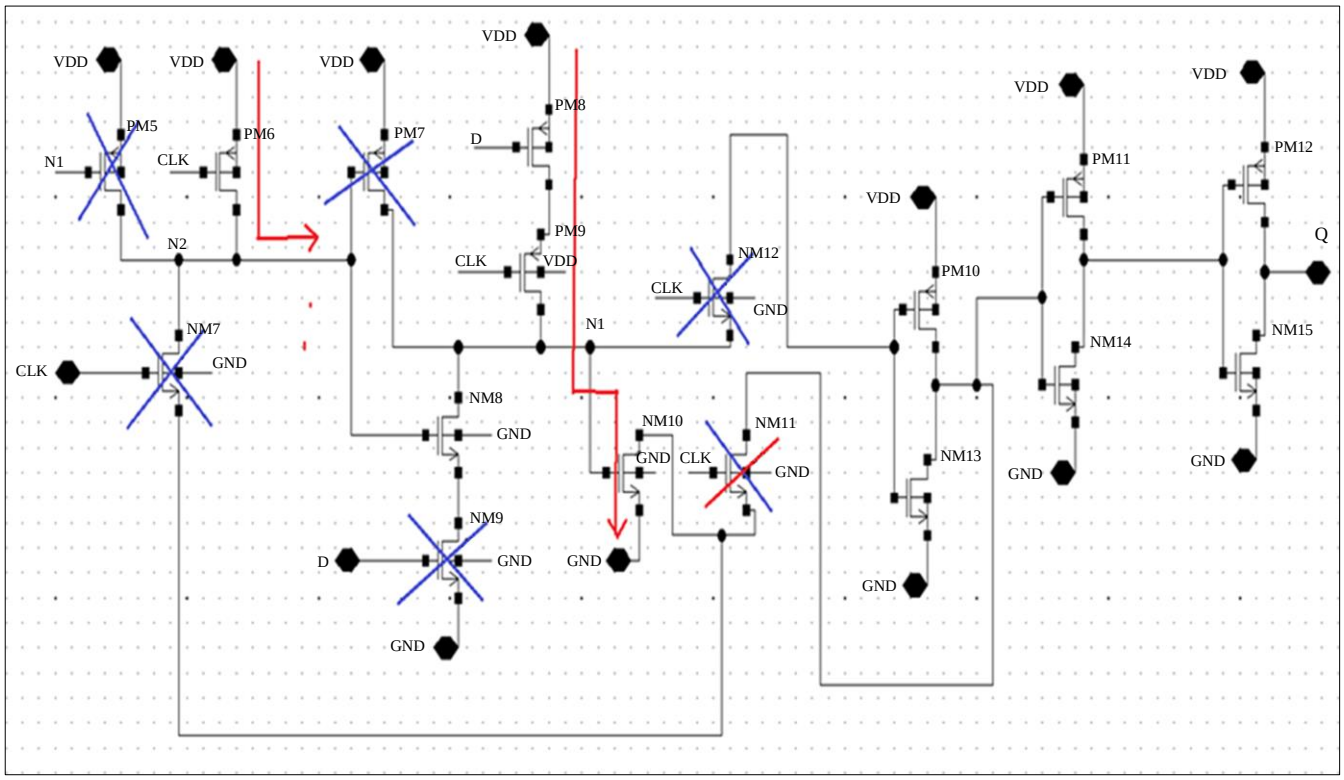

Fig. 6 Operation of proposed FF when CLK=0 & D=0

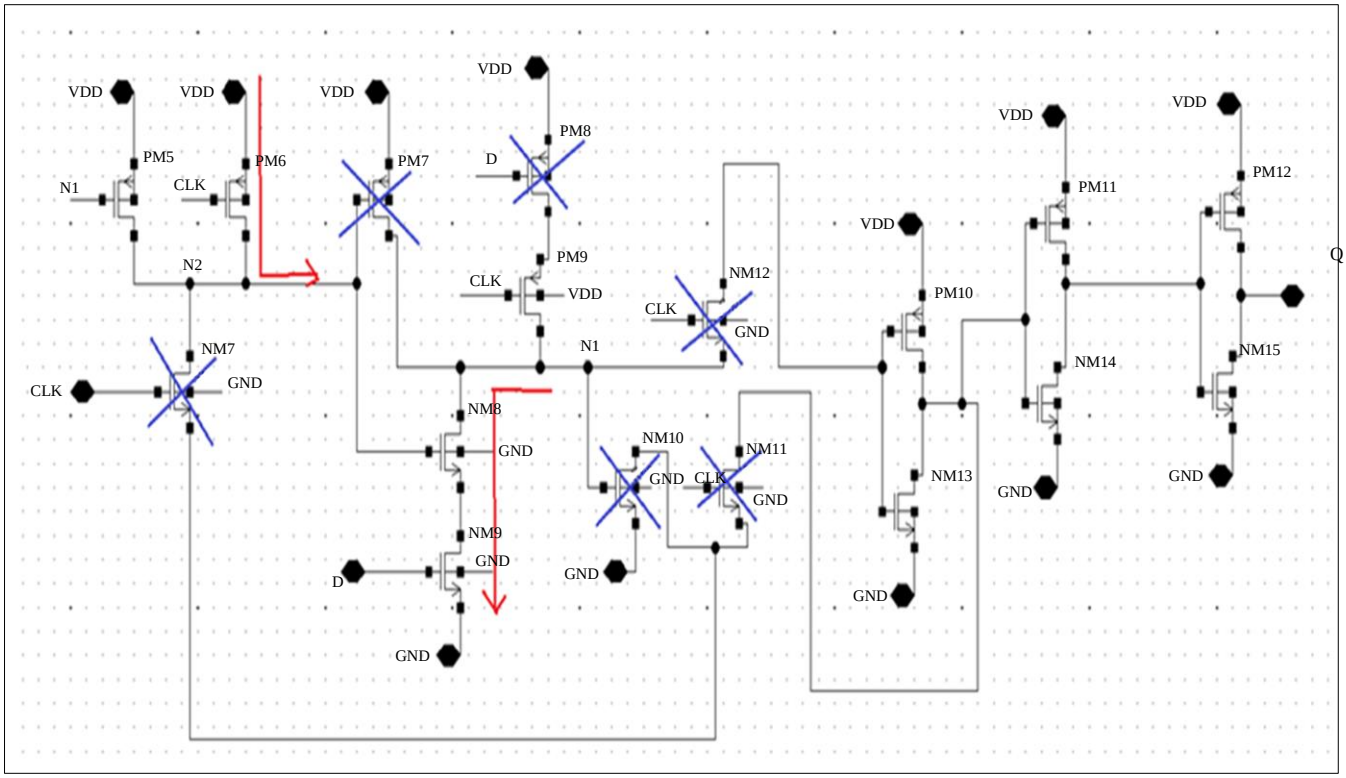

Fig. 7 Operation of proposed FF when CLK=0 & D=1

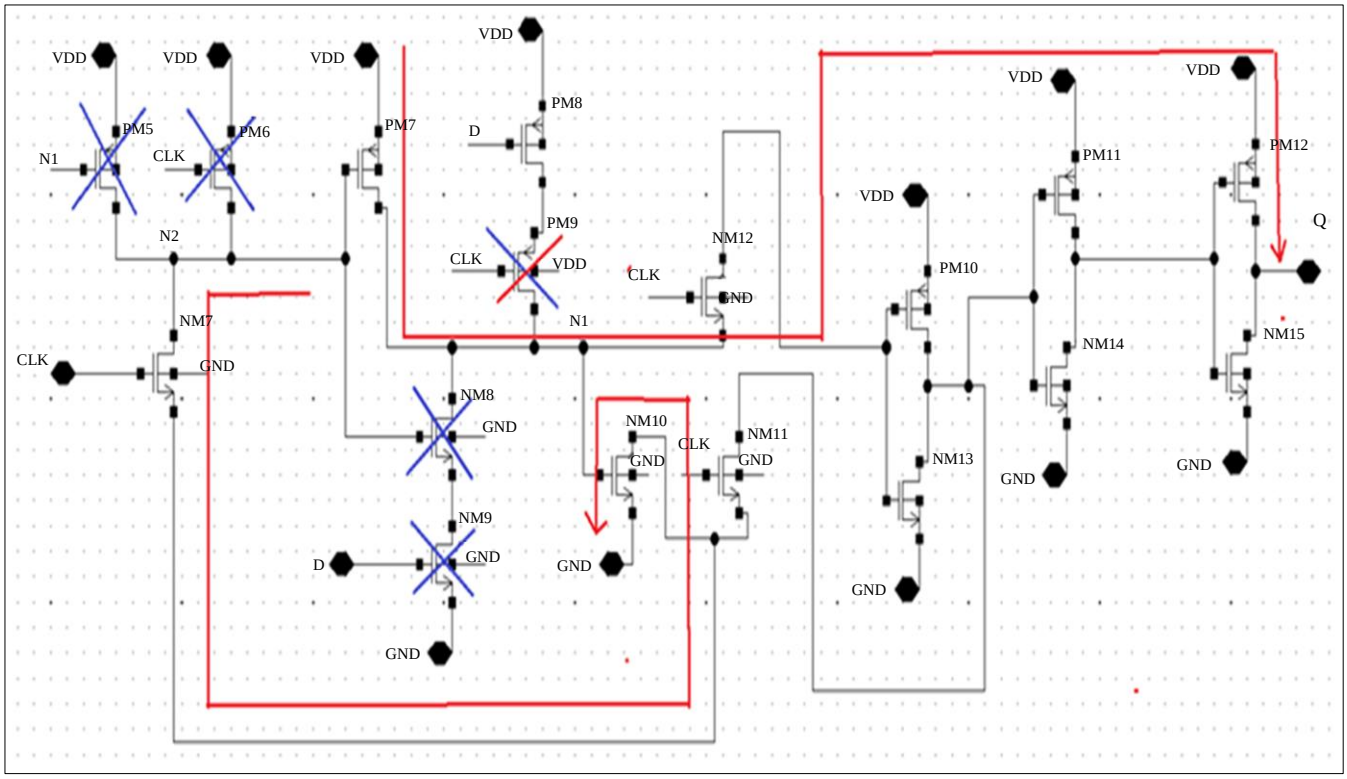

Fig. 8 Operation of proposed FF when CLK=1 & D=0

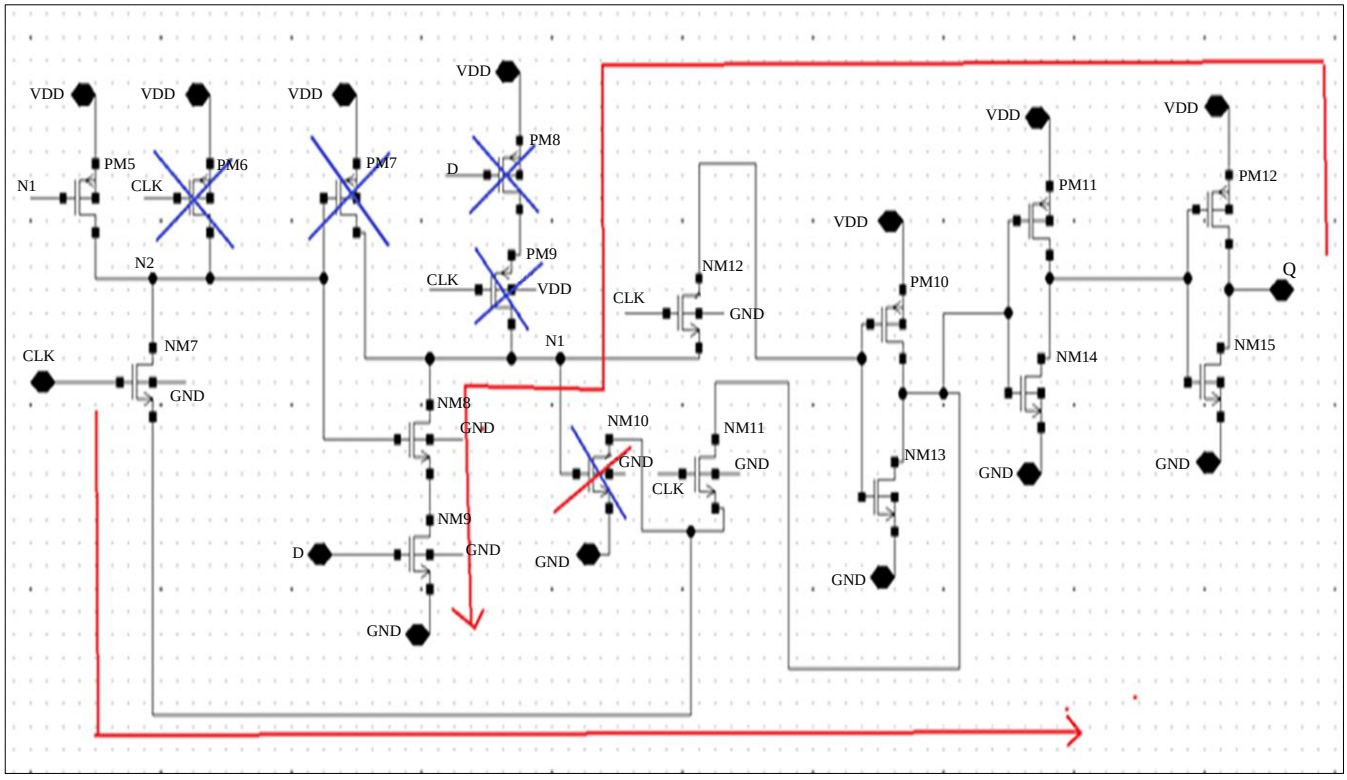

Fig. 9 Operation of proposed FF when CLK=1 & D=1

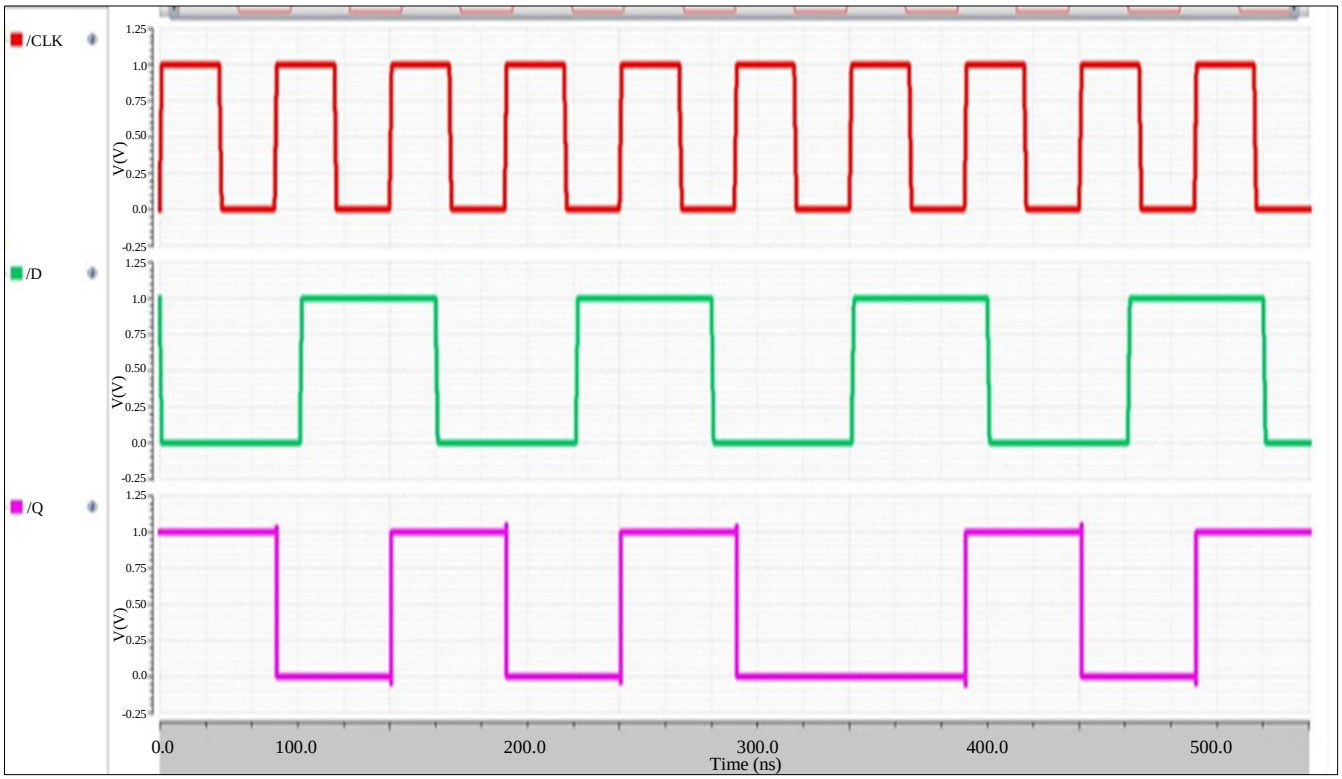

Fig. 10 Transient analysis waveform of proposed FF

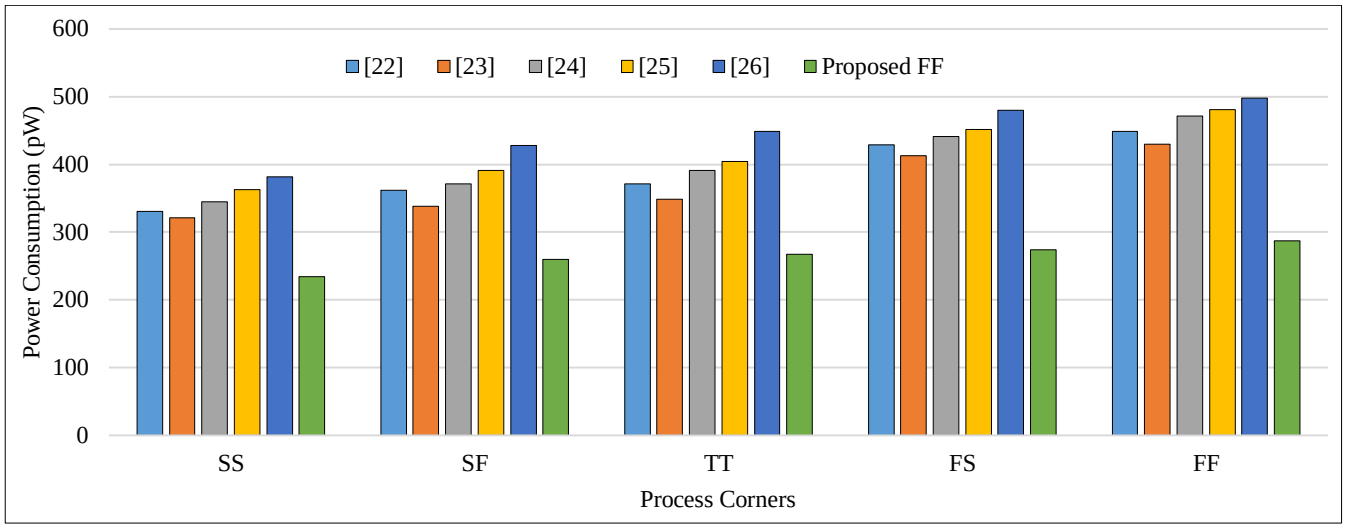

Fig. 11 Power usage of proposed FF w.r.t existing FFs under various process corners

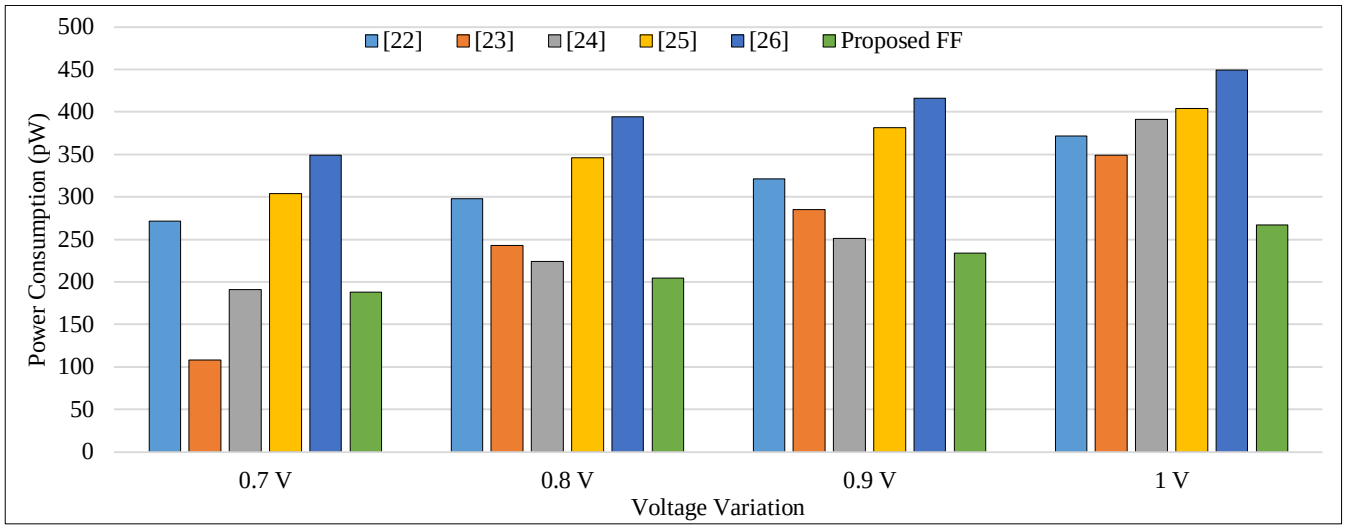

Fig. 12 Power usage of proposed FF w.r.t existing FFs under various supply voltages

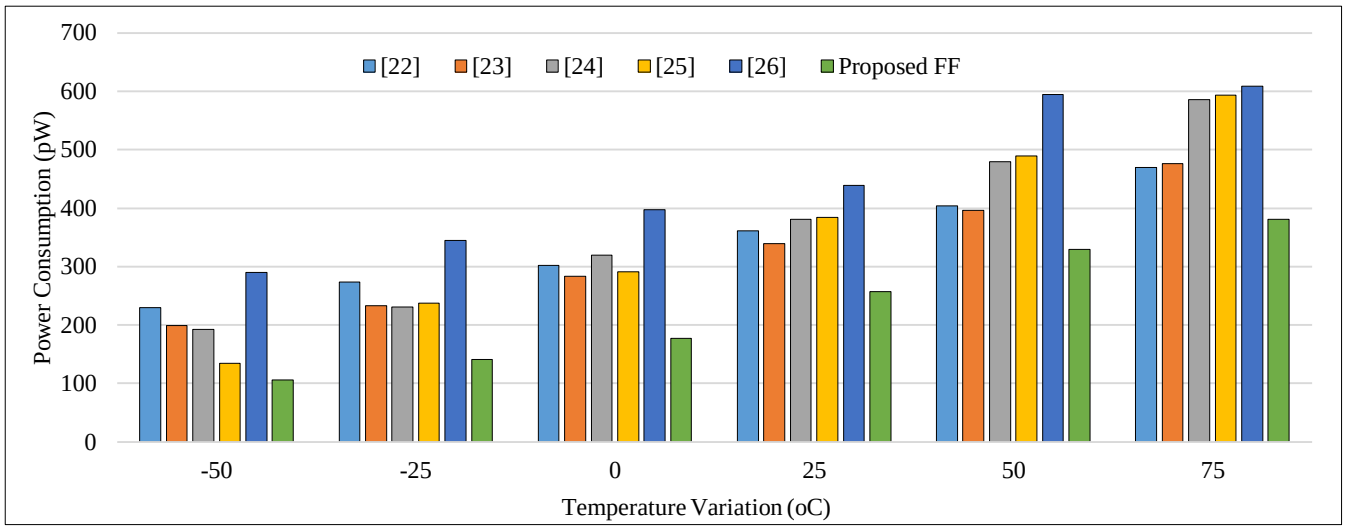

Fig. 13 Power usage of proposed FF w.r.t existing FFs under various temperatures

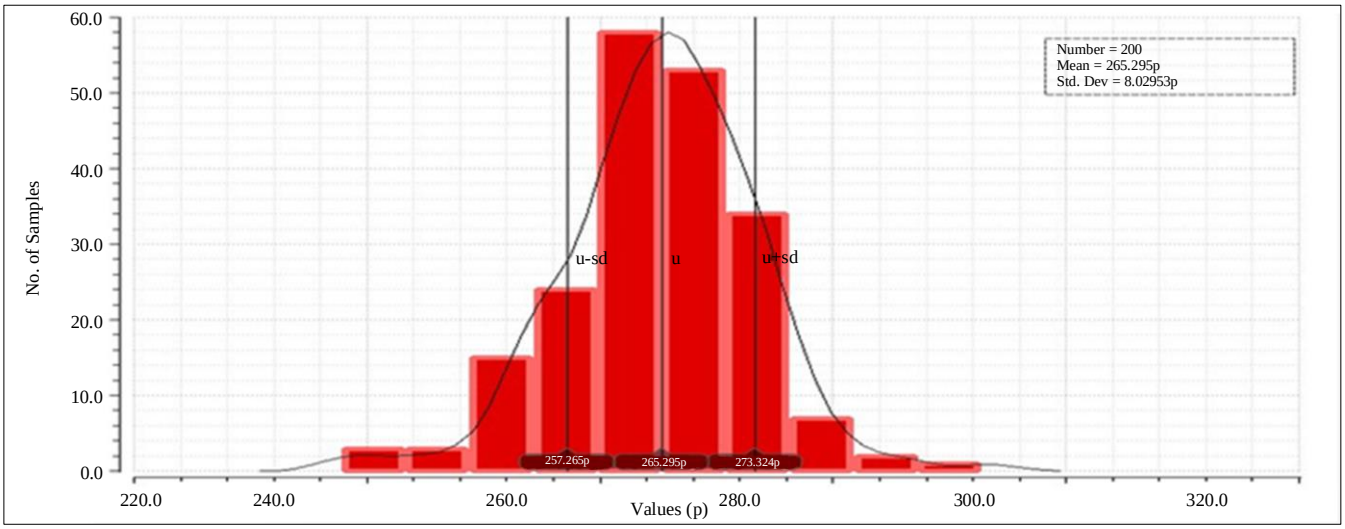

Fig. 14 Monte Carlo analysis of power usage in proposed FF

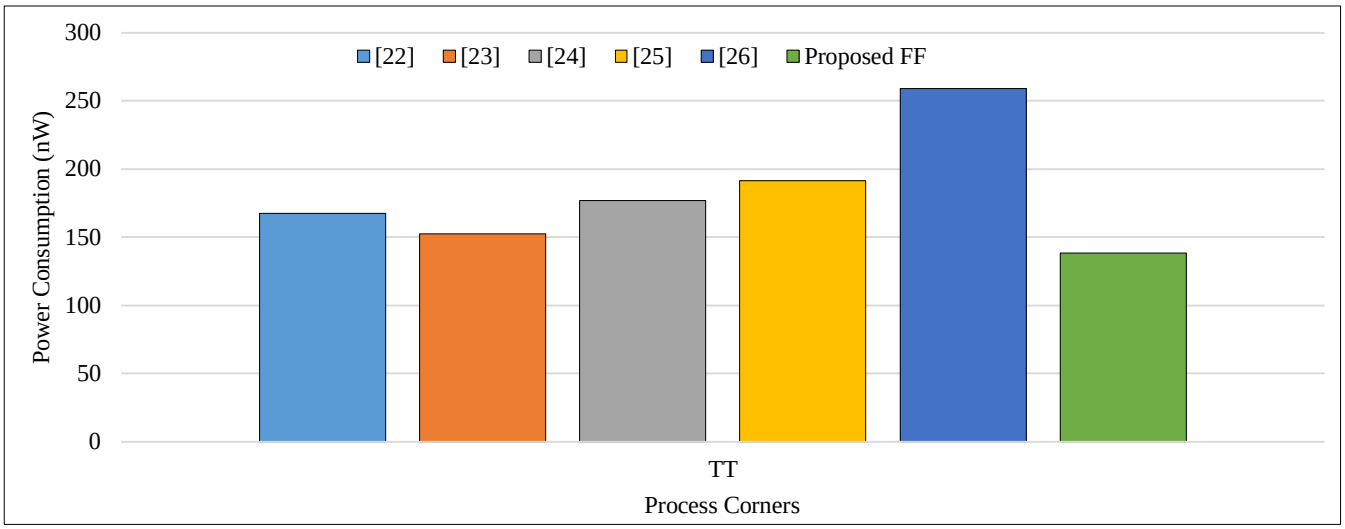

Fig. 15 Leakage power of proposed FF w.r.t existing FFs under various process corners

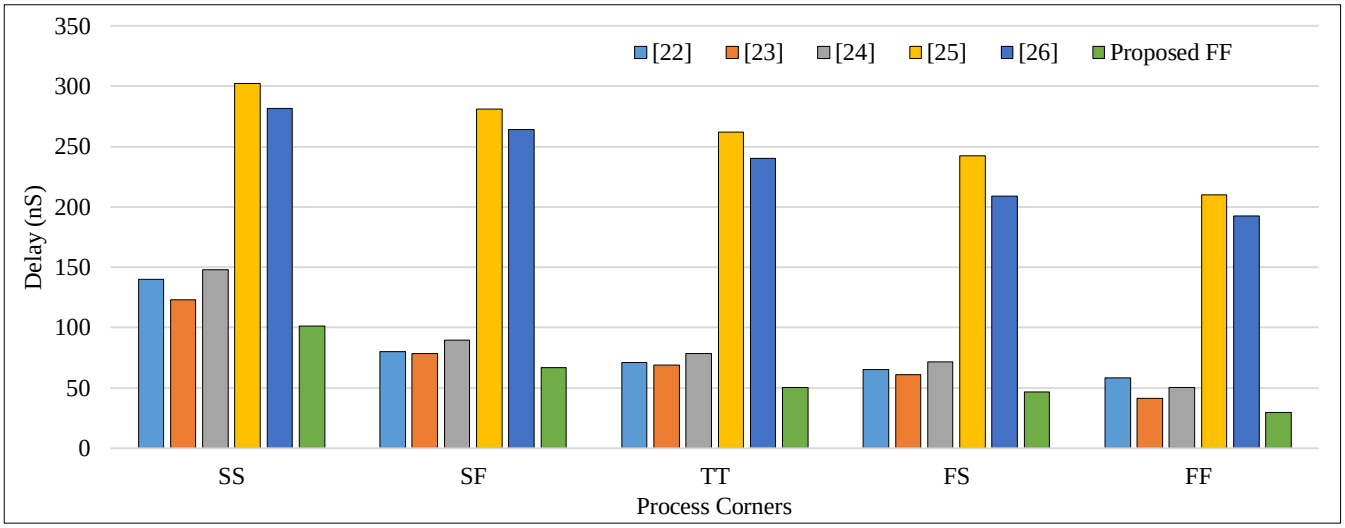

Fig. 16 Delay of proposed FF w.r.t existing FFs under various process corners

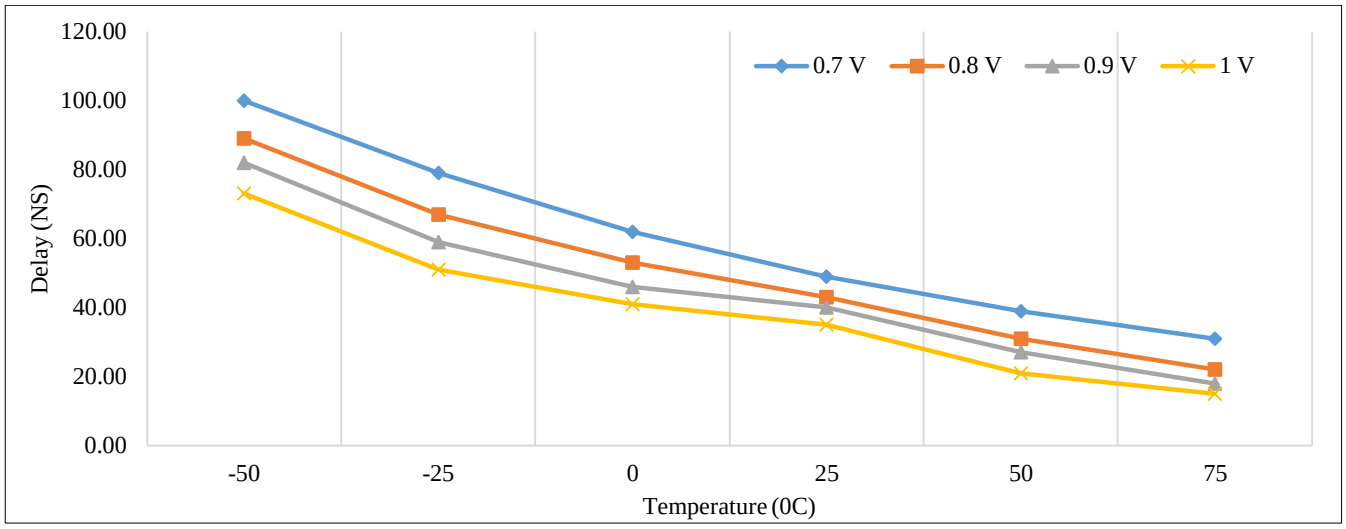

Fig. 17 Delay of proposed FF w.r.t supply voltages and temperatures

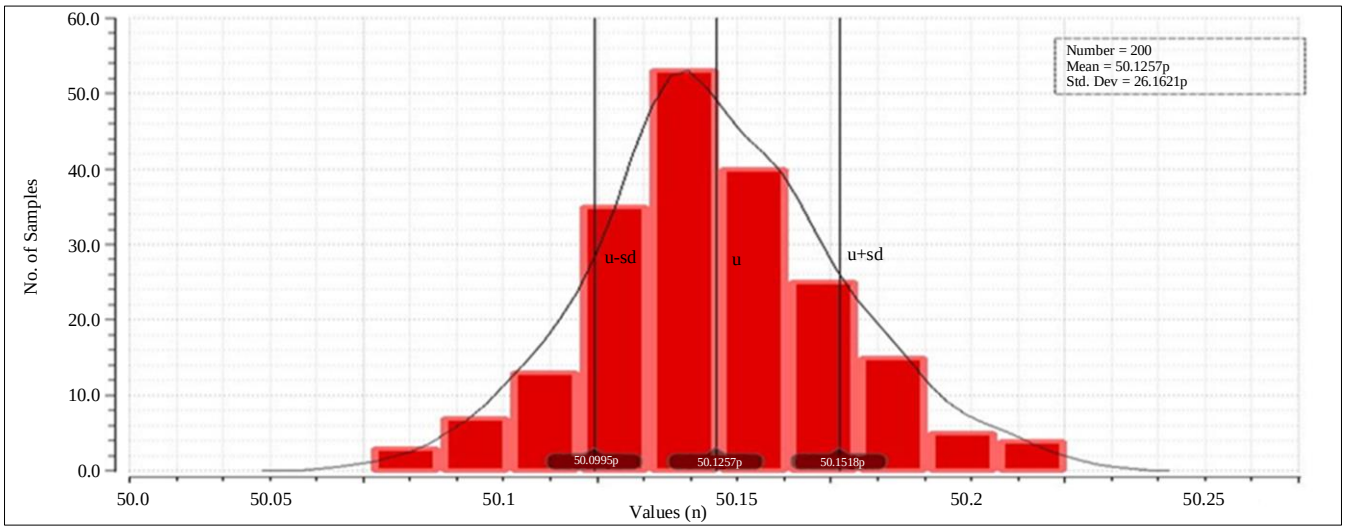

Fig. 18 Monte Carlo analysis of delay in proposed FF

The determination of leakage power has become crucial as master-slave flip-flops frequently operate in idle mode determining leakage power has become critical. Therefore, creating a nanoscale memory with low power leakage has become increasingly challenging. Effectively reducing the current leakage within the suggested flip-flop includes the stacking operation, the use of fewer PMOS transistors, and the lack of clock overload. Figure 15 lowers the leakage power by at least 9.3% when compared to the current flip-flop designs.

This study reduces the clock-to-output (Q) latency in current flip-flop devices. Removing the PMOS devices from the slave circuitry increases the circuit's latency. The proposed work's timing and effectiveness align with VLSI technology requirements. The proposed circuit uses logical techniques to reduce the number of transistors used. It shows improved performance with respect to the latency from the clock signal reaching the output Q. PVT investigates the flip-flop's resilience under various physical conditions. As shown in Figure 16, both the proposed and current flip-flops carry process variations of the delays across all corners.

Figure 16 show that while the proposed flip-flop has fewer PMOS transistors than the conventional designs, it exhibits a shorter clock-to-out node latency in every process corner. This paper assesses, throughout a temperature spectrum of -50 ºC to 75 ºC, the time delay within the clock input and output nodes. We conduct the assessment within the voltage range of 0.7 V to 1.0 V. Figure 17 shows the relevant statistics. The observed PVT fluctuation leads to the conclusion that, within the stipulated range of process voltages, and proposed flip-flop operates appropriately. Functional parameter variations, such as oxide layer alterations, line edge flaws, and probability dopant fluctuations, greatly impact the functionality and efficiencies of devices. To statistically evaluate the suggested flip-flop, we

used a Monte Carlo computer model. Figure 18 shows a Monte Carlo study on the delays encountered during flip-flop operations. The recommended flip-flop cell uses around 10% variation.

5. Conclusion

The researchers presented a high-speed flip-flop with low delay and decreased power utilization without any deviation in reliability or stability. The proposed flip-flop with separate latches indicates that having two different circuits for master and slave latches would be ideal for low-power applications. The proposed low-power, high-speed flip-flop architecture includes 18 transistors. Using fewer PMOS transistors simplifies the proposed design's operation.

The clock signal enters the circuit via a single clock. We realized the proposed designs using 45 nm CMOS technology. The present investigation comprises a PVT analysis to confirm the flip-flop's dependability. When compared to current FFs, the suggested FF consumes at least 9.22% less power, has at least 17.48% less leakage power, and has at least 68.37% shorter clock-to-output delay.

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