

Original Article

Interleaved Parallel Passive Clamping Flyback Photovoltaic Grid-Connected Microinverter

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Abstract - Microinverters for standalone photovoltaic modules can effectively overcome the shading issues present in conventional photovoltaic systems. This study provides a detailed introduction to the topology of an interleaved parallel passive clamping flyback microinverter. The microinverter utilizes LCD passive lossless clamping technology to absorb leakage energy and eliminate voltage spikes. By comparing different clamping topologies, the cost advantages of the proposed passive clamping topology are demonstrated. Moreover, a 400 W microinverter experimental platform is built to verify the correctness of the theoretical analysis and simulation results of this topology structure. The prototype experimental results show that the microinverter can output sinusoidal current with good waveform quality, with a Total Harmonic Distortion (THD) of less than 3% and a full-load maximum efficiency of 94.4%. The system operates stably and reliably.

Keywords - Microinverter, Interleaved flyback topology, Passive clamping, Cost, Experimental platform, MOSFETs.

1. Introduction

In conventional photovoltaic power generation systems, photovoltaic modules are interconnected in series and parallel to form a photovoltaic array, which is then fed into the grid through a centralized inverter. This approach is suitable for large-scale photovoltaic power stations with high system capacity. However, it has limitations such as an inflexible inverter structure, difficulty in system expansion, safety concerns, and the barrel effect, all of which significantly impact the overall system efficiency [1-4]. Microinverters effectively address these issues and have become mainstream in the development of modern photovoltaic systems. Microinverters are directly mounted on the bottom or support structure of photovoltaic modules, converting the DC power output of the photovoltaic modules into AC power and integrating it into the grid. They achieved Maximum Power Point Tracking (MPPT) for each photovoltaic module, improving the overall system efficiency and offering the advantage of plug-and-play functionality. Additionally, through AC output lines, microinverters can facilitate network communication, allowing real-time monitoring of the operational status of each module [5-9].

The flyback inverter has a simple structure, fewer components, and electrical isolation, making it widely used in microinverters [10, 11]. The most important component of the

flyback inverter is the flyback transformer, which has significant leakage inductance due to the air gap and winding process, resulting in a large proportion of losses and significant stress on the main switching device when it is turned off. This not only increases electromagnetic interference but also decreases system efficiency and, in severe cases, can damage the switching devices, rendering the system unable to function properly [12, 13].

Currently, passive soft-switching technologies for handling leakage energy in flyback transformers mainly include RCD clamping circuits [14], Dual-Transistor Clamping Circuits [15], and LCD clamping circuits [16]. For flyback microinverters with RCD clamping circuits, when the main switching device is turned off, the drain-source voltage is clamped by the clamping capacitor, and the leakage energy flows into the clamping circuit, ultimately dissipating in the clamping resistor, resulting in lower system efficiency [17]. Dual-transistor clamping flyback microinverters minimize the voltage stress on the switching devices, ensuring that the stress on each device stays below the input voltage, making them ideal for high-input voltage situations. Additionally, the energy from transformer leakage inductance is efficiently returned to the grid without any loss, resulting in higher system efficiency, although more components are required [18, 19]. LCD passive clamping circuits can return the leakage



energy of the transformer to the grid without any loss and require fewer devices [20]. This research also adopts this LCD passive clamping method.

Typically, interleaved parallel flyback circuits operate independently, with each passive clamping circuit responsible for a single flyback circuit. This results in the redundant use of components, leading to higher hardware costs. Therefore, the existing passive soft-switching technology still requires improvement.

2. Methods

This research focuses on a grid-connected system using a single solar module and proposes a cost-effective interleaved parallel flyback topology with passive clamping soft-switching technology to address the issues of high losses, low efficiency, high switch stress, and component redundancy. An experimental platform is constructed, and both simulation and experimental results confirm the feasibility and stability of the microinverter topology.

2.1. Topology Structure and Operating Principle

The interleaved parallel passive clamping topology proposed in this paper is illustrated in Figure 1. It includes two snubber circuits and one reset circuit, where two flyback circuits share a reset diode D_b , avoiding the redundant use of components.

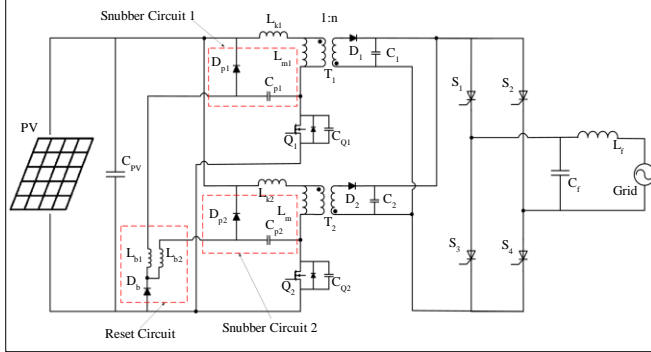


Fig. 1 Schematic representation of the interleaved flyback microinverter topology

The passive clamping working process proposed in this research can be divided into six modes, as depicted in Figure 2, with similar waveforms. PWM is the driving signal of the Metal–Oxide–Semiconductor Field Effect Transistor (MOSFET) Q_1/Q_2 , U_Q is the source-drain voltage of MOSFET Q_1/Q_2 , U_{CP} is the voltage across the snubber capacitor C_{p1}/C_{p2} , and I_p is the primary current of transformer T_1/T_2 .

Taking the operation of the main flyback circuit as an example, the following briefly outlines the operating principle of the circuit during the positive half-cycle of the grid in Discontinuous Conduction Mode (DCM). Figure 3 illustrates the sequential activation of circuit components over time,

from mode 1 (t_0-t_1) through mode 6 (t_5-t_6), highlighting the dynamic changes in voltage and current paths through the snubber capacitor, MOSFETs and other key components. Each state is marked to reflect shifts in electrical characteristics critical for understanding microinverter behavior under operational stress.

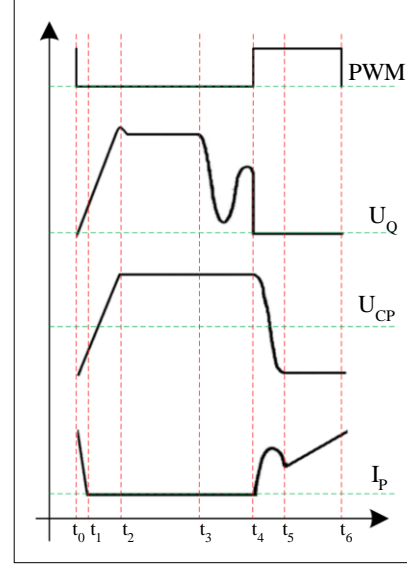


Fig. 2 Working process waveforms of passive clamping

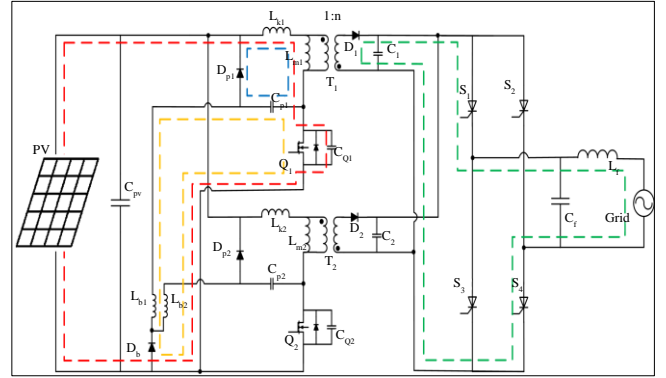


Fig. 3 Operating states of the proposed microinverter

Mode 1 (t_0-t_1): The circuit marked in red in Figure 3 operates; at this time, the voltage direction across the snubber capacitor C_{p1} is positive on the left and negative on the right. The driving signal $PWM1$ of the MOSFET Q_1 is 0, and Q_1 is turned off, thus entering the buffering period. The primary current I_{p1} of the transformer is transferred to the parasitic capacitor C_{Q1} , generating resonance. When I_{p1} decreases, the voltage U_{Q1} across the parasitic capacitor of Q_1 increases.

Mode 2 (t_1-t_2): The circuits marked in red and blue in Figure 3 operate when the voltage U_{Q1} across the parasitic capacitor C_{Q1} rises to the difference between the input voltage and the buffering voltage. The snubber diode D_{p1} conducts and buffering oscillation occurs between the primary side winding

of the transformer and the snubber capacitor C_{p1} . During this time, the voltage across the MOSFET Q_1 does not continue to rise due to clamping. This process continues until the buffering ends, at which time the voltage across the snubber capacitor C_{p1} changes direction to negative on the left and positive on the right.

Mode 3 (t2-t3): The circuits marked in red, blue, and green in Figure 3 all operate. When the voltage across the snubber capacitor C_{p1} increases to the voltage reflected from the output, the flyback rectifier diode D_1 is activated, and the transformer releases energy to the output side.

Mode 4 (t3-t4): The circuits marked in red and blue in Figure 3 operate. When the secondary current I_{s1} drops to zero and the energy release is complete, diode D_1 naturally turns off. At this point, the clamping voltage from the secondary side to the primary side of the transformer disappears. The voltage across MOSFET Q_1 undergoes significant changes, causing fluctuations in the drain-source voltage and leading to a large magnitude of resonance.

Mode 5 (t4-t5): The circuits marked in red and orange in Figure 3 operate. To ensure that the snubber capacitor C_{p1} functions in the next switching cycle, it needs to be completely discharged to reset. Upon the start of the reset, MOSFET Q_1 conducts, and the snubber capacitor C_{p1} discharges through MOSFET Q_1 , reset inductor L_{b1} , and reset diode D_b . Through energy exchange in the LC resonance, when the current flowing through the reset inductor L_{b1} returns to zero, the voltage direction across the snubber capacitor C_{p1} reverses, and the reset process ends.

Mode 6 (t5-t6): Only the circuit marked in red in Figure 3 operates. The primary current I_{p1} of the transformer increases, and the energy stored in the transformer increases until the MOSFET Q_1 is turned off, completing one cycle.

The interleaved flyback microinverter topology is essentially an interleaved combination of two single-ended flyback converters. The operating principle and design parameters of each flyback converter circuit are the same as those of the single-ended flyback topology. The control algorithms for both are essentially the same, except that the control signal for one of them is delayed by half a switching cycle relative to the other.

To reduce losses in microinverters and extend the lifespan of components, only the main circuit is driven to operate for flyback when the grid phase is low. When the output power reaches 90 W, as set by the program, the auxiliary circuit also begins to operate. The design parameters for the interleaved microinverter are listed in Table. The key component selection of the microinverter is shown in Table 1.

2.2. Fabrication of the Experimental Platform

The system functional block diagram of the experimental platform is shown in Figure 4. A Digital Signal Processor (DSP) collects the voltage and current signals of a photovoltaic module, grid voltage and current signals, grid voltage and zero-crossing signals, and grid-connected current signals. These signals are processed by the software programs of the Central Processing Unit (CPU) to control the drive circuits that output Pulse-Width Modulation (PWM) signals to the main circuit, thereby achieving flyback, inversion, and grid connection functions.

Table 1. Key parameters of the interleaved parallel passive clamp flyback topology

Parameter	Value	Unit
DC input voltage U_{pv}	25-55	V
Effective value of output voltage U_{gp}	220	V
Output voltage frequency f_{gp}	50	Hz
Rated output power P	400	W
Maximum switching frequency f_{max}	300	kHz
Ratio of transformer n_1, n_2	2:12	-
Output filter capacitors C_1, C_2	10n	F
Snubber capacitors C_{p1}, C_{p2}	45n	F
Reset inductor L_{b1}, L_{b2}	33n	H
Excitation inductors L_{m1}, L_{m2}	3.4u	H
Leakage inductors L_{k1}, L_{k2}	34.22n	H
Parasitic capacitors C_{Q1}, C_{Q2}	321.5p	F

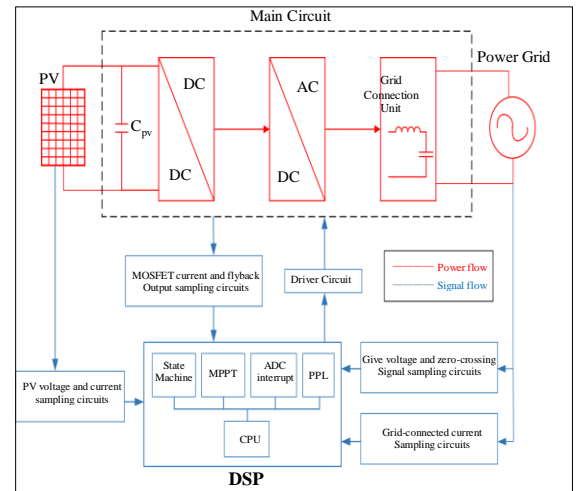


Fig. 4 System diagram of the experimental platform

Table 2. Key component selection of the microinverter

Key Component	Component Selection	Function
S_1 - S_4	HSB80R240K2	Inverter circuit
Q_1/Q_2	HGN099N15S	Flyback input side
$D_{p1}/D_{p2}/D_b$	UG3GB	Clamping circuit
D_1/D_2	MSD02120G1	Flyback output side

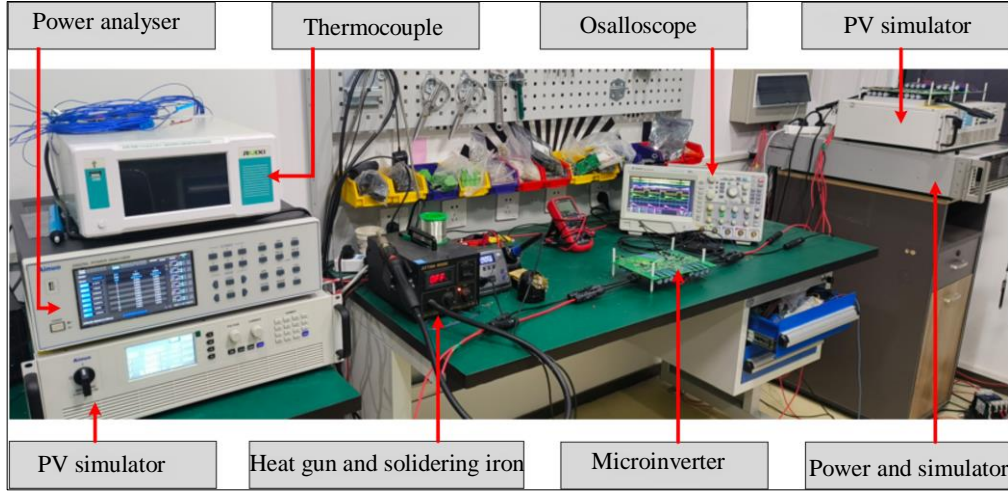


Fig. 5 Experimental setup for microinverter performance validation

Figure 5 shows the experimental setup for micro-inverter performance validation, which includes the microinverter prototype used in this experiment, a power analyser for measuring power, efficiency, and detecting power consumption, a thermocouple for temperature measurement, an oscilloscope for displaying various waveforms, a photovoltaic simulator for simulating photovoltaic module voltage-current curves, a heat gun and a soldering iron for soldering components, and a power grid simulator for simulating grid output, meeting the experimental requirements.

3. Results and Discussion

3.1. Simulation Validation

To verify the effectiveness of the single-ended passive clamping flyback topology, the entire system model was simulated and validated in PSIM software.

3.1.1. Waveform Analysis of the Clamping Circuit

Figure 6 presents several key waveforms of the main flyback circuit in the passive clamping topology. $PWM1$ is the driving signal of MOSFET Q_1 , U_Q is the drain-source voltage of Q_1 , U_{Cp1} is the voltage of the snubber capacitor C_{p1} , and I_{P1} is the primary current of the transformer. The figure annotates six modes within one switching cycle. Modes 1 and 2 represent the buffering stage, where the driving signal $PWM1$ of MOSFET Q_1 is off, and the voltage across Q_1 and snubber capacitor C_{p1} continues to rise until U_{Cp1} reaches the voltage

reflected to the primary side of the transformer from the output voltage.

Modes 3 and 4 correspond to the energy release stage, during which the flyback rectifier diode D_1 conducts, transferring energy from the primary side to the secondary side for output. Modes 5 and 6 are the reset stage, where $PWM1$ is on, and the snubber capacitor C_{p1} is fully discharged to achieve reset while the primary current I_{P1} rises, increasing stored energy. The simulation results are consistent with the theoretical mode analysis.

Furthermore, the effectiveness of the passive clamping circuit was verified. The drain-source voltage waveforms of MOSFET Q_1/Q_2 before and after the addition of the passive clamping circuit in the same phase of the power grid are compared. As shown in Figure 7, Figure 7 (a) illustrates the drain-source voltage waveform without the added clamping circuit, while Figure 7 (b) represents the drain-source voltage waveform with the clamping circuit added.

When Q_1/Q_2 is off, the drain-source voltages of both topologies fluctuate at approximately 90 V. Without the passive clamping circuit, the voltage spike of Q_1/Q_2 reaches 112 V. After adding the passive clamping circuit, at the same power and voltage level, due to the resonant effect of the clamping circuit, there is absorption and feedback of leakage inductance, reducing the voltage spike of MOSFET Q_1/Q_2 to 101 V, a decrease of 9.8%.

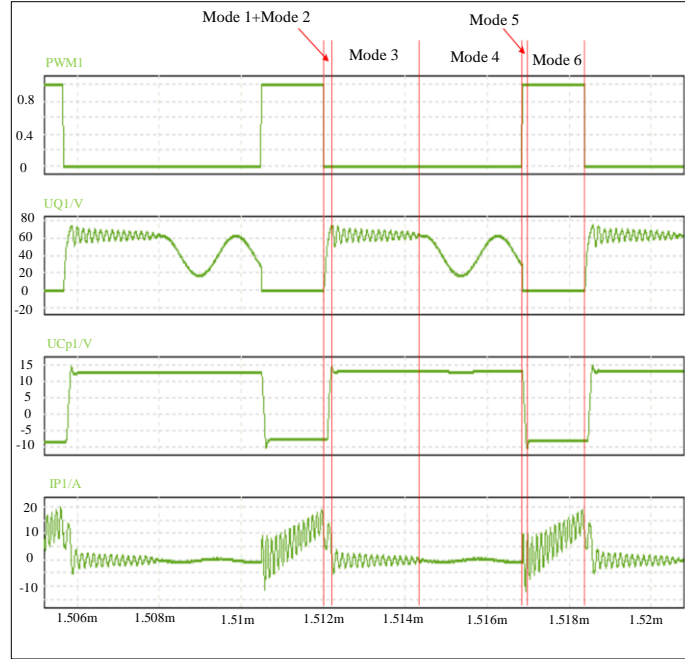
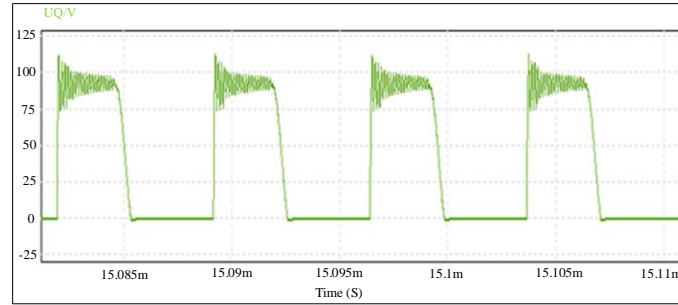
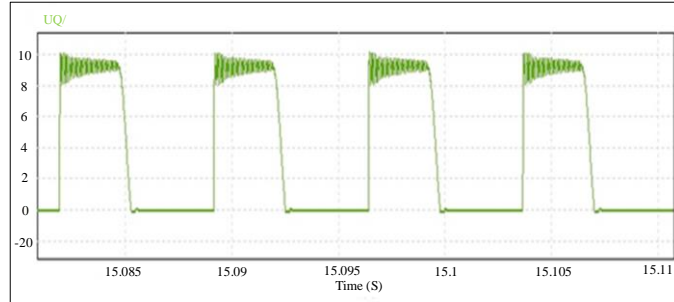


Fig. 6 Key waveforms of the main flyback circuit



(a)



(b)

Fig. 7 Comparison of the drain-source voltage waveforms with and without the clamping circuit (a) Drain-source voltage waveform of MOSFET without the clamping circuit, and (b) Drain-source voltage waveform of MOSFET with the clamping circuit.

3.1.2. Waveform Analysis of the Flyback Circuit and Grid Connection Circuit

Figure 8 presents several key waveforms of the interleaved flyback topology, including the driving signals $PWM1$ and $PWM2$ of the main and auxiliary circuits, the drain-source voltages U_{Q1} and U_{Q2} of the main MOSFET Q_1 and the auxiliary MOSFET Q_2 , and the primary currents I_{p1} and I_{p2} through the main circuit and the auxiliary circuit. When

the grid phase is low, only the signal $PWM1$ drives MOSFET Q_1 , and the main circuit operates. Once the output power reaches a certain level, the signal $PWM2$ drives MOSFET Q_2 , and the auxiliary circuit starts to operate. The MOSFETs Q_1 and Q_2 of the main and auxiliary circuits alternate on and off, with a switching frequency twice that of the single-ended flyback topology, effectively expanding the power level of the flyback circuit and enhancing its capacity. Under the condition

of using the same power level of photovoltaic cells and the same main switching frequency, the interleaved flyback circuit, compared to the single-ended flyback circuit, has twice the equivalent switch frequency.

This results in smaller input and output ripples, as well as a smaller volume for the input and output filters. Figure 9 shows the grid voltage and grid-connected current waveforms of the interleaved flyback topology.

Similarly, the current signal is amplified by 50 times. The peak value of the grid-connected current is 2.46 A, approximately twice that of the single-ended flyback topology. After FFT analysis, the THD was found to be 2.11%. Compared to the 3.02% THD obtained from the same

passive clamping single-ended flyback topology, the waveform is smoother, reducing the harmonic content by 0.91%.

3.1.3. Cost Comparison and Analysis

Table 3 lists the number of components used in the DC-DC flyback circuit with different clamping technologies for interleaved flyback topologies.

The diode, capacitor, inductor, and resistor used in the flyback unit have similar prices, while the price of the MOSFET is several times greater than that of these four components. By comparison, the improved LCD passive clamping circuit proposed in this research has the lowest component cost.

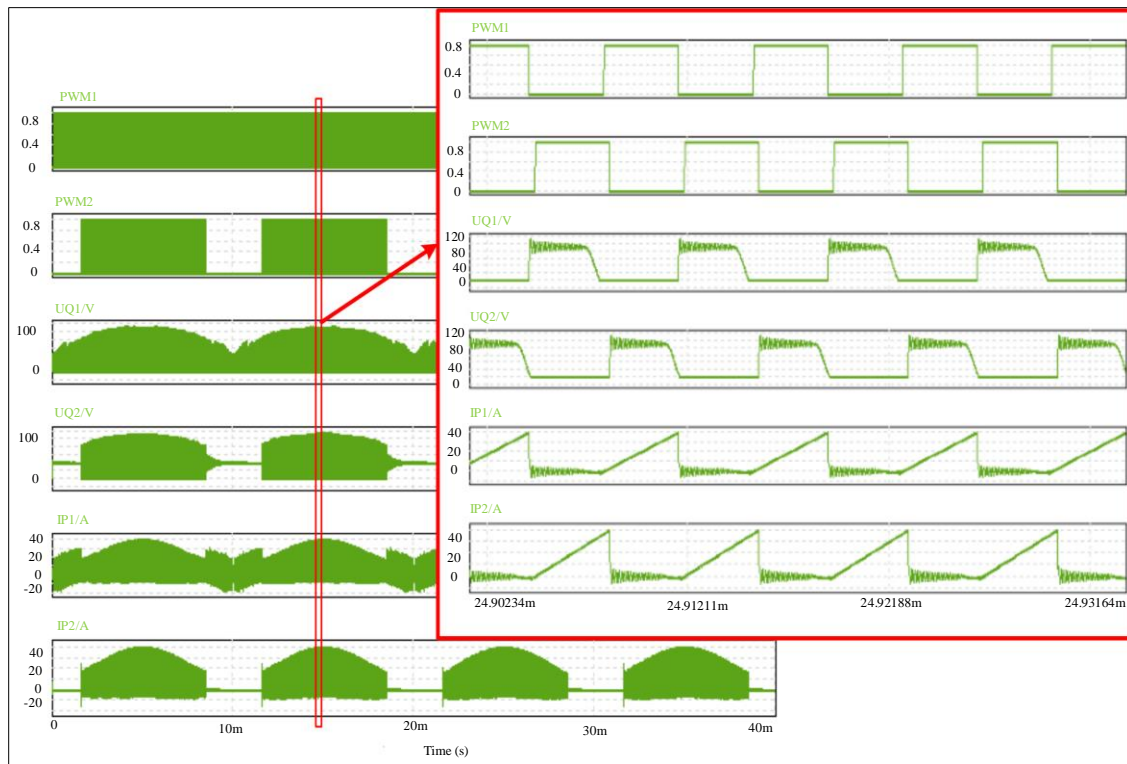


Fig. 8 Key waveforms of the interleaved passive clamping flyback topology

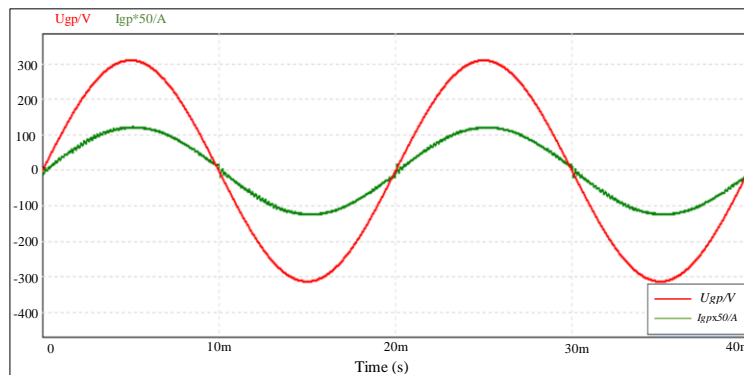


Fig. 9 Waveforms of the grid voltage and grid-connected current of the interleaved flyback topology

Table 3. ElementNum comparison of different interleaved clamping topologies

Clamping Technology	ElementNum				
	Transistor	Diode	Capacitor	Inductor	Resistor
This Research	2	3	2	2	0
PMOS Active Clamping [21]	4	0	2	0	0
NMOS Active Clamping [22]	4	0	2	2	0
RCD Passive Clamping [14]	4	2	2	0	2
LCD Passive Clamping [16]	2	4	2	2	0
Dual-Transistor Passive Clamping [23]	4	2	0	0	0

3.2. Experimental Validation

Figure 10 shows the waveforms of the driving signals and primary currents. CH1 is the driving signal $PWM1$ of the main flyback circuit, CH2 is the driving signal $PWM2$ of the auxiliary flyback circuit, CH3 is the primary current of I_{p1} of the main flyback circuit, and CH4 is the primary current of I_{p2} of the auxiliary flyback circuit. The driving signals of the main flyback circuit and auxiliary flyback circuit have a phase angle difference of 180° , which reduces the current ripple. In the case of a low AC voltage, considering loss issues, both circuits do not have to work simultaneously.

Therefore, the main flyback circuit operates with full-phase wave emission, while the auxiliary flyback circuit starts operating only after reaching the programmed 90 W power level, effectively improving operational efficiency.

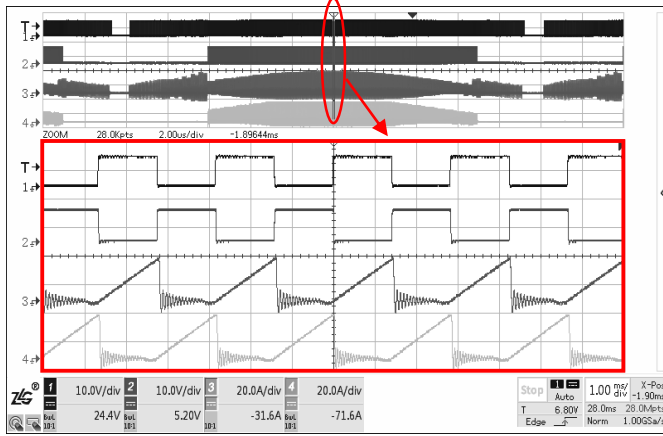


Fig. 10 Waveforms of the driving signals and primary currents

Figure 11 shows the grid voltage and grid-connected current waveforms corresponding to the primary currents. CH1 is the primary current of I_{p1} of the main flyback circuit, CH2 is the primary current of I_{p2} of the auxiliary flyback circuit, CH3 is the grid voltage U_{gp} , and CH4 is the grid-connected current I_{gp} . The experimental waveforms completely match the simulated waveforms. The grid-connected current I_{gp} is in phase and frequency with the grid voltage U_{gp} , and the waveform I_{gp} is of high quality, with the output power factor basically reaching 1, achieving good inverter output performance.

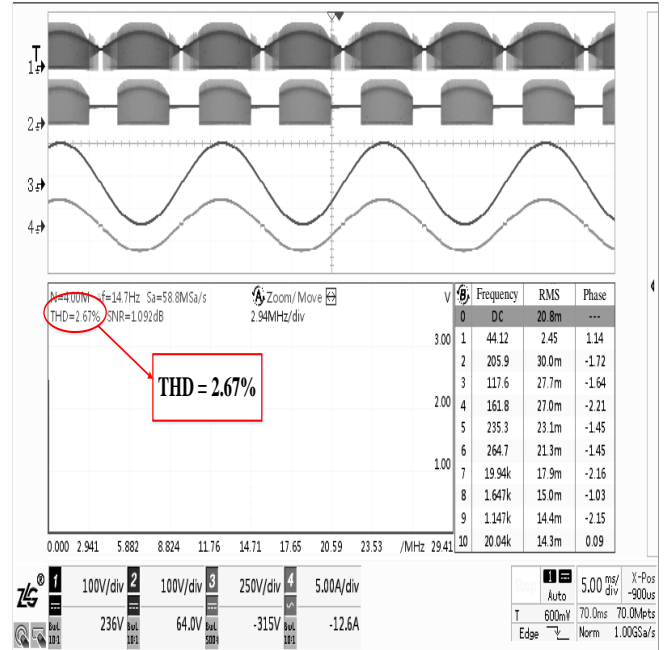


Fig. 11 Waveforms of the grid voltage and grid-connected current

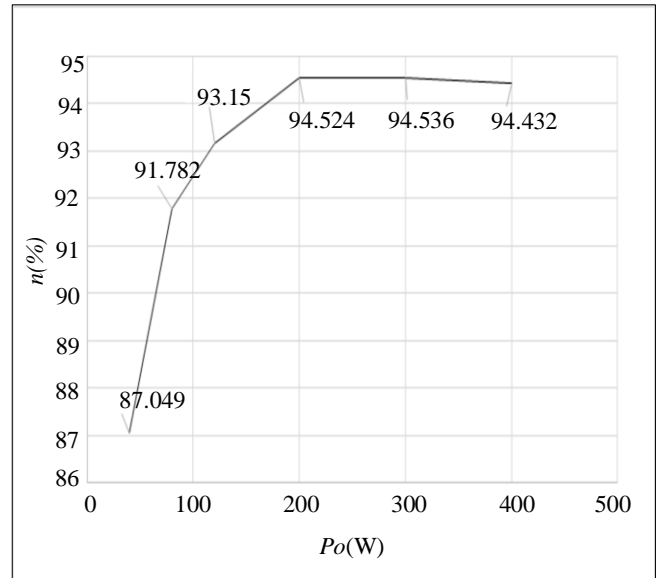


Fig. 12 Power curve

Simultaneously, Figure 11 shows the THD of the grid-connected current as 2.67%, complying with the international requirement for harmonic content of grid-connected current (IEC 62109-1 International Standard is below 5%), thus indicating that the proposed interleaved parallel passive clamping flyback topology can effectively control harmonic content and ensure undistorted grid-connected current. Using a power analyser, the efficiency curve of the microinverter prototype was measured, as shown in Figure 12, where P_o is the output power and η is the efficiency. This further demonstrates that the microinverter achieves high efficiency throughout the entire load range, with a maximum efficiency of 94.4% at full load.

4. Conclusion

This paper proposed a topology for an interleaved parallel passive clamping flyback microinverter, introduced passive lossless clamping technology, eliminated the voltage spikes generated between the high-frequency transformer leakage inductance and the parasitic capacitor of the main switching

transistor, reduced the switching losses, and improved the inverter efficiency. Compared to the single-ended topology, the interleaved flyback topology makes the grid-connected current smoother, reducing the harmonic content by 0.91%. By comparing different clamping topologies, it was concluded that the proposed LCD passive clamping topology has cost advantages.

Finally, experimental validation of the microinverter was conducted. The waveforms of the flyback circuit and grid-connected circuit were analysed, which matched the simulation results. The efficiency curve and THD were also measured, with a full-load maximum efficiency reaching 94.4% and a THD of 2.67%. This validated the stability of the microinverter's grid-connected operation.

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