SSRG International Journal of Electrical and Electronics Engineering
ISSN: 2348-8379/ https://doi.org/10.14445/23488379/IJEEE-V11I7P127

Volume 11 Issue 7, 302-311, July 2024

Original Article

Robust and Improvised Enhanced Phase Lock Loop Structure for its Application with Electric Spring

Mehul Dansinh Solanki[1], Satish K. Joshi[2]

[1]*Department of Electrical Engineering, Shantilal Shah Engineering College, Gujarat, India.*
[2]*Department of Electrical Engineering, Faculty of Technology and Engineering, The MSU of Baroda, Gujarat, India.*

[1]*Correspondig Author : solankimehuld@gmail.com*

Received: 13 May 2024 Revised: 15 June 2024 Accepted: 12 July 2024 Published: 26 July 2024

Abstract - *Phase-Locked Loops (PLL) are an integral part of grid-tied Power Frequency Applications (PFA) and play a crucial role in their proper operation and control. This work proposes an update in the available Enhanced Phase Lock Loop structure (E-PLL) by introducing an adaptive integral gain, which adapts a value depending on the error that it processes to give it more robustness. The basic function of PLLs for PFA is to synchronize the apparatus with the grid's phase, and additionally, it may function as an orthogonal function generator, may deduce phase angle, and may give out harmonic free pure sinusoidal signal perfectly in tandem with the input. An Electrical Spring (ES) is a grid connected Voltage Source Inverter (VSI) acting in tandem with the noncritical load of a consumer and provides voltage regulation to critical loads. Synchronization of the converter (ES) with the grid parameter is a must, and hence a PLL, for the grid connected inverters. Further, ES is required to function amidst dynamically challenging conditions, viz., sag, swell, transients, under voltages, unbalance, and in the presence of harmonics. PLL is crucial to ES's proper functioning and must stand robust against the mentioned odds and provide synchronization with the greatest possible speed and accuracy. To demonstrate the might of the proposed Improvised Enhanced PLL structure (IE-PLL) as an ancillary component of ES, its performance has been compared with that of another robust PLL structure employing a Second Order Generalized Integrator (SOGI).*

Keywords - *Electric spring, PLL, Synchronous reference frame, Second order generalized integrator, Voltage regulation.*

1. Introduction

In 1923, Appleton devised a primitive Phase Lock Loop (PLL) for synchronizing noise-free and stable high-frequency radio signals, having a phase detector and a Voltage Controlled Oscillator (VCO). This PLL might not be the best fit for Power Frequency Applications (PFA) as harmonics and notches may have molested it and are prone to frequency alterations, albeit in a strict bend (±0.5%), due to concurrent alterations in load and generation.

Emerging technologies, viz., Custom Power Devices (CPDs), Flexible AC Transmission Systems (FACTS), grid-tied inverters, Uninterrupted Power Supply (UPS), Active Power Filters (APFs), Phasor Measurement Units (PMU), have substantially elevated the quantum of research in the field of PLL, for the reason that these devices/technologies required grid synchronization.

These PFAs are nothing but converters with power electronics switches operating at very switching rates, intrinsically nonlinear, and necessitate system analysis in a likewise manner, and the same is the case with the PLLs used in conjunction with them. It must be robust enough to withstand frequency fluctuations, distortion, load fluctuations, and noise.

These factors have led to advances in research of PLLs used with PFAs, of which few have been reviewed here. PLL using a zero-crossing detector [1] is the most acclaimed one due to its ease of implementation, but it lacks accuracy and robustness in a harmonically molested and noisy environment. Poor robustness is an issue with PLLs using Fourier Transforms (FT) or their enhanced variants (DFT, FFT) due to spectral leakage [2].

Phasor Rotation-based algorithm [2], despite its great robustness, suffers the drawback of large window length. PLLs operating with the algorithm of Kalman filter [3] ask for an accurate system model and hence lose their resilience due to the perturbing model parameters. PLLs with the Least Square Fit approach [4] garbles when the system exhibits singularity. Poor sensitivity threshold for noise is an issue with Demodulation based methods [5]. The adaptive notch filters

[6], Newton-type algorithm [7], and various signal processing approaches are numerically arduous and involved in terms of their implementation. ANN-based techniques [8] can perform well when dealing with noisy or contaminated inputs, but they need a large amount of training time and computing effort and are difficult to deal with. The flaws, as mentioned earlier, of the reviewed PLLs for PFAs, led to the emergence of new PLL structures wiz., Enhanced PLL (E-PLL), and PLL with SOGI.

ES is to be commissioned in the distribution system to execute the regulation of voltage across critical loads of a consumer, with a reduced voltage on the DC side of the converter, as compared to UPS, by getting the support of dissipative (tolerant to fluctuating voltage profile) non-critical load. An ES is to provide voltage regulation amidst,

- Dynamically changing loads, which introduce dynamics in the form of transients (sag, swell) and dynamic variation in the voltage
- A gross mismatch between demand and supply leads to frequency change
- Harmonics, due to non-linear loads, and
- Phase angle variation, due to changes in power factor as a result of changing load type.

The PLL for ES is to furnish a precise phase at all the sampled instances amidst all these perturbating conditions in the shortest possible time and with the least ramp-up time at the start-up. A careful review of the available literature on ES reveals the lack of a systematically designed PLL structure that could be used with the grid-tied application of ES having robustness against perturbing load and grid conditions and is fast enough to provide a distortion-free synchronizing signal with unity amplitude and zero startup time lag.

These identified gaps have been addressed in this work by proposing a systemic approach to PLL design in the form of a SOGI-PLL using a Lead compensator and an improvised version of an E-PLL structure called IE-PLL that could possess blazing speed and work perfectly in the presence of harmonics, and also robust enough to be synchronized with the given input in the perturbing grid and load conditions. Looking at the stringent requirements of ES and enumerated flaws of the various PLL structures, the results of three different PLL structures have been compared, to evaluate and identify the best fit of ES.

This work is organized into the following sections: a testbed for ES for testing of PLL against the strenuous grid conditions, an introduction to three different PLL structures for ES and associated design philosophies, a comparative analysis of the results amidst harmonics and dynamically changing grid conditions, performance analysis of proposed IE-PLL for the application of ES.

2. Conceptualization and Characterization of Testbed for the PLL

An ideal PLL structure that is to be used with ES must possess sufficient robustness to avert the adverse impact of dynamics, transients, phase jumps, harmonics, and frequency variations. A PLL structure could be considered robust if it could attain stability instantaneously against the mentioned odds. A testbed has been conceptualized to justify the performance of PLL being used with ES if it could synchronize the controller's output with that of its input signal in the wake of:

- Perturbations in grid voltage (220V±20%), i.e., 176V to 264V.
- Change in the phase from 0^o to 90^o due to a possible change in the type of connected load (R-L-C) or possibly some of its combination.
- Variation in frequency from 47Hz to 53Hz, which might be a possibility in the case of micro-grid application of ES.
- Harmonics (most dominant ones for a single phase (1-φ) system of ES) of the order of 3^{rd} and 5^{th}, having a magnitude of one-third and one-fifth of the fundamental signal.

A testbed incorporating the conditions mentioned above has been established for the sake of testing the robustness of the PLL to be used with ES. As can be seen from Figure 1, the testbed could inflict the step variation in phase, magnitude, and frequency and could introduce harmonics to a signal, as evident from Table 2.

3. PLLs for ES

Detailed result analysis of the following PLL structures, namely,

(1) Time period/3 delay PLL,
(2) SOGI-PLL [10] being controlled using a Lead compensator [11], and
(3) Improvised E-PLL [12] called IE-PLL

has been presented for evaluation of accuracy, robustness, and speed in the presence of dynamic changes that an ES is subjected to.

3.1. Time Period / 3 Delay-PLL

A Time period/3-Delay PLL is the most elementary structure devised to get started with. The phase (ϕ) of the signal to be synchronized has been identified through Clarke's transformation. The formulation of 3-phases (x,y,z) from a single available phase (x) is accomplished by applying consecutive one-third time delay to the time period (of a cycle of 20ms) to x and y, respectively.

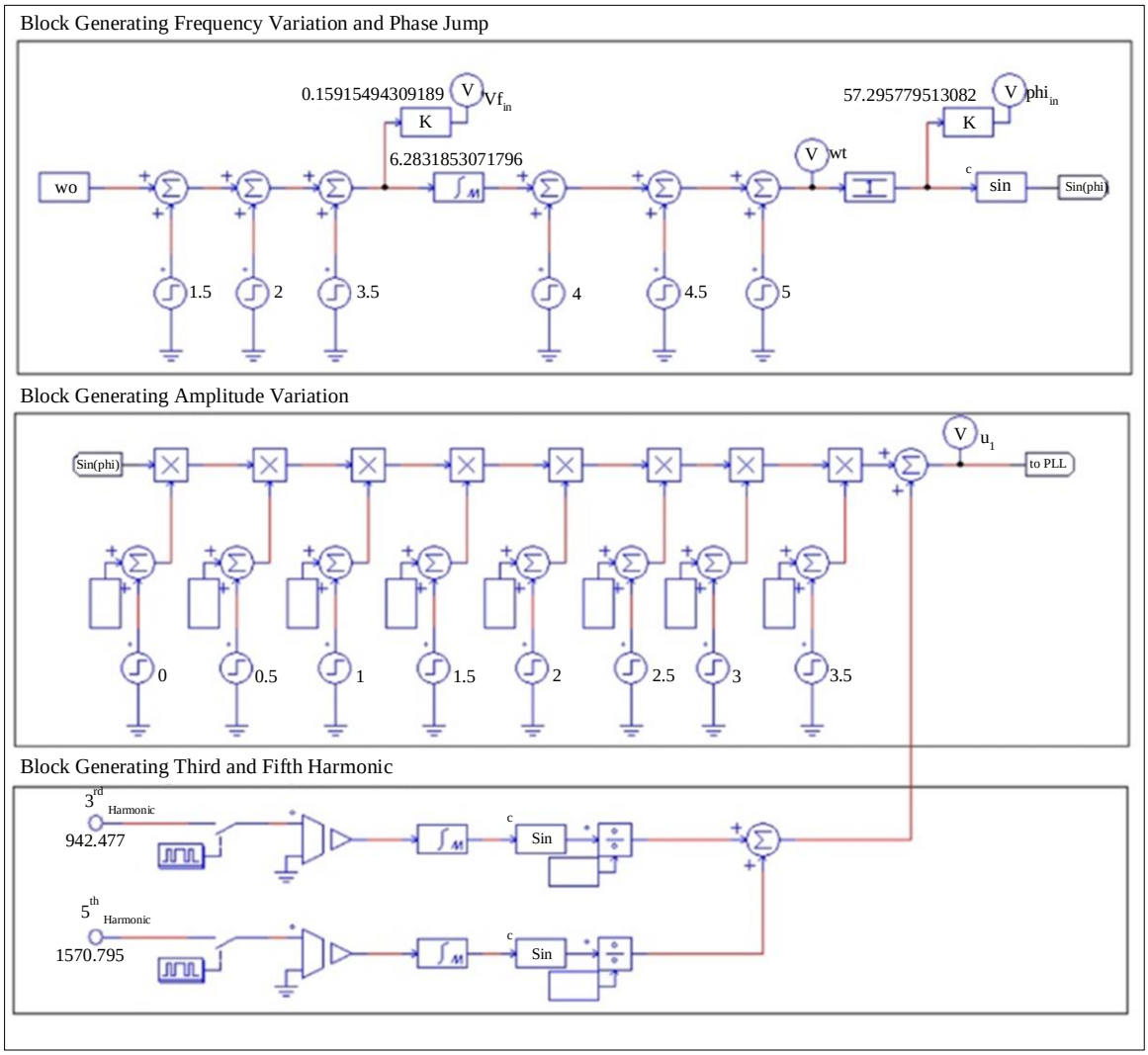


Fig. 1 Test setup for PLL

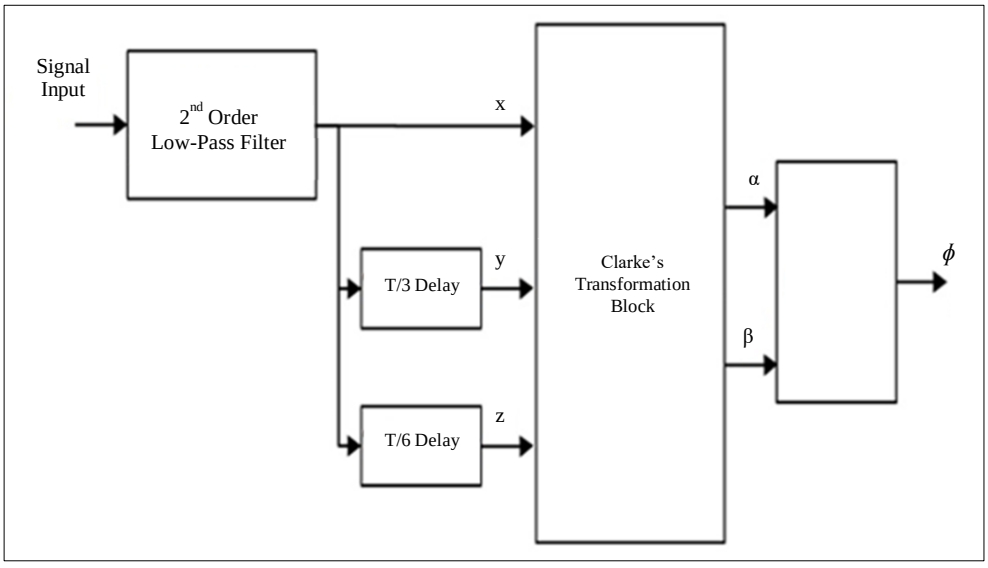


Fig. 2 Time Period/3 - PLL

This *3-φ* quantity is converted into *2-φ* quantity (*α-β*) in the stationary reference frame. Figure 2 depicts the overall structure of this PLL. Here, ϕ is,

$$\phi = tan^{-1}\left(\frac{\beta}{\alpha}\right) \quad (1)$$

Figure 3 reveals that this PLL works fine with phase jumps, harmonics, and amplitude variation (Figures 3(a), and (b)) as it catches up with these changes in just two cycles (40ms) but fails miserably in the presence of frequency change (Figure 3(c)).

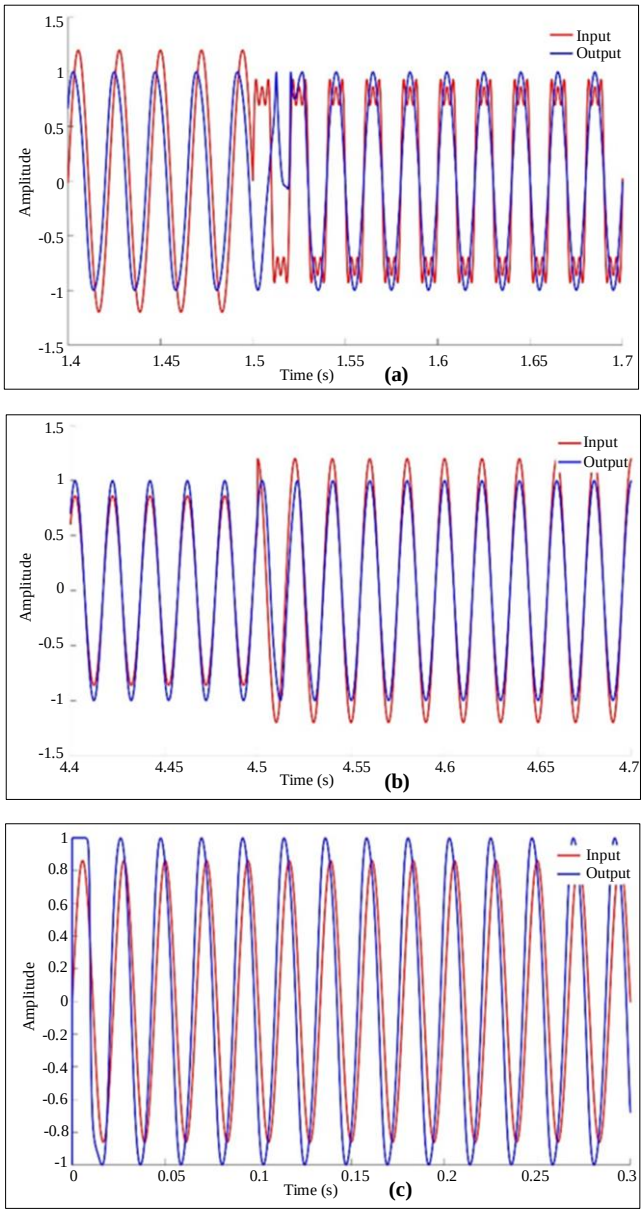


Fig. 3 Results of PLL having (a) 3rd and 5th harmonics, (b) Change in phase and amplitude, and (c) Change in frequency.

3.2. Single-Phase SOGI-PLL

Orthogonal signal generation is the basis on which this PLL works. Since it uses a SOGI to transform a 1-φ periodic (sinusoidal or non-sinusoidal) signal into a 2-φ quantity through Park's transformation (stationary reference frame of (α-β), and is further transformed into synchronous reference frame (d-q) as depicted from Figure 4.

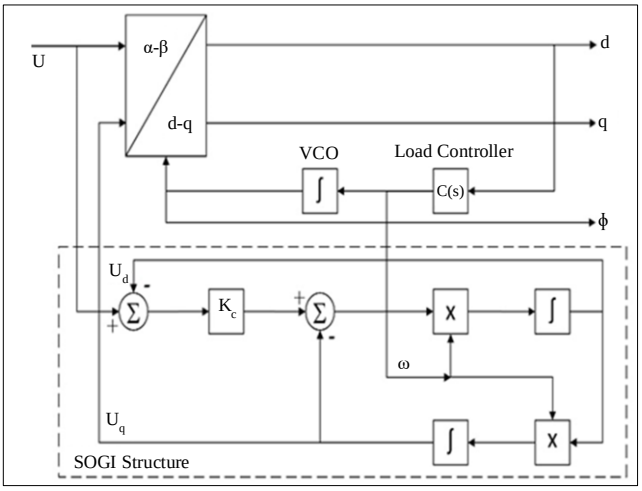


Fig. 4 PLL with 2nd order generalized integrator

SOGI can be represented in the form of open loop gain by Equation (2), in a closed loop in the d-axis by Equation (3) and in the q-axis by Equation (4) as:

$$C(s) = \frac{\omega s}{s^2 + \omega^2} \quad (2)$$

$$C_q(s) = \frac{U_q}{U} = \frac{K_c \omega^2}{s^2 + K_c \omega s + \omega^2} \quad (3)$$

$$C_d(s) = \frac{U_d}{U} = \frac{K_c \omega s}{s^2 + K_c \omega s + \omega^2} \quad (4)$$

K_c governs the Bandwidth (BW) of the filter and speed and, ultimately the robustness of the SOGI. Larger K_c gives sharper and selective gain response with sharp roll-off and it signifies better filtering abilities, but is sluggish in response and vice-versa. Bode plots of Equation (3) resemble that of a low-pass, and the plot of Equation (4) looks as if it is a band-pass filter, as can be depicted in Figures 5(a) and (b) for the different K_c. Figure 5(c) gives out the step response of the same. Looking at Figure 5, an intermediate and optimal value of Kc=0.9 has been considered for evaluating the performance of SOGI-PLL. This PLL, as shown in Figure 4, accommodates a resettable integrator that functions as a voltage-controlled oscillator responsible for reproducing the phase angle while C(s) acts as a filter. To nullify the steady-state error, it is required to accommodate two integrators, of which one is to have a pole at zero, and the other must possess a large value, to offer larger BW and, hence, robustness.

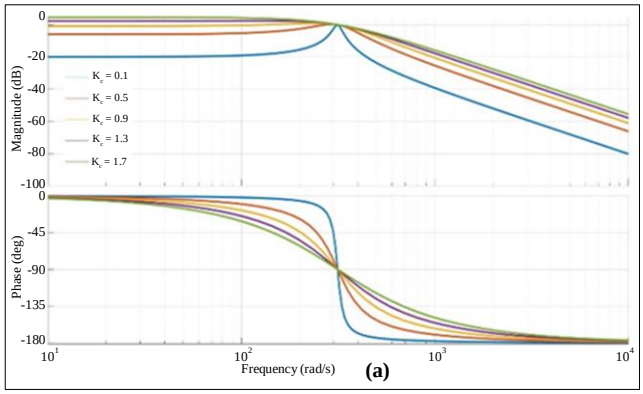


Fig. 5 (a) Bode plot of Equation (3), (b) Bode plot of Equation (4), and (c) Step response.

Conventionally, a PI is used as a controller in conjunction with the SOGI structure since it exhibits a strong Low-pass character, but at the expense of BW. Only with a larger BW, robust performance can be assured, but with a sluggish response. Converse of that improves the speed, but with an introduction of amplitude and phase angle error. These contradicting demands of larger BW and higher response speed could be achieved with the use of a lead controller [11] and hence it has been proposed for SOGI-PLL.

3.2.1. Design of Lead Controller for SOGI-PLL

The design has been initiated with an assumption of a possible *30%* increase in grid voltage (230V(rms)), i.e., V_m*=1.3*325V*, and ω*=314.15 rad/s*, as an input to the PLL. Double frequency components are inevitably present and are to be negotiated by introducing complex conjugate zeros at $\pm 2\omega$. Further, a pole at the origin and repeated poles at -2ω are allocated, which leads to a loop gain,

$$C(s) = L(s)\partial \frac{s^2+4\omega^2}{s^2(s^2+4\omega+4\omega^2)} \quad (5)$$

Substituting $C(s)\partial=1$, and considering a phase margin $>60^o$, $C(s)$ at a corner frequency of *200rad/s* can be calculated as -126^o. A 90^o phase lead is required which can only be attained by connecting two identical lead controllers of 45^o connected in cascade.

Following the standard lead controller design [11], considering the assumptions mentioned above, it could be evaluated as,

$$L(s) = f_{Lead}^2(s) = \left(\frac{s+83}{s+483}\right)^2 \quad (6)$$

Substituting Equation (6) and the value of ∂ in Equation (5) leads to the final loop gain as:

$$C(s) = \partial\left(\frac{s^2+1.6e6}{s^2(s^2+1.3e3+1.6e6)}\right)\left(\frac{s+83}{s+483}\right)^2 \quad (7)$$

$$\text{Substituting } \partial = \frac{\varepsilon}{V_m} = \frac{2.6e5}{423} = 616.1 \quad (8)$$

Where,

ε is $|L(j200)|$.

Substituting Equation (8) into Equation (7) leads to the evolution of final controller $C(s)$ as,

$$C(s) = 616.1\left(\frac{s^2+1.6e6}{s^2(s^2+1.3e3+1.6e6)}\right)\left(\frac{s+83}{s+483}\right)^2 \quad (9)$$

3.2.2. Result Analysis of SOGI-PLL

The designed controller $C(s)$ Equation (9) after having been substituted in the control block of SOGI-PLL (Figure 4), its performance has been evaluated through the testbed as presented in Figure 6, Figure 10 through Figure 16, and in Table 2. The revelations are as follows:

- The worst-case delay occurs at start-up, wherein SOGI-PLL takes around 0.1s to synchronize with the input.
- SOGI-PLL manages phase jump in 3.5 cycles.
- It responds to a step change in amplitude in just 30ms, with a corresponding error of 0.2^o.

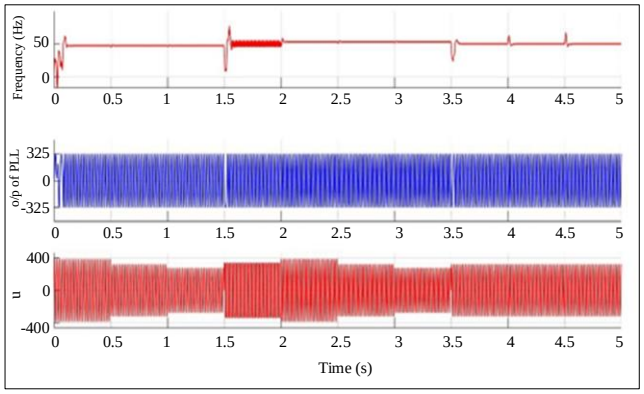


Fig. 6 Complete spectrum of *u* and output of SOGI-PLL

These findings demonstrate the strong and deserving character of the *1-φ* PLL having SOGI as an orthogonal signal generator and its controller's robustness, examined for the application with ES.

3.3. Improvised E-PLL structure

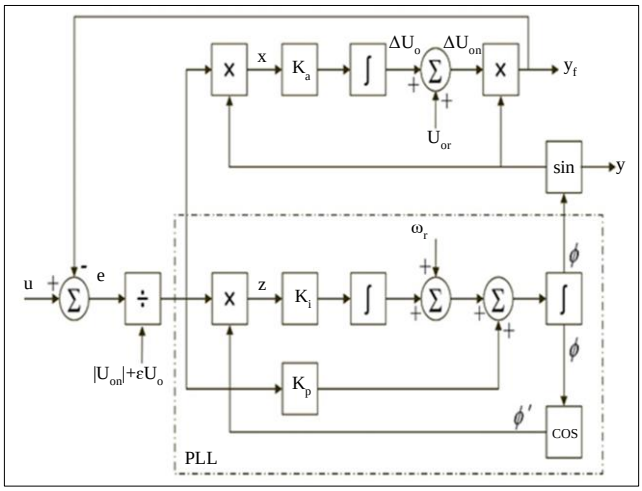


Fig. 7 IE-PLL structure

The primary drawback of oscillations created by double frequency components of the standard PLL structure could be easily mitigated by the Enhanced Phase Lock Loop structure (E-PLL). It was originally presented by M. Karimi [12], and an improvised version of the same (IE-PLL) has been proposed here, comprising an adaptive integrator for the application with ES. At the outset, it could furnish information about Phase angle, its orthogonal, angular frequency, amplitude, and normalized fundamental component. The E-PLL has been analyzed in [12].

The IE-PLL structure is included with K_a, K_p, and K_i respectively, named as magnitude, proportionality, and integral constant. Here, the value of K_i, as in Equation (10), has been made adaptive to follow the dynamically changing error to improvise the startup and transient performance of the conventional E-PLL so that it could function as an enhanced and improvised version of E-PLL.

$$K_i = \omega^2 \times \frac{1}{1 + \frac{\lambda|e|}{|U_{on}| + \epsilon U_o}} \tag{10}$$

Where,
$\lambda = 10$,
$e = u - y_f$,
$K_a = K_p = 2\xi\omega = 439.81$,
$\xi = 0.7$,
$\omega = 2\pi f_0 = 314.15$, and
$\varepsilon = 0.011$

The small modification proposed here in IE-PLL in the form of $e_1 = e/(|U_{on}| + \epsilon U_o)$ is responsible for providing enhanced robustness against dynamics in frequency and phase and making the response of the system faster due to the adaptive behavior of K_i, as compared to E-PLL, which has been presented in [12] for the PFA.

The designed IE-PLL has been evaluated through the testbed, and corresponding results have been assimilated in Figure 8, Figure 10 through Figure 16, and Table 2. The key findings are:

- It takes a start-up time of 0.01s to get synchronized with the input.
- It manages frequency jump and phase jump in less than 4 cycles.
- Filtering performance is a bit inferior, having a THD of 9%.

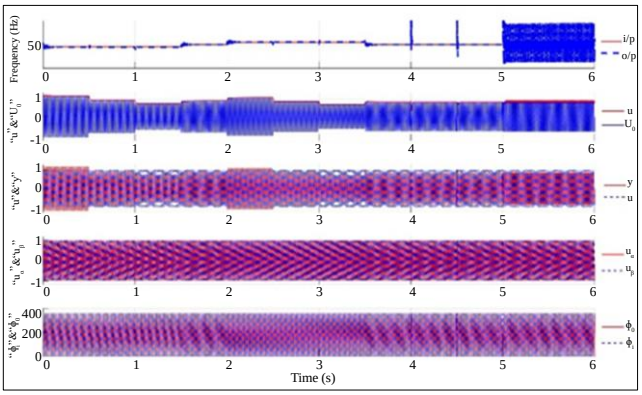
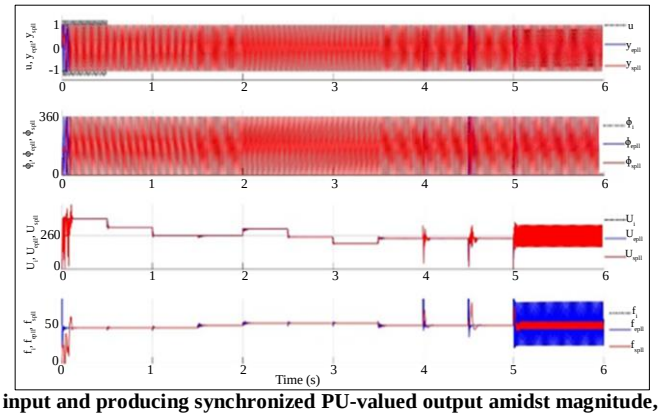


Fig. 8 Results of IE-PLL (complete spectrum)

4. Comparative Analysis

The Time period/3 delay PLL could not catch up with the task of frequency estimation and hence has been dropped being considered for comparative analysis. IE-PLL and SOGI-PLL have been critically analyzed for the startup delay, step change in magnitude, frequency, phase, and immunity against harmonics and their filtering abilities. The complete spectrum of the results in Figure 9, and in specific information in Figure 10 through Figure 16, and Table 2 accommodate parameters of interest: input-*u*, output-*y*, phase-*ϕ*, amplitude-*U*, and

frequency-*f*, (for SOGI-PLL and IE-PLL with the subscript of "$_{spll}$" and "$_{epll}$" respectively).



input and producing synchronized PU-valued output amidst magnitude, frequency, and phase variation

4.1. Start-Up Delay

The time required by the SOGI-PLL for a cold start is 0.11s, compared to that of IE-PLL is 0.02s, as could be evident from Figure 10 and Table 2.

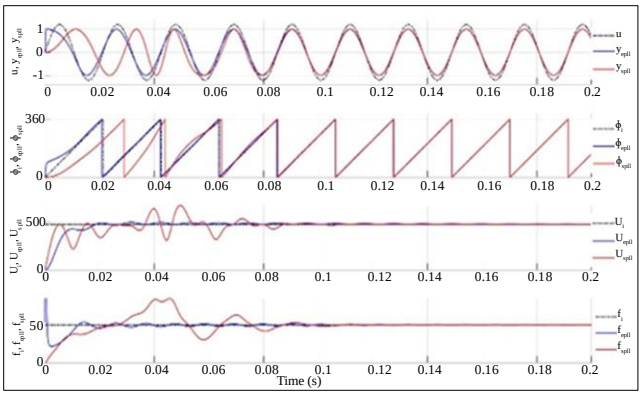


Fig. 10 Start-up delay

4.2. Step Change in Amplitude

The IE-PLL responds to step descent in the amplitude in a bit sluggish manner and attains a steady state faster without any undershoot. Similar is the case with frequency, and the phase is attained almost at the same instance, as evident from Figure 11 and Table 2.

4.3. Frequency Variation in the form of Step Change

The frequency of the test signal is varied in steps; at $1\frac{1}{2}$ *s*, *2s*, and $3\frac{1}{2}$ *s*, as seen in Table 2 and one such instance could be depicted in Figure 12. Signal, in terms of frequency, attains synchronism with lesser dynamics compared to amplitude with SOGI-PLL, and it reaches into steady state in less time, but frequency estimation is not the prime concern of PLL to be used with ES.

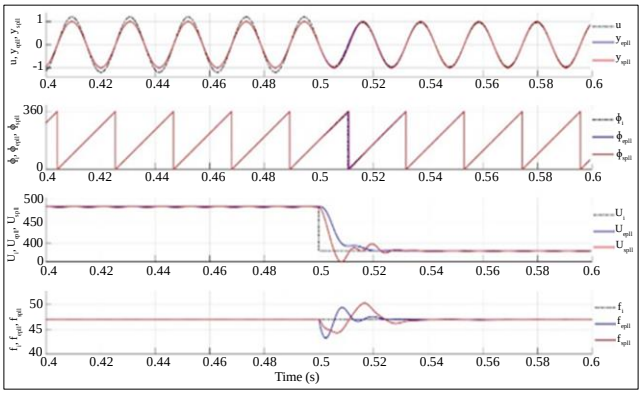


Fig. 11 Step change in the magnitude

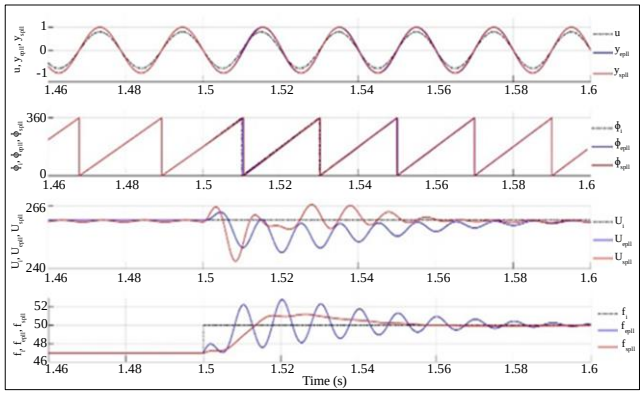


Fig. 12 Step change in frequency

4.4. Phase Variation in the form of Step Change

The phase of the test signal has been altered from 0º to 45º and 45º to 90º at 4s and 4.5s, respectively. IE-PLL is way swifter in attaining the phase, amplitude, and frequency, compared to SOGI-PLL, and shows smoother transition, as can be seen from Table 2 and Figure 13.

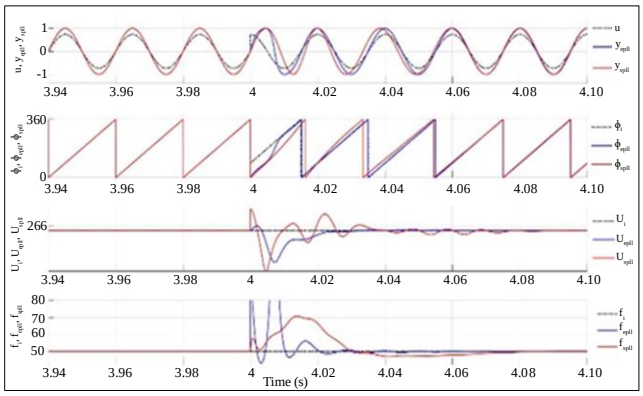


Fig. 13 Phase jump

4.4. Step Changes Applied Simultaneously to Amplitude and Frequency

The frequency and phase of the test signal have been varied simultaneously in the instances of $1\frac{1}{2}$ *s*, 2s, and $3\frac{1}{2}$ *s*, as evident from Table 2. One such instance can be seen in

Figure 14. SOGI-PLL exhibits smooth transition and lesser dynamics, and attain phase and frequency.

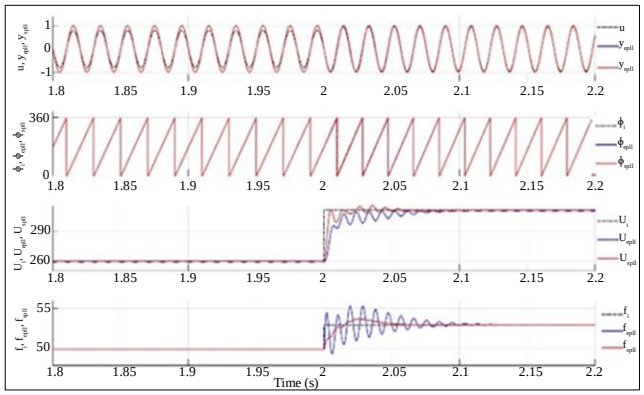


Fig. 14 Step change in amplitude and frequency

4.5. Signal Molested with Harmonics

3rd and 5th harmonics are induced into the signal at 5ths. IE-PLL takes less time to attain amplitude and phase, as can be depicted in Figure 15. FFT of the signal in Figure 16 reveals that SOGI-PLL performs better in filtering out the harmonics from a signal having THD of 51% to 1.5%, whereas IE-PLL THD is 9%.

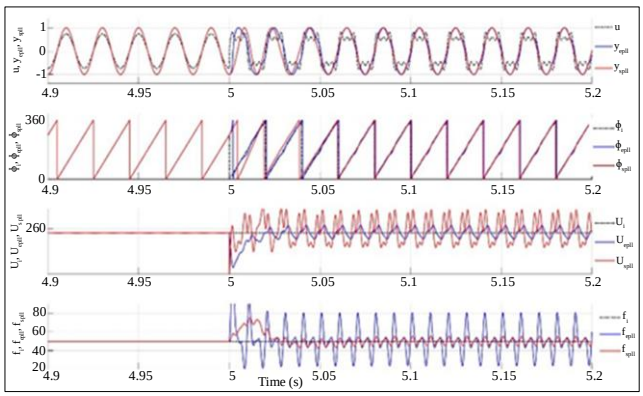


Fig. 15 Harmonically molested signal

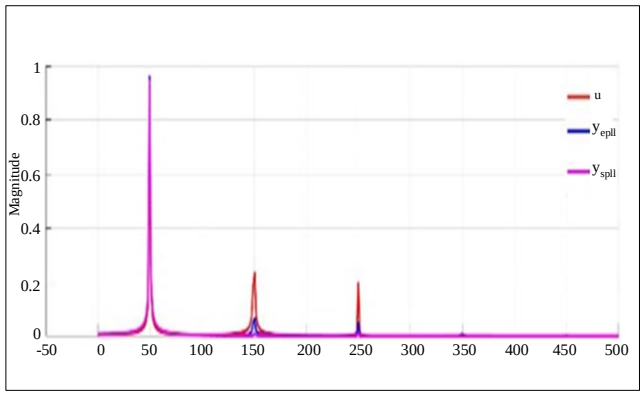


Fig. 16 FFT of harmonically molested signal

4.6. Performance Review of Proposed Enhancements in Standard SOGI-PLL and E-PLL

The proposed enhancement ($e_1 = e/(|U_{on}| + \epsilon U_o)$) in the form of adaptive K_i, which manages the error dynamically, in standard E-PLL structure to transform it into IE-PLL makes it more robust against parametric excursions and makes it swifter compared to E-PLL presented in [12] for the PFA. Similarly, SOGI, in conjunction with a controller accommodating two cascaded Lead controllers and a few well-placed poles and zero, gives it an edge over a conventional PI-controlled SOGI-PLL [10] in terms of speed and robustness. Looking at the comparative performance analysis, in terms of startup time, speed of response to step change, and minimal transients while responding to dynamics, IE-PLL has opted to be used with the phase tracking of ES, and the same has been examined in the next section.

5. Performance Evaluation of IE-PLL through its Application with ES

ES is a CPD that is primarily used for voltage regulation of critical load through the support of a Noncritical (NC) load and forms a smart load. The modeling and concept of ES have been nicely presented in [13]. The so-derived mathematical model is conceived in the form of a transfer function by omitting grid voltage (disturbance input) as,

$$P(s) = \frac{v_{critical}}{control\ i/p} = C(sI - A)^{-1}B + D \qquad (11)$$

Substituting model parameters from Table 1 in Equation (11) yields,

$$P(s) = \frac{6.3e7s + 1.03e11}{s^3 + 2.6e4s^2 + 5.2e8s + 5.9e11} \qquad (12)$$

Table 1. System parameters

Parameter	Value
Inductance of VSI- L_f	2 mH
Capacitance of VSI - C_f	6 μF
Inductance of feeder - L_g	0.305 mH
Critical Load - R_c	6.6 Ω
Noncritical Load - R_{nc}	2.2 Ω

A PI controller is derived using Equation (12) through the "systune" function of Matlab as,

$$C(s) = K\left(1 + \frac{1}{sT}\right) \qquad (13)$$

Where,
K = 3.38, and T = 5.469e-4
Design constraints:
Settling time < half cycle of 20ms, Gain margin >150db, and Phase margin > 70°

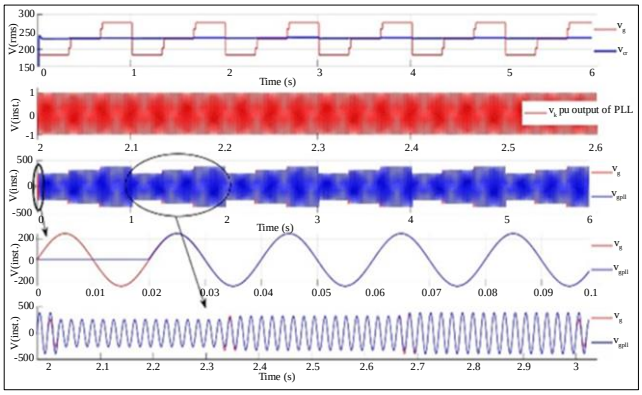


Fig. 17 Results of IE-PLL assimilated through ES

The voltage regulating capabilities of the same have been presented here for the sake of justifying the appropriateness of IE-PLL with the ES in Figure 17.

The first plot of Figure 17 reveals the voltage-regulating abilities of ES amidst varying grid voltage. IE-PLL plays a crucial role thereby providing synchronization with the controller's phase with that at the Point of Common Coupling (PCC). IE-PLL gives out the constant sinusoidal signal of unity amplitude by being in perfect synchronism with the voltage at PCC, which is evident from the second plot of Figure 17.

The third plot of Figure 17 shows v_g and $v_{g_{epll}} = \sqrt{2} v_{g_{rms}} v_{g_{pu}}$. Here, we can see that the two signals go hand in hand. Two sections of the plot have been amplified to see the efficacy of the proposed IE-PLL for the application of ES. The fourth plot is the magnification of the third plot for a period of 0s to *0.1s*, and it shows a delay of one cycle, considered as start-up time. The fifth plot is the magnified representation of the third plot for a period of *1.98s* to *2.02s*, representing three dynamic/step changes applied to the grid voltage v_g, wherein we could see a lag of only one cycle in catching up the v_g at four instances.

6. Conclusion

The system of SOGI-PLL represents a 5^{th} order system and hence is far more complex and complicated to design, whereas an IE-PLL is a 2^{nd} order system and hence a lot easier to implement. The performance of IE-PLL is excellent in terms of start-up time. Phase and frequency tracking is much better in the case of IE-PLL at the behest of a step change in phase and amplitude.

SOGI-PLL negotiates harmonics in a better way by filtering it out in a better manner, but IE-PLL is not much lagging in this domain either. Looking at the overall performance, IE-PLL proved to be a better choice to be opted for, as far as the startup time, dynamically changing voltage, and phase angle.

The ES, using IE-PLL, commensurate with the claimed efficacy of the results presented in Section 4 and Table 2, wherein the start-up time and the time required to synchronize with the signal in the case of step change is 0.02s (one cycle of 50Hz signal), and hence IE-PLL has proved itself a worthy contender to be used with ES.

References

[1] D.W.P. Thomas, and M.S. Woolfson, "Evaluation of Frequency Tracking Methods," *IEEE Transactions on Power Delivery*, vol. 16, no. 3, pp. 367-371, 2001. [CrossRef] [Google Scholar] [Publisher Link]

[2] A.G. Phadke, J.S. Thorp, and M.G. Adamiak, "A New Measurement Technique for Tracking Voltage Phasors, Local System Frequency, and Rate of Change of Frequency," *IEEE Transactions on Power Apparatus and Systems*, vol. PAS-102, no. 5, pp. 1025-1038, 1983. [CrossRef] [Google Scholar] [Publisher Link]

[3] A. Routray, A.K. Pradhan, and K.P. Rao, "A Novel Kalman Filter for Frequency Estimation of Distorted Signals in Power Systems," *IEEE Transactions on Instrumentation and Measurement*, vol. 51, no. 3, pp. 469-479, 2002. [CrossRef] [Google Scholar] [Publisher Link]

[4] M.M. Giray, and M.S. Sachdev, "Off-Nominal Frequency Measurements in Electric Power Systems," *IEEE Power Engineering Review*, vol. 9, no. 7, pp. 42-43, 1989. [CrossRef] [Google Scholar] [Publisher Link]

[5] M.M. Begovic et al., "Frequency Tracking In Power Networks of Harmonics," *ICHPS V International Conference on Harmonics in Power Systems*, Atlanta, GA, USA, pp. 151-157, 1992. [CrossRef] [Google Scholar] [Publisher Link]

[6] P.K. Dash et al., "Estimation of Power System Frequency Using Adaptive Notch Filters," *Proceedings of EMPD '98, 1998 International Conference on Energy Management and Power Delivery (Cat. No.98EX137)*, Singapore, vol. 1, pp. 143-148, 1998. [CrossRef] [Google Scholar] [Publisher Link]

[7] V.V. Terzija, M.B. Djuric, and B.D. Kovacevic, "Voltage Phasor and Local System Frequency Estimation Using Newton Type Algorithm," *IEEE Transactions on Power Delivery*, vol. 9, no. 3, pp. 1368-1374, 1994. [CrossRef] [Google Scholar] [Publisher Link]

[8] L.L. Lai et al., "Real-Time Frequency and Harmonic Evaluation Using Artificial Neural Networks," *IEEE Transactions on Power Delivery*, vol. 14, no. 1, pp. 52-59, 1999. [CrossRef] [Google Scholar] [Publisher Link]

[9] Paul C. Krause, Oleg Wasynczuk, and Scott D. Sudhoff, *Analysis of Electric Machinery and Drive Systems*, Wiley IEEE Press, 2002. [Google Scholar] [Publisher Link]

[10] Mihai Ciobotaru, Remus Teodorescu, and Frede Blaabjerg, "A New Single-Phase PLL Structure Based on Second Order Generalized Integrator," *2006 37th IEEE Power Electronics Specialists Conference*, Jeju, Korea (South), 2006, pp. 1-6. [CrossRef] [Google Scholar] [Publisher Link]

[11] Katsuhiko Ogata, *Modern Control Engineering*, 5th ed., Prentice Hall, 2010. [Publisher Link]

[12] Masoud Karimi-Ghartema, *Enhanced Phase-Locked Loop Structures for Power and Energy Applications*, John Wiley & Sons, 2014. [CrossRef] [Google Scholar] [Publisher Link]

[13] Qingsong Wang et al., "A Parameter-Exempted, High-Performance Power Decoupling Control of Single-Phase Electric Springs," *IEEE Access*, vol. 8, pp. 33370-33379, 2020. [CrossRef] [Google Scholar] [Publisher Link]

Appendix 1

Table 2. Comparative analysis of results

Time Interval (s)	Peak Amplitute U_m	Frequency of u (Hz)	Frequency Included	Phase Angle (deg)	Type of Change	Time to Synchronize						PLL Error (deg)	S-PLL Error (deg)
						U_{epll}	U_{spll}	ϕ_{epll}	ϕ_{spll}	f_{epll}	f_{spll}		
0.0-0.5	390	47	f_0	0	Amplitute	0.02	0.11	0.04	0.1	0.01	0.11	0.2267	0.225026
0.5-0.1	325	47	f_0	0	Amplitute	0.02	0.02	0.02	0.02	0.01	0.02	0.2239	0.220975
0.1-1.5	271	47	f_0	0	Amplitute	0.01	0.01	0.02	0.02	0.01	0.02	0.2250	0.226728
1.5-2.0	390	50	f_0	0	Frequency & Amplitute	0.08	0.06	0.02	0.07	0.08	0.04	0.2193	0.219283
2.0-2.5	390	55	f_0	0	Frequency & Amplitute	0.06	0.06	0.02	0.05	0.08	0.04	0.2227	0.218437
2.5-3.0	325	55	f_0	0	Amplitute	0.02	0.02	0.02	0.02	0.02	0.03	0.2218	0.221821
3.0-3.5	271	55	f_0	0	Amplitute	0.02	0.02	0.02	0.02	0.02	0.03	0.2210	0.226728
3.5-4.0	325	50	f_0	0	Frequency & Amplitute	0.08	0.08	0.02	0.05	0.08	0.06	0.2201	0.223852
4.0-4.5	325	50	f_0	45	Amplitute & Phase	0.03	0.1	0.02	0.1	0.04	0.08	0.2193	0.225036
4.5-5.0	325	50	f_0	90	Amplitute & Phase	0.03	0.1	0.02	0.14	0.04	0.11	0.2184	0.219283
5.0-6.0	U_0=325; U_3=U_0/3; U_5=U_0/5	f_0=50; f_3=150; f_5=250	f_0 +f_3 +f_5	0	Harmonics	0.08	0.1	0.02	0.1	0	0	0.5562	8.9532