SSRG International Journal of Electrical and Electronics Engineering
ISSN: 2348-8379/ https://doi.org/10.14445/23488379/IJEEE-V11I8P104

Volume 11 Issue 8, 36-49, August 2024

Original Article

Design of High-Speed Low Power 4-bit ALU Using CNTFET

B. Anjaneyulu[1], N. Siva Sankara Reddy[2]

[1]*Department of E.C.E., College of Engineering, Osmania University, Telangana, India.*
[2]*Department of E.C.E., Vasavi College of Engineering, Hyderabad, India.*

[1]*Corresponding Author : anjaneyulu702@gmail.com*

Received: 02 June 2024 Revised: 04 July 2024 Accepted: 02 August 2024 Published: 31 August 24

Abstract - *As the electronic semiconductor sector undergoes downsizing, there are many challenges, including scaling, short-channel impacts, leakage currents and stability. Carbon Nanotubes (CNT) have emerged as an exciting new invention that can overcome the limitations of CMOS while maintaining high efficiency and dependability. The Arithmetic and Logical Unit (ALU) is the central operational programmable logic component that exists in microprocessors, and real-time computer chips. Traditional Arithmetic Logic Units (ALUs) were created utilizing CMOS technology, leading to high power usage, delays, as well as transistor count. This article specifically addresses the conceptualization and development of a hybrid Arithmetic Logic Unit (ALU) employing Carbon Nanotube Field-Effect Transistors (CNTFET). First, a combination of XOR and MUX is developed, which is then utilized to create hybrid adders and subtractors. The study showcases the development, simulation, and evaluation of an enhanced Arithmetic Logic Unit (ALU) utilizing Carbon Nanotube (CNT) technology and compares it to a traditional CMOS implementation using 32 nm technology nodes. The ALU that utilizes Carbon Nanotube (CNT) technology showed higher performance with regard to power usage, propagation delay, and the Power-Delay Product (PDP) when compared to its counterparts depending on CMOS technology.*

Keywords - *CNTFET, ALU, Power, Delay, CMOS, Short-channel impacts.*

1. Introduction

In the past few years, there has been a demand for reducing the dimensions and energy consumption of digital circuits by optimizing time while boosting efficiency. The basic digital circuits are composed of adders as well as multipliers as it is foundational components. Moreover, these components are often used as distinct modules in Digital Signal Processing (DSP) and Arithmetic Logic Unit (ALU) systems. DSP encompasses techniques such as spectral analysis, digital filtering, DFT, and FFT to enhance and modify digital signals. The power utilization performance depends on the operation of the adder. The field of convenience electronics that comprises the VLSI sector is seeing rapid growth, particularly regarding the design of low-power arithmetic circuits. Enhancing the power and area efficiency of a rapid information path scheme is an investigation area of focus. The computation speed achieved by the adder is restricted by the amount of time needed for carry transmission in digital adders. The bits within an adder circuit are produced sequentially, following a constant pattern, and they transport a carry signal to the next position.

ALUs are essential components of several high-performance structures, including DSP, spectrum analysis and digital communications. The efficiency of a system can be assessed by the effectiveness of the multiplier, which is the component that takes up the most area and operates at the lowest rate of speed. Therefore, it is essential to optimize the speed and area of the multiplier. Various techniques and concepts have been developed to achieve a more optimal proportion of area and speed because these two factors impose conflicting constraints.

In addition, the fact that numerous DSP applications are geared towards portable devices means that both battery life and power consumption are important design constraints. ALUs, or Arithmetic Logic Units, are essential components found in Integrated Circuits (ICs). They are extensively used in many VLSI systems, including specialized applications of DSP architectures and microprocessors [4, 5]. In addition, the ALU does computations such as additions, along with multiplications, correspondingly. The primary objective of addition is to combine two binary integers. This operation serves as the foundation for other essential operations, including multiplication.

Division, subtraction, and computations, among others. An adder is an integral component of the most significant path

systems since it governs the general efficiency of these systems. Optimizing the efficiency of the ALU cell, which serves as the fundamental building block for binary addition, is a crucial objective.

In recent times, there has been a significant advancement in VLSI systems, particularly in terms of low power consumption. This has been driven by the rapid progress in mobile computing and communication technological advances, leading to a high demand for such systems. However, mobile systems have limited power capabilities. Full Adder (FA) serves as the fundamental component of a variety of digital Very Large Scale Integration (VLSI) circuits. Improvements have been made to the structure that constitutes it since its conception.

In submicron as well as submicron technologies [6, 7], VLSI engineers aim to minimize the amount of power used by VLSI Integrated Circuits (ICs), both when they are idle and when they are active. When considering the energy efficiency of arithmetic circuits within processors, it becomes necessary to acquire an energy-effective ALU design. When designing an energy-efficient Arithmetic Logic Unit (ALU) for use in higher-order adders, a crucial factor to consider is the decrease in overall power usage. This is going to contribute to an increased rate of logical level signal transitioning in both internal as well as external loads for each subcircuit inside arithmetic components, resulting in substantial utilization of dynamic power.

Therefore, the primary aspect that contributes to enhancing energy efficiency in mathematical building blocks is the decrease in dynamic power usage. Increased leakage current throughout discrete devices manufactured in VLSI ICs results in a significant jump in static power usage. To create an energy-efficient ALU cell, it is necessary to focus on reducing static as well as dynamic power usage. This is clearly shown by the subsequent analysis of power dissipation in circuits based on CMOS technology [8, 9].

Currently, FinFET, Carbon Nanotube FET (CNT FET), GnrFET, and RibbonFET are extensively used in many applications to enhance area, Delay, and power efficiency. The development of these sophisticated FET models involves adjusting several processing factors. This study focused on the use of Carbon Nanotube Field-Effect Transistors (CNTFETs) for the design and fabrication of different mathematical operations. The primary advancements of this study are shown in the following manner:

The research investigation introduced a new and enhanced version of a full-swing 11 Transistor (11T) adder. This adder is developed and demonstrated using CNTFET technology and implemented using CMOS at the 32 nm technology node. Additionally, the study demonstrates the design and modelling of a subtractor using CNTFET technology. Furthermore, the study focuses on the development and modelling of AND and OR gates. A 4-bit Arithmetic Logic Unit (ALU) has been designed and demonstrated with Carbon Nanotube Field-Effect Transistors (CNTFETs) with a CMOS implementation at the 32 nm technology node. The remaining sections of the paper are presented as follows: Section 2 focuses on the relevant research and issues. Section 3 introduces the CNTFET model. Section 4 pertains to the suggested methodology. Section 5 analyzes and interprets the simulation findings. Section 6 concludes by discussing potential areas for future development and expansion.

2. Literature Review

This section provides a comprehensive overview of the several adders that have been produced in recent years. The survey primarily focuses on the examination of hybrid adders. In their study, the investigators in [9] designed approximation adders that demonstrated smaller dimensions but had a slower speed. On the other hand, the carry look ahead method resulted in much faster performance but required more area to operate. The addition procedure of faster speeds involves the design and implementation of a full adder [10].

In addition, the CNFET-based Full Adder uses a streamlined and effective approach to modify the gate level while decreasing parameters in the standard HFFA [11]. The authors in [12] designed the Hybrid Full Adder (HFA) designs specifically for the processing of video and image applications. The design of the addition demonstrates the gate thickness and incorporates a pair of RCAs having input values of 0 and 1, correspondingly. Additionally, FA is an optimization procedure specifically designed to meet the limitations of VLSI designs.

The quaternary half adder as well as 1-trit multiplication structure were created [13] and assessed for their efficacy in regards to area, power, alongside latency. To address the challenges of space, power, and latency utilization in 4-bit and 8-bit CNTFET circuits, the Ternary Full Adder Circuit (CTFA) and Carbon Nanotube Field-Effect Transistor (CNTFET) Ternary Adder (CTA) was designed in [14] without using a Multiplexer (Mux) and instead employing approximation adders. Simulations showed that the improved designs performed better than the current state-of-the-art techniques.

The MTCMOS Subtractor (MTCMOSS) [16] provides a fast and straightforward method for processing VLSI hardware configurations. The mobile phone sector is seeing significant growth, driven not only by the increasing number of arithmetic units but also by the development of more efficient and compact arithmetic units.

In their study, the authors introduced the PTL-based Subtractor (PTLS) using gate-level changes, resulting in a

reduced number of gates needed to carry out the operation in their suggested work. It offers both area reduction and overall power optimization. The evaluation of the results indicates that the circuit exhibits greater efficiency and is quicker than the other circuits. The performances of the modified CSLA were assessed in conjunction with those of other adders. The logic conversion introduces modest delay modifications to the circuit by using the BEC modifications rather than the MFA [18] circuit. TUTS's high-speed processing capabilities are used for performing arithmetic tasks in data handling processors.

In their study, the researchers introduced a novel approach called CNTFET-based Adder and Subtractor (CNTFET-AS) [18]. This method offers a combination of rapid computation and small dimensions, although it does need a larger amount of space. Furthermore, CNTFET may be easily used with low-power multiplication. Simulation findings demonstrated greater efficiency compared with conventional adders that utilized FinFET technology [19, 20].

The researchers in [21] created an 8-bit Dadda multiplication (FDM) utilizing 14 nm FinFET technological devices with approximated 4 : 2 compressors. The authors within [22] devised an approach for constructing an area-efficient approximation multiplier using FinFET technology. The methodology focuses on minimizing voltage and current usage in the circuits. These modifications were made for an existing functioning EETM and present conveyor.

An N-bit ALU [23] had been designed utilizing 18 nm FinFET technology. It mostly performs addition operations, and its architecture prioritizes speed, which is a crucial efficiency measure. Digital circuits featuring high-speed efficiency have traditionally been highly valued. This approach is experiencing significant computational difficulties. The authors in reference [24] designed a high-speed 8-bit Arithmetic Logic Unit (ALU), referred to as HS-ALU, employing 18 nm FinFET technological devices. The design of HS-ALU has been dependent on Kogge Stone addition as well as Dadda multipliers. It is a commonly seen operation in many real-time DSP implementations; however, it requires a considerable amount of power.

The authors within [25] designed the FALU-32, a 4-bit Arithmetic Logic Unit (ALU) dependent on 32 nm-FinFET technology. The FALU-32 was constructed utilizing array multiplication and carry save additions. The power usage of the ALU circuitry has to be reduced for two specific explanations: to minimize the loss of heat and to maintain a large number of functions required for managing the IC. A delay-controlled hybridization adder and subtractor was generated by merging the the existing hybrid adder, as described in [26]. Furthermore, a delay control array multiplication was also created utilizing proposed adder modules.

The results of the research [27] employ CNTFET devices to create and execute highly effective ternary logical gates. The suggested STI design enhances energy efficiency and boosts noise margin, whilst the recommended TBUF architecture decreases energy usage. In addition, the suggested TOR architecture decreases power usage along with energy consumption, whereas the suggested TAND architecture enhances these. The mathematical calculations were conducted employing the HSPICE program, employing the Stanford 32 nm CNTFET approach, utilizing a supply potential of 0.9 V. The suggested work [28] introduces a ternary 1-trit multiplication circuit that uses pass transistor logic. This circuit utilizes just 28 transistors. The suggested logic circumvents the traditional method of employing logic gates, multiplexers, and encoder/decoder, resulting in a decreased overall device number required for implementing the multiplier function. The decreased number of transistors results in lower power usage and latency compared to other advanced systems. The simulations were conducted using the Stanford 32-nm CNTFET modelling file and the Synopsis HSPICE simulator, with a supply voltage of 0.9 V.

3. Introduction to Carbon Nanotube Field Effect Transistors (CNTFETs)

Carbon Nanotubes (CNTs) have a great reputation for substances with extraordinary mechanical and physical properties. They are now being extensively studied for a wide variety of applications, ranging from large-scale constructions to nanometer-scale electronics [29]. CNTs had been serendipitously identified by Japanese scientist S. Iijima [30] in 1991 while doing studies on carbon. Carbon nanotubes (CNTs) are tiny tubes made from rolled sheets of graphite. They have exceptional properties, such as outstanding tensile strength, high conductivity of electricity, and remarkable stability chemically [31].

Carbon nanotubes (CNTs) represent nano-materials which are detectable only with a Transmission Electron Microscope (TEM) [32]. They represent the smallest-scale elements in the field of nanotechnology. Carbon Nanotubes (CNTs) may be categorized into two types: Single-Walled (SWCNT), which consists of a single nanotube, and Multi-Walled (MWCNT), which are composed of several nanotubes having a distance of 0.34 nm between each layer.

The electrical properties of CNTFETs rely on the chirality vector, which is defined by the integer pairing (n, m). The chiral vector indices specify the orientation in which the sheet of graphene is rolled. Figure 1 illustrates the architecture of a conventional CNTFET device. The Carbon Nanotube (CNT) within the device functions as a conductive pathway of the transistor that a gate may alter. The drain and source contacts of a CNTFET are heavily doped, but the gate region may remain undoped. The width of the CNTFET gate is determined by the number of adjacent Single-Walled Carbon Nanotubes (SWCNTs).

The pitch value is the measurement of the distance across the axes of two neighbouring Single-Walled Carbon Nanotubes (SWCNTs). The gate width of a CNTFET is computed using Equation (1), as mentioned in reference [33].

$$\text{Channel Gate Width } (W_{gate}) = \text{Maximum } (W_{minimum}, M \times \text{Pitch}) \quad (1)$$

Where in,

$W_{minimum}$= CNTFET gate minimum width,

M - Quantity of SWCNTs positioned underneath the gate of the transistor.

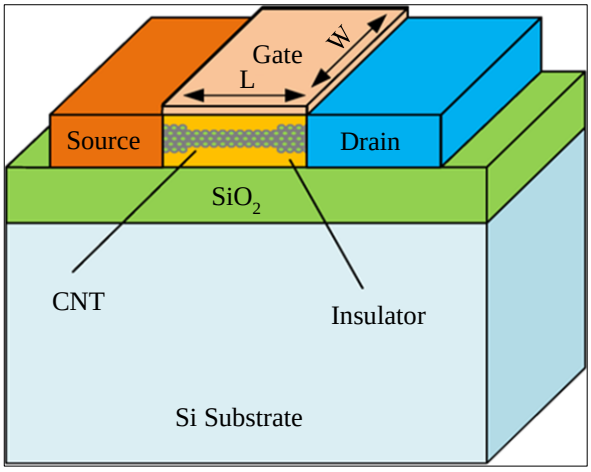

Fig. 1 Structure of CNTFET device

To compute the diameter of a CNT, we apply Equations (2) and (3) as shown [34].

$$D_{CNT} = \frac{\sqrt{3}\, a_0}{\pi} \sqrt{m^2 + n^2 + mn} \quad (2)$$

$$= 0.0783\sqrt{m^2 + n^2 + mn} \quad (3)$$

The spacing between neighbouring carbon atoms has been designated as $a0$ and represents 0.142 nm. The rolling direction of a Carbon Nanotube (CNT) is specified by the chirality vectors n and m.

4. Proposed CNTFET-Based 4-Bit ALU

Arithmetic Logic Units (ALUs) constitute fundamental components of all integrated circuits, and they play a crucial role in determining the efficiency of numerous applications. Therefore, optimizing the architecture of adders and subtractors would improve the efficiency of embedded processors. This subsection focuses on the comprehensive examination of the development of a hybrid ALU. The ALU is produced employing hybrid full-swing adder, subtractor, AND and OR gates. Additionally, these adders and subtractors are designed utilizing a hybrid logic-based swing logic. Figure 2 depicts the N-bit design of the recommended Arithmetic Logic Unit (ALU), which effectively utilizes sophisticated full adders to provide minimal area, power usage, and delay features. In this case, A and B represent N-bit inputs, S represents the selection line that includes two inputs, whereas OUTPUT represents the ultimate output of the ALU. In addition, the ALU will carry out various operations depending on the selected combinations.

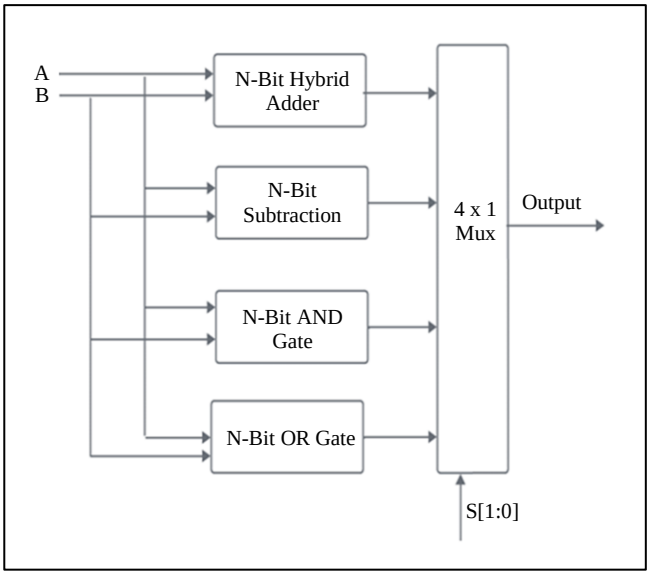

Fig. 2 Block diagram of N-bit ALU

Table 1 illustrates the comprehensive steps for every possible selection combination in the proposed Arithmetic Logic Unit (ALU).

Table 1. Operations of proposed ALU

S. No.	Selection Inputs (S[1:0])	Function
1	00	Addition
2	01	Subtraction
3	10	AND gate
4	11	OR gate

4.1. Design of 4-Bit Addition

Adder modules are crucial computational devices which operate as basic arithmetic elements. The Full Adder (FA) element represents the most common and essential computational element in the field of adder modules. The FA designed in this work used XOR gates along with a multiplexer. Enhancing and maximizing the effectiveness of the adder circuitry could optimize and improve the effectiveness of larger and more complex circuits. As a result, we developed and implemented a cutting-edge F.A. circuitry employing the "execution involving XOR gates with a 2x1 mux". Figure 3 is a schematic block representation of the whole adder design.

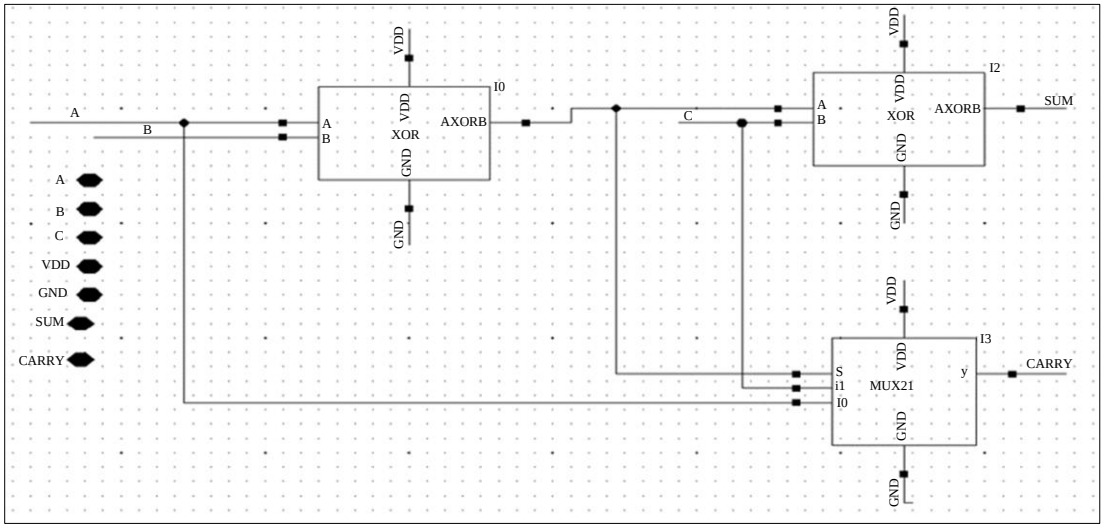

Fig. 3 Proposed full adder implementation using XOR and MUX modules

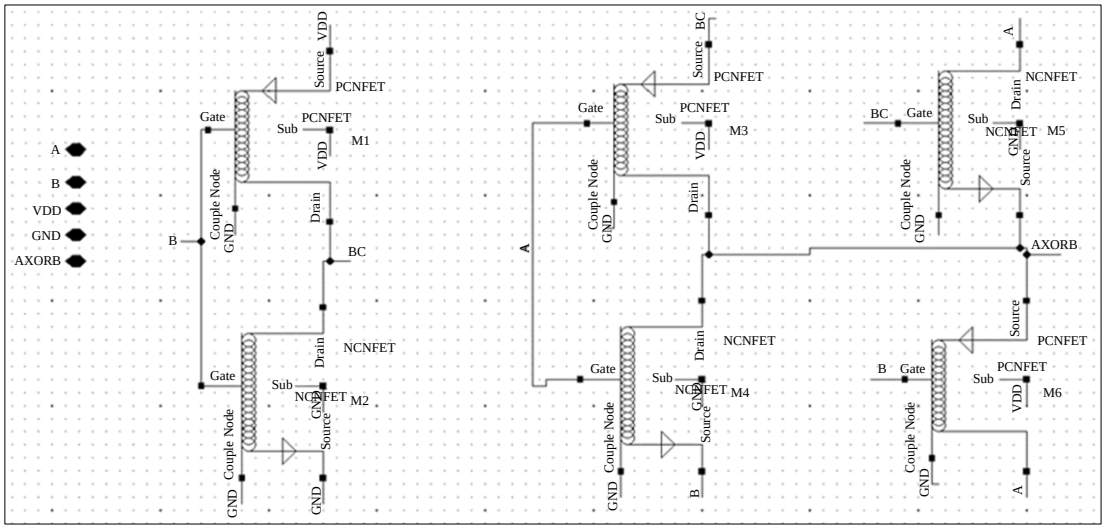

Fig. 4 CNTFET-based implementation of XOR gate

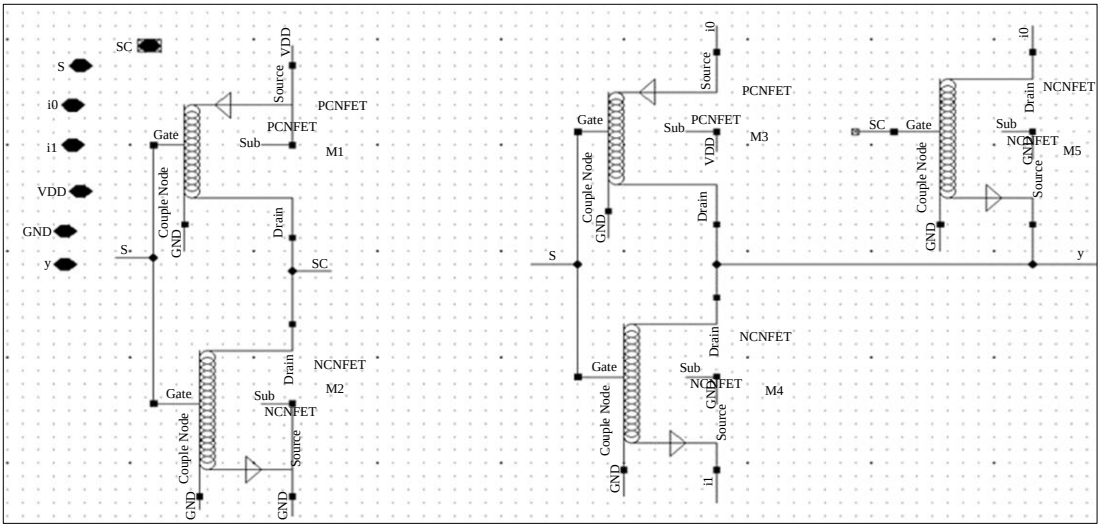

Fig. 5 Full swing hybrid 2x1 MUX

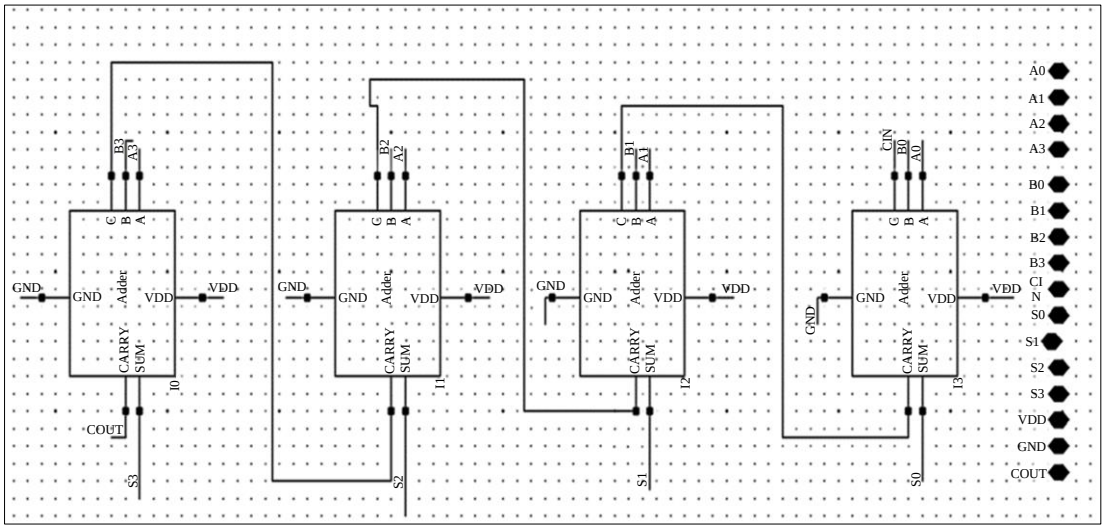

Fig. 6 Illustration of 4-bit hybrid adder

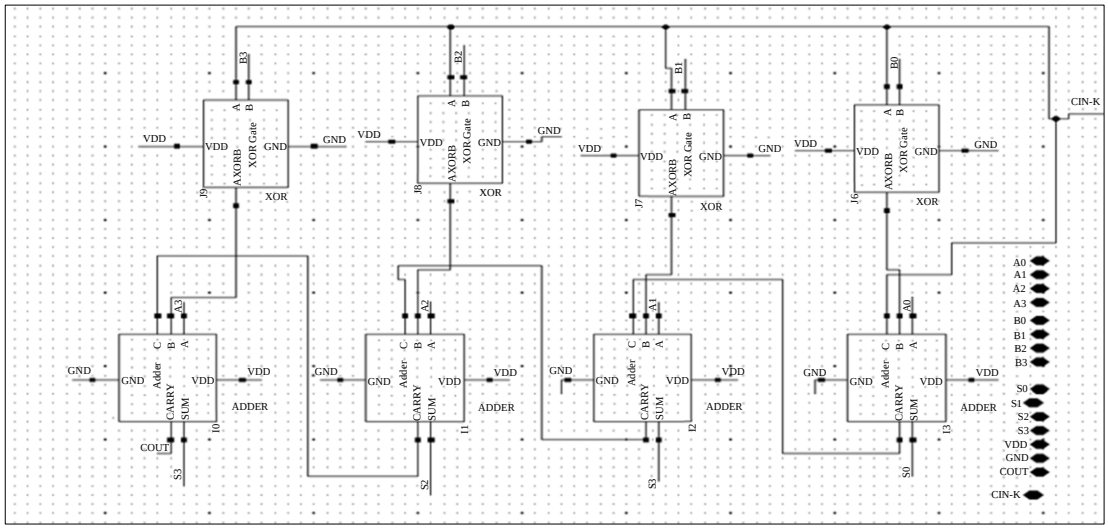

Fig. 7 Illustration of 4-bit hybrid subtraction

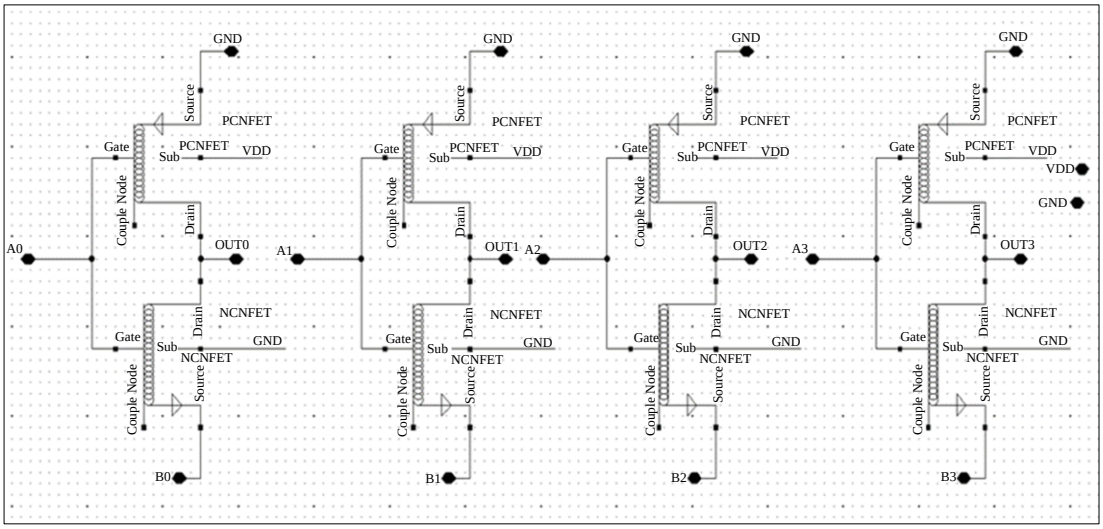

Fig. 8 Illustration of 4-bit bitwise AND gate

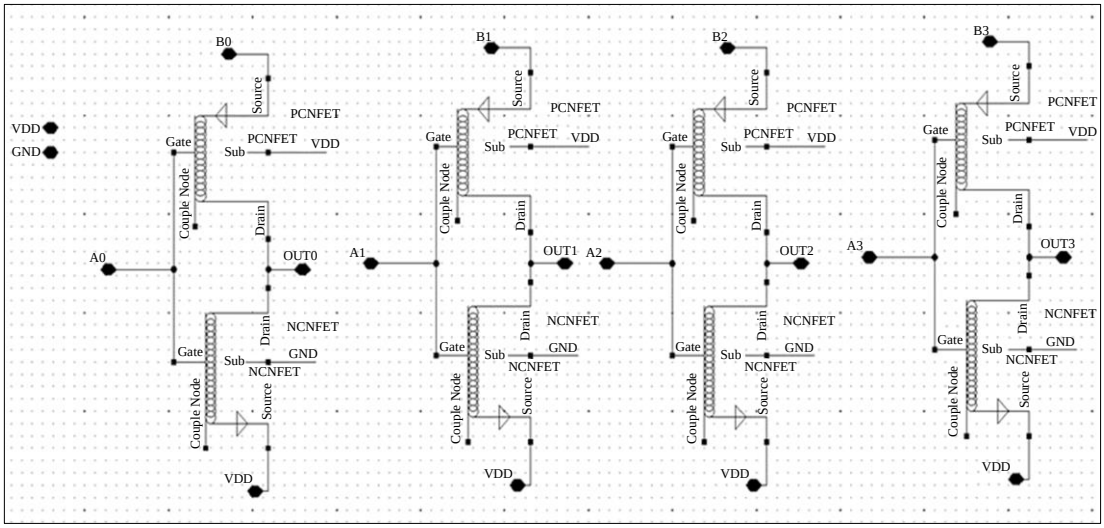

Fig. 9 Illustration of 4-bit bitwise OR gate

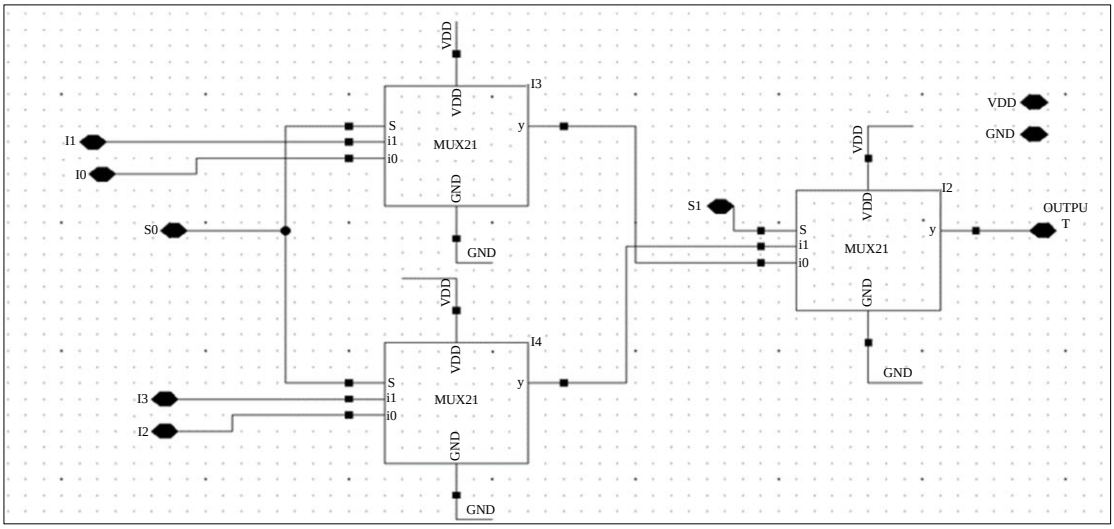

Fig. 10 Full swing 4x1 MUX

The XOR gate design that is proposed has been specifically built to demonstrate full swing operation. The suggested 1-bit full addition design relies on it as a crucial element, and the effectiveness of the adders has been assessed by utilizing the full-swing XOR gate. The proposed XOR gate employs four transistors, with the exception of an inverter used to generate the complementary input in order to provide a full-swing result. Figure 4 depicts the arrangement of an XOR gate, which employs a full swing. The CNTFET Transistors M6, M5, and M3 possess a conducting state whenever AB equals 00.

The CNTFET transistor M5 continues to play a crucial role in delivering a robust '0' signal. In a separate scenario, where AB is equivalent to 10, the CNTFET transistors M6, M5, and M4 operate in a manner that M6 sends a robust '1' output into the output terminal. CNTFETs M5 and M6 have no impact on the resultant voltage whenever AB equals 01 and also 11. Hence, the proposed design effectively attains an accurate outcome regarding the XOR gate.

Figure 5 depicts the structure of a complete swing 2x1 MUX within this research. The CNTFETs M3 along with M4 form a Multiplexer (MUX) employing GDI functionality. The problem regarding the GDI MUX arises because of its restricted ability to manage a high-voltage input. In order to maintain an extensive variety of output voltages, the M5 CNTFET was attached in parallel alongside the M3 device. Figure 6 illustrates the 4-bit hybrid adder.

4.2. Design of 4-Bit Subtraction

The illustration of 4-bit hybrid subtraction is depicted in Figure 7. The subtraction has been developed from adder. The initial full adder features a control line that serves as its initial input (input carry CIN). The input A0 for the adder has been immediately fed into the full adder.

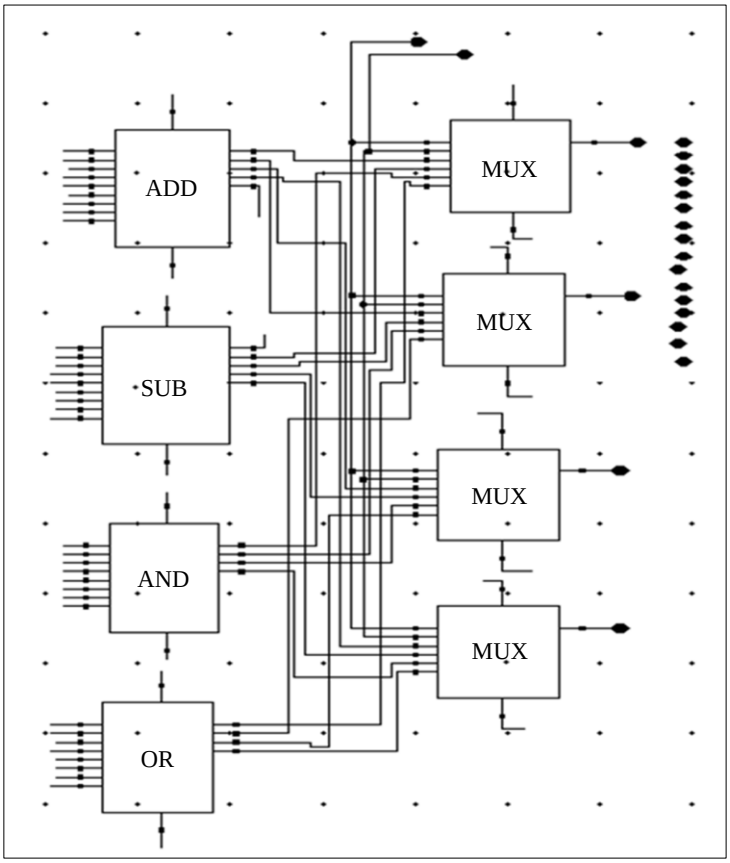

Fig. 11 CNTFET implementation of 4-bit ALU

The third and final input corresponds to the exclusive OR (xor) of B0 along with CIN-K. Each of the resulting outputs is Sum/Difference (S0). In addition, the carry value (C0). Whenever the initial value of CIN-K becomes 1, then the result of B0 XOR K is equal to the corresponding complement of B0, denoted as B0′. Therefore, the operation may be expressed as A plus the complement of B0. The 2's complement subtraction involving two integers A and B is calculated using the formula A + B' + Cin. This implies that whenever CIN-K = 1, the mathematical operation being carried out on the four-bit values is subtraction.

A1, A2, and A3 are used as inputs for the following full adders, namely the third and fourth ones. Subsequently, the third input entails the XOR operation, where B1, B2, B3, and CIN-K are combined, and the result is linked to the subsequent, third, and fourth full adders. The carry C 1 and C 2 are consecutively sent to the next full adder as the input. The term "COUT" denotes the final carry value throughout the computation of a sum or difference. The outcome is generated by combining the recordings of S1, S2, and S3 alongside S0.

4.3. Design of 4-Bit Logic Gates

The 4-bit CNTFET AND gate and OR gates are demonstrated in Figures 8 and 9, respectively. The AND and OR gates have been designed using GDI logic. In the AND gate, the inputs of PCNFET and NCNFET are connected to form an input A. The sources of PCNFET and NCNFET are connected to ground and input B, respectively.

The drains of both the CNTFET are connected to form the output node. In the OR gate, the inputs of PCNFET and NCNFET are connected to form an input A. The sources of PCNFET and NCNFET are connected to input B and VDD, respectively. The drains of both the CNTFET are connected to form the output node.

4.4. Design of 4 to 1 MUX

The 4-bit ALU determines the task to be performed using a 4:1 MUX, as seen in Figure 10. A 4:1 multiplexer operates based on the selection inputs S0 and S1. It features four inputs and produces only one outcome at a time.

Figure 11 demonstrates the 4-bit hybrid adder. The CNTFET implementation of 4-bit ALU is demonstrated in Figure 11.

5. Results and Discussion

The 4-bit Arithmetic Logic Unit (ALU) circuit has been effectively constructed and tested using CADENCE virtuoso software, using the Stanford - CNTFET computational parameters specified in Table 2.

Table 2. Simulation parameters in CNTFET

Name of the Parameter	Value
Technology of CMOS (nm)	32
Technology of CNTFET (nm)	32
CNTFET Model	Stanford
MOSFET Model	PTM
Mean Path (L_{geff})	2e-07
CNTFET Channel Length ($L_{g)}$	3.2e-08
Gate Oxide Thickness (Tox)	4e-09
Chiral Value (n1,n2)	(19,0)
The Dielectric Constant of Gate Oxide (K_{gate})	16
Temperature during Simulation	27 ^{0}C
Number of Carbon Nanotubes (CNTops)	1

Figures 12 and 13 illustrate the transient computational outcomes of the recommended 4-bit adder and subtractor accordingly. Figure 14 illustrates the transient evaluation of an AND gate. The output will remain at logic one only if both of the inputs, A and B, are logic one; otherwise, it will be logic zero. Figure 15 illustrates the transient evaluation of an OR gate. If both inputs, A as well as B, are set to logic zero, the output will also remain at logic zero. Otherwise, the output will be set to logic one.

Figure 16 illustrates the transient computation outcomes of the recommended full-swing 4x1 MUX. The calculation inputs, i0, i1, i2, i3, and the selection inputs, S1 and S0, are displayed in Figure 16. The resultant signal, y, exhibits a characteristic where it swings fully. If the choice of input S has been assigned as logic 00, subsequently, input i0 becomes connected to output y. Whenever the value of S is configured to 01, then the input signal i1 becomes connected to the output y. When the value of S has been set to 10, the input i2 becomes connected to the output y. Alternatively, the input i3 would be connected to the output y.

Table 3 presents a comparison of the performance between the proposed Carbon Nanotube Field-Effect Transistor (CNTFET) Arithmetic Logic Unit (ALU) and the CMOS ALU. The ALU simulation takes place using a supply voltage of 1V. The present investigation examines different metrics for evaluating the effectiveness of the proposed solutions and compares them to the most advanced methods currently available.

Power utilisation, delay, and the power-delay product are all critical factors to take into account. CNTFET technology demonstrates notable reductions in power usage, propagation delay, and Power-Delay Product (PDP) when compared to CMOS counterparts. The simulations have been conducted using a 32 nm technological node using CADENCE SPECTRE. The changes in power utilisation, delay, as well as PDP with regard to the supply voltage and variation in the temperature, are compared in Tables 3 and 4.

In CMOS technology, power consumption rises in proportion to the temperature. Increased temperatures lead to a rise in current leakage, which is influenced by the degree of concentration of minority carriers. Consequently, power usage rises as temperature rises. Nevertheless, CNT-based ALU maintains comparatively stable power utilization because of the exceptionally low resistivity within the carbon nanotube channel, decreased parasitic capacitance, a one-dimensional ballistic transport, and lesser leakage current within CNT-based designs.

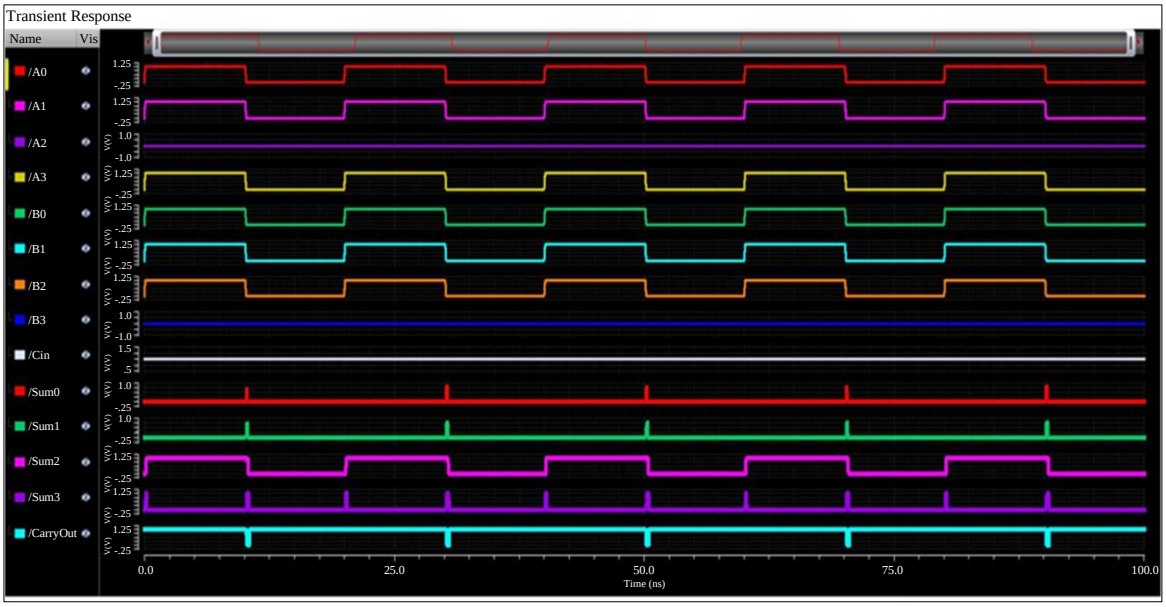

Fig. 12 Transient simulation of 4-bit hybrid adder

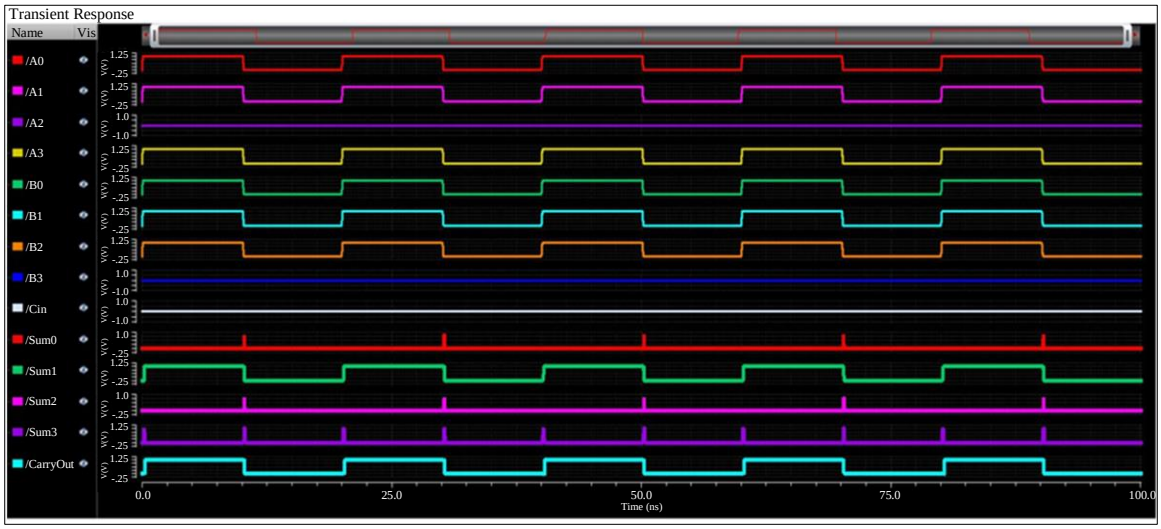

Fig. 13 Transient simulation of 4-bit hybrid Subtraction

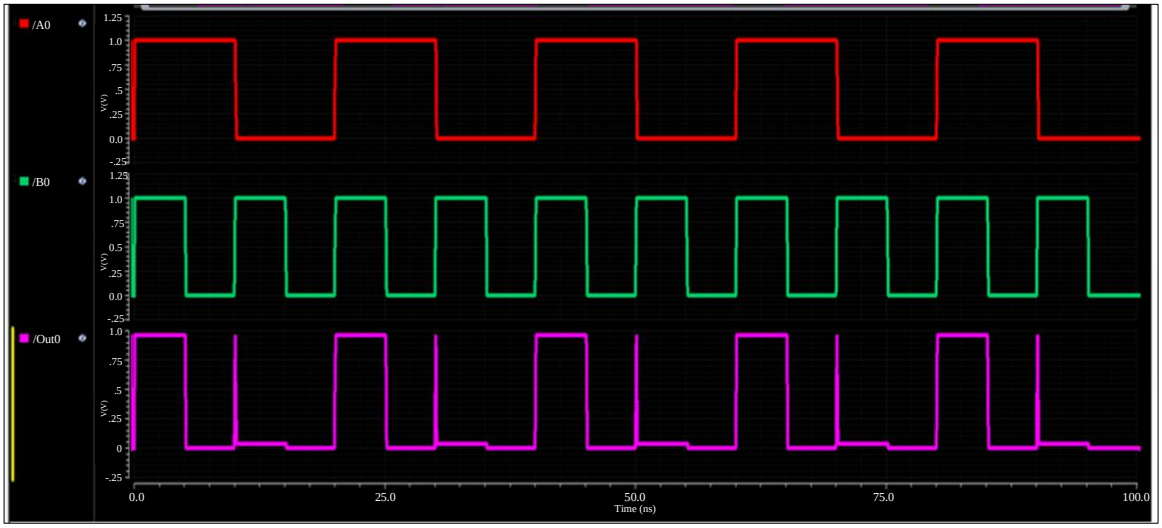

Fig. 14 Transient simulation of AND gate

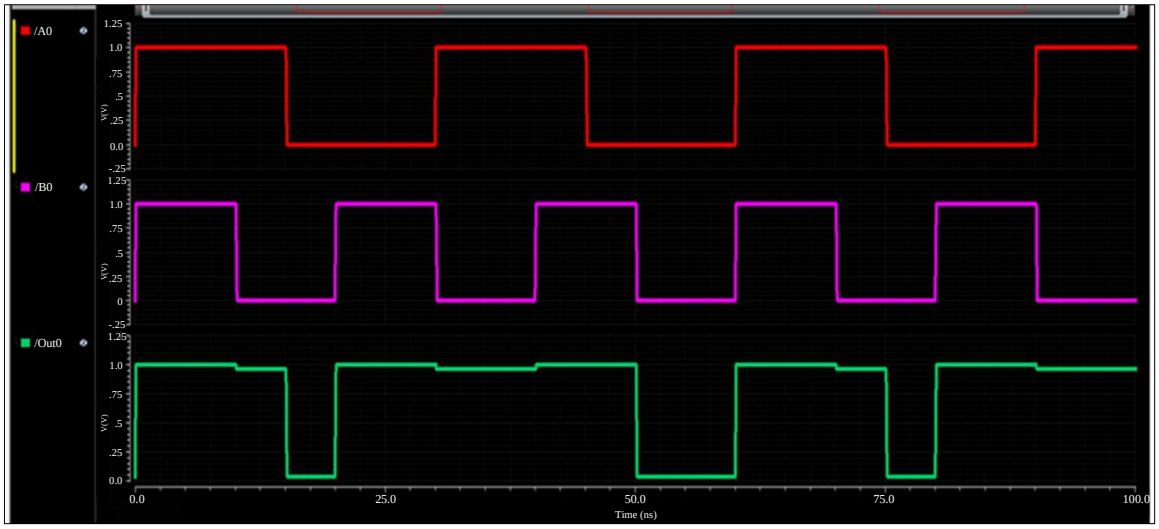

Fig. 15 Transient simulation of OR gate

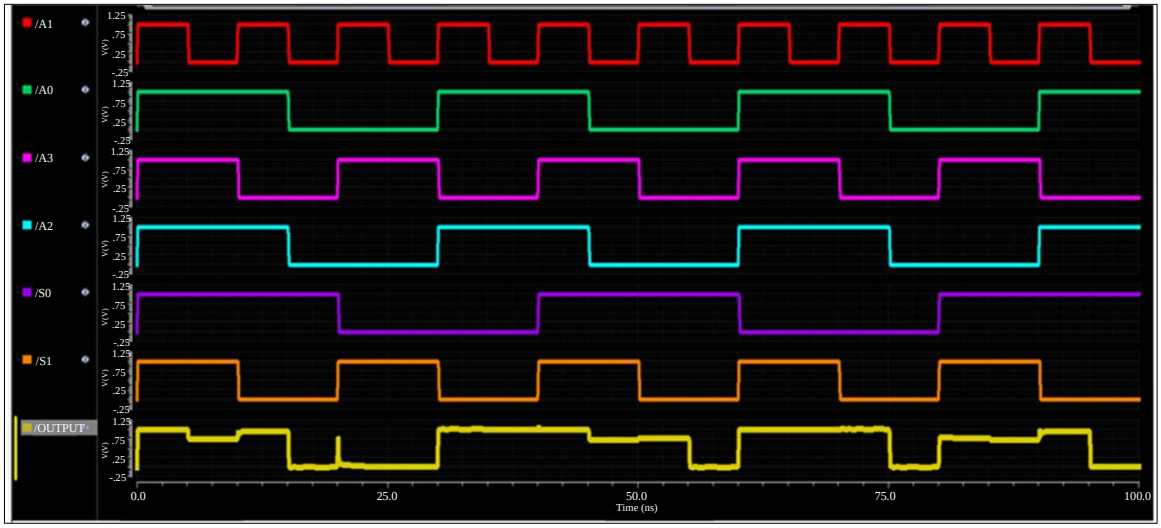

Fig. 16 Transient simulation of 4x1 MUX

Table 3. Variation of ALU output parameters w.r.t. supply voltage

Source Voltage (V)	CNTFET			CMOS		
	Power Usage in µW	Delay in nS	PDP (x 10^{-15}) in Ws	Power Usage in µW	Delay in nS	PDP (x 10^{-15}) in Ws
0.8	30.77	19.21	591.09	46.87	33.57	1573.42
0.9	32.94	18.32	603.46	48.72	32.34	1575.60
1	34.98	16.89	590.81	51.68	31.02	1603.11
1.1	36.15	15.19	549.11	53.71	29.93	1607.54
1.2	38.91	13.73	534.23	56.83	28.31	1608.85

Table 4. Variation of ALU output parameters w.r.t. change in temperature

Temperature Variation (°C)	CNTFET			CMOS		
	Power Usage in µW	Delay in nS	PDP (x 10^{-15}) in Ws	Power Usage in µW	Delay in nS	PDP (x 10^{-15}) in Ws
-25	30.67	14.81	454.22	41.67	24.37	1015.49
0	32.17	15.64	503.13	45.73	26.73	1222.36
25	34.98	16.89	590.81	51.68	31.02	1603.11
50	36.81	18.32	674.35	56.09	36.06	2022.60
75	34.98	19.91	696.45	59.18	40.52	2397.97

Figures 17 and 18 depict the influence of supply voltage and temperature on the power consumption and Delay of CMOS, as well as the recommended CNTFET-dependent ALU, respectively. The Delay associated with a CMOS adder increases as temperature rises. The Delay of a CNTFET ALU, as well as the Delay of a CMOS circuitry, remains generally constant, although the Delay of the CNTFET ALU is significantly smaller. This discrepancy becomes more evident at higher temperatures. The statistics demonstrated in Figures 17 and 18, respectively illustrate a clear and direct relationship between power utilization and source voltage. Nevertheless, the enhancement associated with the CNTFET ALU has become less significant when compared to the CMOS equivalent. The latency associated with the CNTFET ALU can frequently be much less than that of the conventional CMOS equivalent.

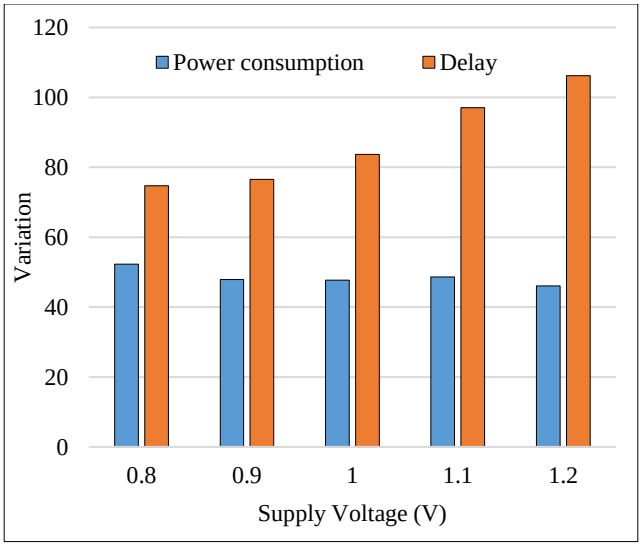

Fig. 17 Variation in ALU parameters w.r.t supply voltage using CMOS and CNTFET

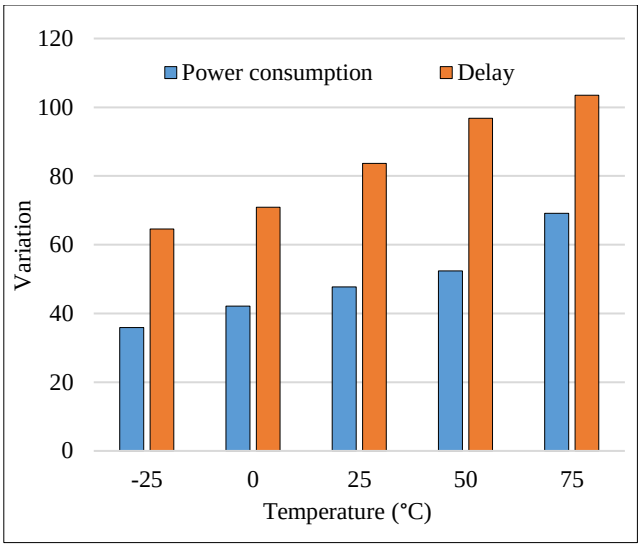

Fig. 18 Variation in ALU parameters w.r.t temperature using CMOS and CNTFET

6. Conclusion

This study suggests an acceptable design for an Arithmetic Logic Unit (ALU) that employs CNTFET along with CMOS technologies. In contrast to CMOS circuits, an analysis of comparison has been conducted to assess the hurdles and effectiveness of employing CNTFET technology in the development of nano-electronic circuitry. The results demonstrate that an ALU constructed from Carbon Nanotubes (CNT) functioned better than their counterparts, depending on CMOS technology in terms of power usage, latency, and Power-Delay Product (PDP).

Table 2 shows that the CNTFET ALU has a 46% lower power usage and a 74% shorter latency compared with the CMOS counterpart of the ALU. This improvement is observed throughout a supply voltage range of 0.8V to 1.2V. In the course of the operating temperature spectrum of -25°C to 75°C, the CNTFET adder exhibits a 35% reduction in power utilisation and a 64% reduction in latency in comparison to the CMOS equivalent that contains the ALU, as illustrated in Table 3. CNTFET has become a viable alternative to CMOS in the development of nano-electronic components, as indicated by the statistics discussed above.

References

[1] S. Seyedi, and N.J. Navimipour, "Designing a New 4: 2 Compressor Using an Efficient Multi-Layer Full-Adder Based on Nanoscale Quantum-Dot Cellular Automata," *International Journal of Theoretical Physics*, vol. 60, pp. 2613-2626, 2021. [CrossRef] [Google Scholar] [Publisher Link]

[2] Takamoto Watanabe, "All-Digital VCO-ADC TAD Using 4CKES-Type in 16-nm FinFET CMOS for Technology Scaling with Stochastic-ADC Method," *2021 28th IEEE International Conference on Electronics, Circuits, and Systems (ICECS)*, Dubai, United Arab Emirates, pp. 1-4, 2021. [CrossRef] [Google Scholar] [Publisher Link]

[3] A.A. Sujata, and Y.S. Lalitha, "Survey on Latest FinFET Technology and its Challenges in Digital Circuits and IC's," *International Journal of Electronics Engineering*, vol. 10, no. 2, pp. 577-585, 2018. [Google Scholar] [Publisher Link]

[4] Masoomeh Tirgar Fakheri, Keivan Navi, and Mohammad Tehrani, "A Novel Device to Implement Full Set of Three-Input Logic Gates Using a Naphthalene-Based Single-Molecule Field-Effect Transistor," *IEEE Transactions on Electron Devices*, vol. 68, no. 2, pp. 733-738, 2021. [CrossRef] [Google Scholar] [Publisher Link]

[5] P. Saritha et al., "4-Bit Vedic Multiplier with 18nm FinFET Technology," *2020 International Conference on Electronics and Sustainable Communication Systems (ICESC)*, Coimbatore, India, pp. 1079-1084, 2020. [CrossRef] [Google Scholar] [Publisher Link]

[6] Wei-Xiang You, Pin Su, and Chenming Hu, "Evaluation of NC-FinFET Based Subsystem-Level Logic Circuits," *IEEE Transactions on Electron Devices*, vol. 66, no. 4, pp. 2004-2009, 2019. [CrossRef] [Google Scholar] [Publisher Link]

[7] Ayushi, and Kailash Chandra, "Low Power and High Speed Mutliplier Deisgns Using FinFET Technology," *International Journal of Advanced Research in Computer and Communication Engineering*, vol. 7, no. 2, pp. 143-146, 2018. [CrossRef] [Publisher Link]

[8] Mahdieh Nayeri, Peiman Keshavarzian, and Maryam Nayeri, "High-Speed Penternary Inverter Gate Using GNRFET," *Journal of Advances in Computer Research*, vol. 10, no. 2, pp. 53-59, 2019. [Google Scholar] [Publisher Link]

[9] Nandhaiahgari Dinesh Kumar, Rajendra Prasad Somineni, and CH Raja Kumari, "Design and Analysis of Different Full Adder Cells Using New Technologies," *International Journal of Reconfigurable and Embedded Systems*, vol. 9, no. 2, pp. 116-124, 2020. [CrossRef] [Google Scholar] [Publisher Link]

[10] Sina Bakhtavari Mamaghani, Mohammad Hossein Moaiyeri, and Ghassem Jaberipur, "Design of an Efficient Fully Nonvolatile and Radiation-Hardened Majority-Based Magnetic Full Adder Using FinFET/MTJ," *Microelectronics Journal*, vol. 103, 2020. [CrossRef] [Google Scholar] [Publisher Link]

[11] N. Hajizadeh Bastani, and K. Navi, "Imprecise Minority-Based Full Adder for Approximate Computing Using CNFETs," *International Journal of Nanoscience and Nanotechnology*, vol. 15, no. 4, pp. 239-248, 2019. [Google Scholar] [Publisher Link]

[12] M. Aalelai Vendhan, and S. Deepa, "Investigations on Performance Metrics of FINFET Based 8-Bit Low Power Adder Architectures Implemented Using Various Logic Styles," *Indian Journal of Science and Technology*, vol. 11, no. 24, pp. 1-22, 2018. [CrossRef] [Google Scholar] [Publisher Link]

[13] Masoud Mahjoubi et al., "Two Efficient Ternary Adder Designs Based on CNFET Technology," *Journal of Computer and Knowledge Engineering*, vol. 4, no. 7, pp. 25-34, 2021. [CrossRef] [Google Scholar] [Publisher Link]

[14] Farzin Mahboob Sardroudi, Mehdi Habibi, and Mohammad Hossein Moaiyeri, "CNFET-Based Design of Efficient Ternary Half Adder and 1-Trit Multiplier Circuits Using Dynamic Logic," *Microelectronics Journal*, vol. 113, 2021. [CrossRef] [Google Scholar] [Publisher Link]

[15] Aditya Sharma, Nikhil Saxena, and Amit Singh Rajput, "Efficient and High-Performance MTCMOS Employed 34T-Full Subtractor," *Journal of Active & Passive Electronic Devices*, vol. 13, no. 1, 2018. [Google Scholar] [Publisher Link]

[16] Anju Rajput et al., "Novel CMOS and PTL Based Half Subtractor Designs," *2021 IEEE International Symposium on Smart Electronic Systems (iSES)*, Jaipur, India, pp. 165-168, 2021. [CrossRef] [Google Scholar] [Publisher Link]

[17] D. Rebecca Florance, and B. Prabhakar, "Design of FinFET and FET Based Full Adder Cell Using Multiplexer Selection Logic," *2022 4th International Conference on Smart Systems and Inventive Technology (ICSSIT)*, Tirunelveli, India, pp. 741-747, 2022. [CrossRef] [Google Scholar] [Publisher Link]

[18] Trapti Sharma, and Laxmi Kumre, "CNTFET-Based Design of Ternary Arithmetic Modules," *Circuits, Systems, and Signal Processing*, vol. 38, pp. 4640-4666, 2019. [CrossRef] [Google Scholar] [Publisher Link]

[19] Endri Taka et al., "Process Variability Analysis in Interconnect, Logic, and Arithmetic Blocks of 16-nm FinFET FPGAs," *ACM Transactions on Reconfigurable Technology and Systems (TRETS)*, vol. 14, no. 3, pp. 1-30, 2021. [CrossRef] [Google Scholar] [Publisher Link]

[20] B.P. Bhuvana, and V.S. Kanchana Bhaaskaran, "Design of FinFET-Based Energy Efficient Pass-Transistor Adiabatic Logic for Ultra-Low Power Applications," *Microelectronics Journal*, vol. 92, 2019. [CrossRef] [Google Scholar] [Publisher Link]

[21] Pegah Zakian, and Rahebeh Niaraki Asli, "An Efficient Design of Low-Power and High-Speed Approximate Compressor in FinFET Technology," *Computers & Electrical Engineering*, vol. 86, 2020. [CrossRef] [Google Scholar] [Publisher Link]

[22] V.M. Senthil Kumar, and S. Ravindrakumar, "Design of an Area-Efficient Finfet-Based Approximate Multiplier in 32-Nm Technology for Low-Power Application," *Soft Computing and Signal Processing*, pp. 505-513, 2019. [CrossRef] [Google Scholar] [Publisher Link]

[23] Rashmit Patel, Yash Agrawal, and Rutu Parekh, "A Novel Slice-Based High-Performance ALU Design Using Prospective Single Electron Transistor," *IETE Journal of Research*, vol. 68, no. 2, pp. 1115-1124, 2022. [CrossRef] [Google Scholar] [Publisher Link]

[24] N. Shylashree et al., "Design and Analysis of High-Speed 8-Bit ALU Using 18 nm FinFET Technology," *Microsystem Technologies*, vol. 25, pp. 2349-2359, 2019. [CrossRef] [Google Scholar] [Publisher Link]

[25] J. Jency Rubia, and R. Babitha Lincy, "Design of Low Power 4 Bit ALU Using 32nm FinFET Technology," *International Journal of Pure and Applied Mathematics*, vol. 120, no. 6, pp. 8089-8100, 2018. [Publisher Link]

[26] D. Rebecca Florance, B. Prabhakar, and Manoj Kumar, "Design and Implementation of ALU Using Graphene Nanoribbon Field-Effect Transistor and Fin Field-Effect Transistor," *Journal of Nanomaterials*, 2022. [CrossRef] [Google Scholar] [Publisher Link]

[27] Erfan Abbasian, and Mahdieh Nayeri, "A High-Speed Low-Energy One-Trit Ternary Multiplier Circuit Design in CNTFET Technology," *ECS Journal of Solid State Science and Technology*, vol. 12, 2023. [CrossRef] [Google Scholar] [Publisher Link]

[28] Shams Ul Haq et al., "Energy-Efficient High-Speed Dynamic Logic-Based One-Trit Multiplier in CNTFET Technology," *International Journal of Electronics and Communications*, vol. 175, 2024. [CrossRef] [Google Scholar] [Publisher Link]

[29] Joevonte Kimbrough et al., "Dielectrophoresis-Based Positioning of Carbon Nanotubes for Wafer-Scale Fabrication of Carbon Nanotube Devices," *Micromachines*, vol. 12, no. 1, pp. 1-12, 2020. [CrossRef] [Google Scholar] [Publisher Link]

[30] Toshiaki Natsuki, "Carbon Nanotube-Based Nanomechanical Sensor: Theoretical Analysis of Mechanical and Vibrational Properties," *Electronics*, vol. 6, no. 3, pp. 1-20, 2017. [CrossRef] [Google Scholar] [Publisher Link]

[31] Felix Obite, Geoffrey Ijeomah, and Joseph Stephen Bassi, "Carbon Nanotube Field Effect Transistors: Toward Future Nanoscale Electronics," *International Journal of Computers and Applications*, vol. 41, no. 2, pp. 149-164, 2019. [CrossRef] [Google Scholar] [Publisher Link]

[32] S.S. Alabsi et al., "A Review of Carbon Nanotubes Field Effect-Based Biosensors," *IEEE Access*, vol. 8, pp. 69509-69521, 2020. [CrossRef] [Google Scholar] [Publisher Link]

[33] Furqan Zahoor et al., "Carbon Nanotube Field Effect Transistor (CNTFET) and Resistive Random Access Memory (RRAM) Based Ternary Combinational Logic Circuits," *Electronics*, vol. 10, no. 1, pp. 1-20, 2021. [CrossRef] [Google Scholar] [Publisher Link]

[34] Mohammad Hossein Moaiyeri et al., "A Universal Method for Designing Low-Power Carbon Nanotube FET-Based Multiple-Valued Logic Circuits," *IET Computers & Digital Techniques*, vol. 7, no. 4, pp. 143-189, 2013. [CrossRef] [Google Scholar] [Publisher Link]