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Original Article

Realization of Trinary Asymmetrical Nine Level Reduced Switch Count Multi Level Inverter

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Abstract *- The popularity of Multilevel Inverters (MLIs) for obtaining high-power conversion due to their low voltage stress across power switches and low total harmonic distortion in output voltage waveform has emerged enormously. Thus, a trinary asymmetrical module based 9-level RSC-MLI is proposed in this work. By the replacement of a few bidirectional switches with unidirectional switches, the number of semiconductor devices is reduced. Due to this, voltage stress across each switch is reduced. In addition to this low Total Harmonic Distortion and improved efficiency with Zero Voltage Switching operation. The ease of control and implementation is assessed using a reduced carrier pulse width modulation technique, which overcomes limitations of other schemes such as the number of carriers, number of comparators, and total harmonic distortion. Additionally, the superiority of the proposed asymmetrical module over the literature reported is evidenced based on switching losses, redundancy and efficiency. Simulation is carried out on MATLAB/SIMULINK R2020(b). Finally, the simulation results demonstrate the reliability of the proposed design.*

Keywords *- Alternate phase disposition, In phase disposition, Cascaded H-Bridge, Flying Capacitor, Multilevel Inverter, Opposite phase disposition, Reduced switch count, Phase shifted pulse width modulation.*

1. Introduction

Multilevel Inverter (MLI) as its invention has grown the demand rapidly. It is a key technology which plays an important role in different applications such as AC motor drives, uninterruptible power supplies, electric and hybrid electric vehicles and integration high-voltage DC power transmission, flexible AC transmission systems, static VAR compensators, active filters, and utilisation of renewable energy sources [1, 2]. MLI is gaining popularity in terms of both architecture and control scheme because of its high power quality, low Total Harmonic Distortion (THD), and low voltage stress across the switches with low electromagnetic compatibility and low switching losses as well as high dv/dt protection [3, 4].

MLIs are often categorized as Neutral Point Clamped (NPC), Flying Capacitor (FC), and Cascaded H-Bridge (CHB). An NPC MLI has negative aspects such as limited flexibility, high clamping diode requirements, uneven power distribution, switch deployment, and unbalanced voltages. The main constraints of FC MLI include balancing capacitor charges at low switching frequencies and the need for excessive clamping capacitors. CHB MLIs have drawbacks, such as the necessity for remote DC supply for each H-bridge module, which may substantially boost the overall cost of the design. Several H-bridge cells, each with its own DC power source, comprise the CHB MLI. The term “Cascaded H-Bridge (CHB) MLI” refers to cascading MLI using H-bridge cells.

CHB has attracted more attention among conventional MLIs because of its modularity and simplicity; however, an isolated source's necessity is a topology drawback [5-9]. However, MLI possess some imperfections, such as an increment of the number of levels, a reduction in the number of semiconductor devices that compensate for the complexity of the overall system, and cost-effectiveness, which affects the efficiency and reliability of the system. The number of driver circuits, isolation circuits, heat sinks, and protection requirements increases as the number of levels of these MLIs goes up. Researchers are focusing more on creating various topologies that aim to reduce the number of switches while increasing output levels. Therefore, the outcome is the implementation of Reduced Switch Count MLI (RSC MLI) topologies. The increased switch count further increases the computational burden on the controller [10].

The RSC-MLI configurations are categorized as symmetric or asymmetric. When in a symmetric configuration, the magnitudes of DC sources are equal. In the asymmetric configuration, the magnitude of DC sources is unequal due to which higher levels are generated, low

installation is obtained and more economical, and the result is highest efficiency [11]. Extreme research has been done on RSC-MLIs recently, and various topologies with notable reductions in component count, total blocking voltage, cost, and controllability have been produced. The main drawback arises due to unidentical stress on the switches.

The higher voltage stress is experienced by switches connected to the highest input DC voltage than by switches connected to the minimum input DC voltage. Fluctuation of switch temperatures is due to unequal loss sharing among switches [12, 13]. The realization of topologies could be done using different control schemes. The choice of appropriate implementation of the PWM scheme is highly important in acquiring desired voltage levels with the lowest number of switches.

Among the PWM techniques published for MLIs, the most common schemes with the simplest switching logic are carrier-based PWM schemes such as Level Shifted PWM (LSPWM) and Phase Shifted PWM (PSPWM) [14]. For different RSC-MLIs, several carrier-based PWM techniques, such as multi-reference, switching-function, and switching-function schemes, have been revealed [15]. The objective of a modulation signal is to generate a stepped waveform that is the most exact replica of a certain reference signal possible. Reduced carrier PWM uses a modified modulating signal and carrier signal arrangement to provide a staircase, followed by a look up table to produce the required switching action [16].

An extensive review of the literature reported shows that the popular asymmetrical topologies offering a good reduction in switch count are unit-based configurations designed for a specific level. The popular 9-level RSC-MLI reported with trinary voltage ratios synthesizes DC sources, produces 9-levels and offers an appreciable reduction in switch count.

The corresponding switching process, however, creates a built-in short circuit across one of the DC sources, resulting in a distorted output voltage waveform. An objective is to resolve the issue [17]. A proposed trinary voltage module comprising an H-Bridge T-type structure, DC voltage sources in the ratio 1:3, including a number of bidirectional and unidirectional switches, is intended to produce 9 levels. Its switching operation is realized with the simplified switching function PWM, which is popularly reported for asymmetrical RSC-MLI configuration.

The paper is formulated as follows: Section 2 outlines the trinary voltage module design and its operating modes. In Section 3, the modulation strategy being used is demonstrated, and Section 4 presents the simulation results and comparative performance of the topological features of the proposed configuration and conventional topologies. Further, conclusion and references are presented.

2. Proposed Trinary Voltage Module

The replacement of a few switches with IGBTs in conjunction with a snubber circuit has arisen as an approach to prevent such interrupted output voltages. The replaced switch exhibits infinite impedance over it in the off state. The proposed architecture combines bidirectional and unidirectional switches without changing the switch count, but a drastic change in device ratings could be noticed. The proposed topology is advantageous as it operates with less conduction losses and high switching speed. In order to achieve nine phase voltage levels from +40v to -40v, two trinary (1:3) DC sources in each phase are required. The H-Bridge structure in topology plays the role of polarity changer, and the remaining switches are responsible for boosting the sharpness of output voltage. The triggering of switches in bridge structures Sa2–Sa3 and Sa1–Sa4 attained positive and negative levels, respectively.

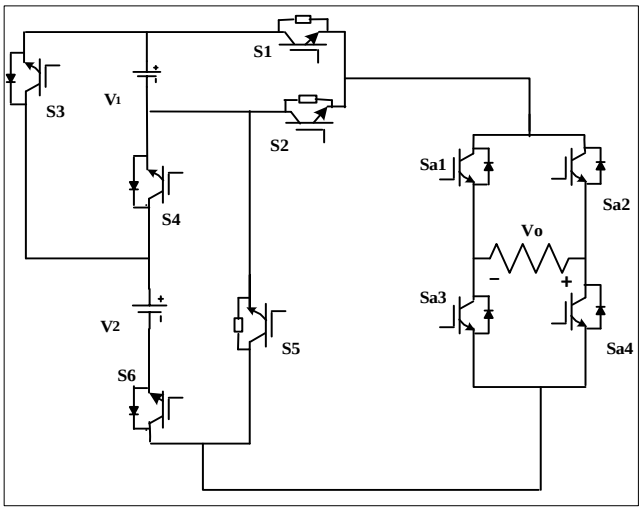


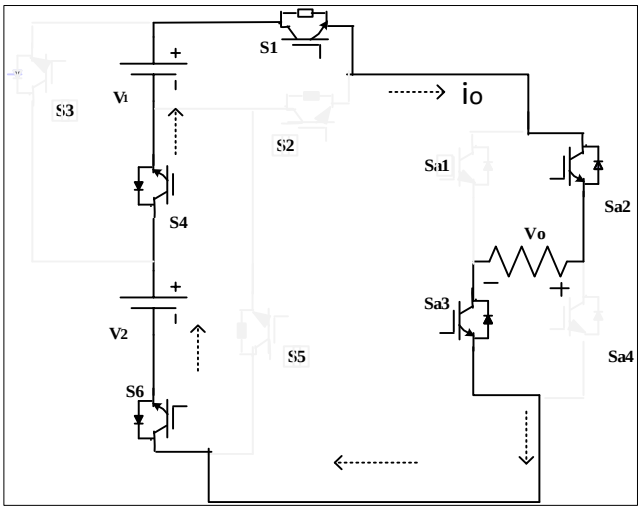
Fig. 1 Proposed topology

2.1. Operating Modes

Achieving positive levels is possible by enabling turning ON switches S_{a2} and S_{a3}. In contrast, negative levels are attained by turning ON S_{a1} and S_{a4}. An attempt to operate S_1, S_2, S_3, S_4, S_5 and S_6 switches fetches different voltage levels. The four operating modes of positive levels are shown in Figure 2 and are discussed below. The switches S_{a2} and S_{a3} are kept ON until positive levels are obtained.

Mode I: Triggering pulses provided to S_1, S_4 and S_6 turn ON IGBTs, and the achieved voltage across the load is +40V. The current flows through S_{a2}-S_{a3}-S_6-V_2-S_4-V_1-S_1, as depicted in Figure 2(a).

Mode II: In this mode, IGBTs S_1, S_3 and S_6 are turned ON, and the voltage level of +30V is attained across the load. The current direction is through S_{a2}-S_{a3}-S_6-V_2-S_3-S_1, as shown in Figure 2(b).



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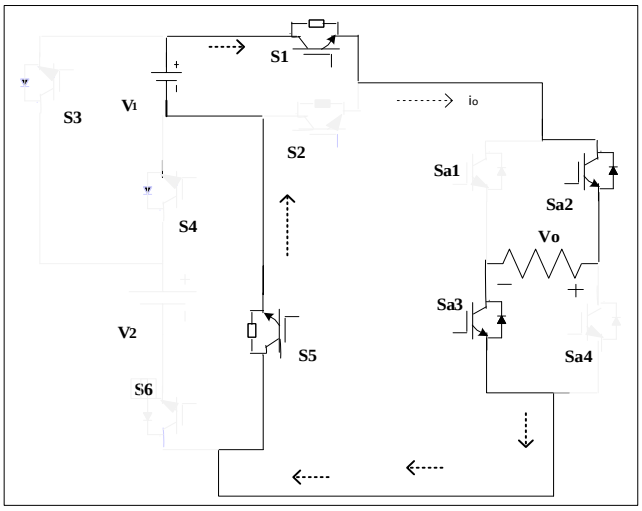

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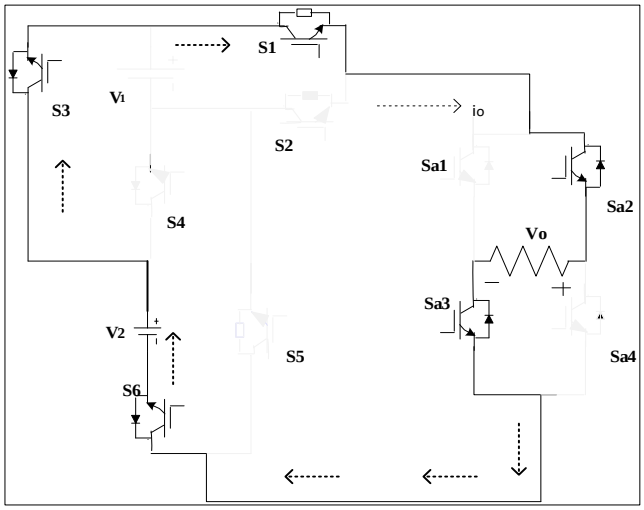
Fig. 2 Switching states for positive voltage levels



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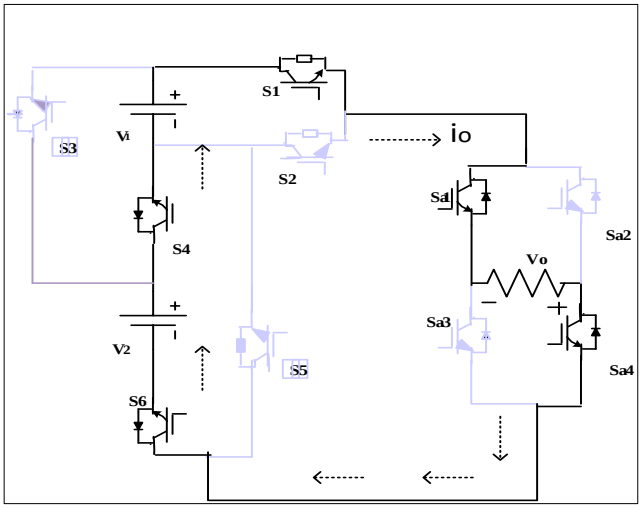

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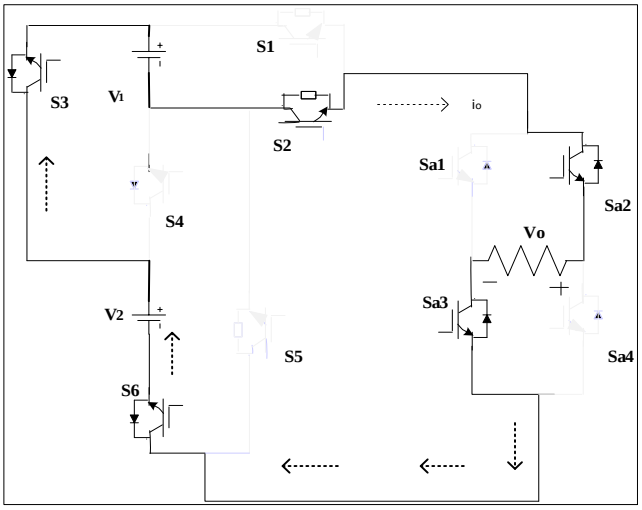

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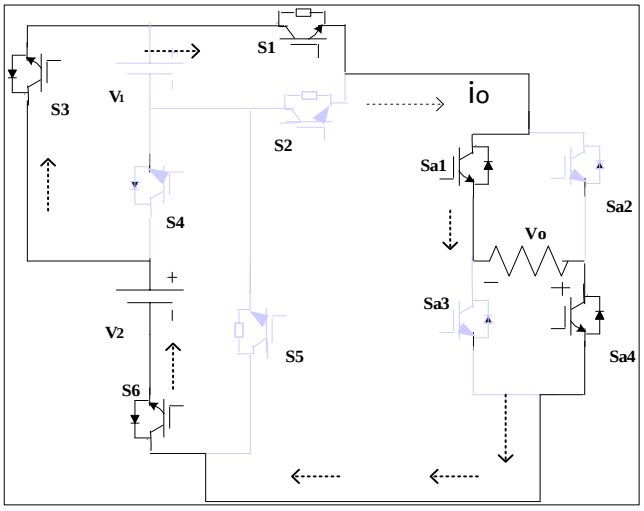

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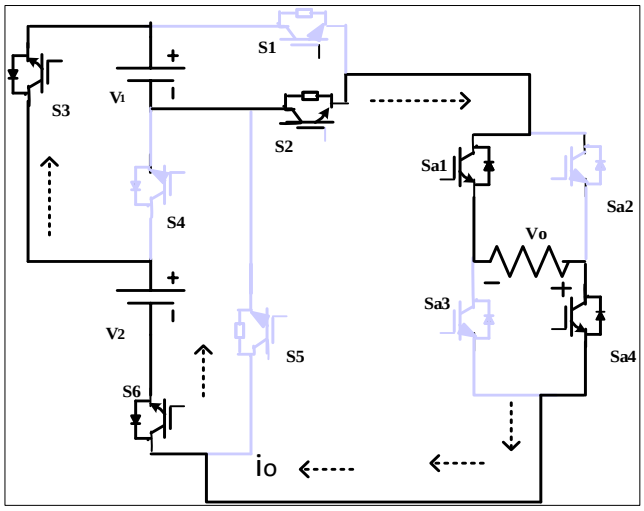

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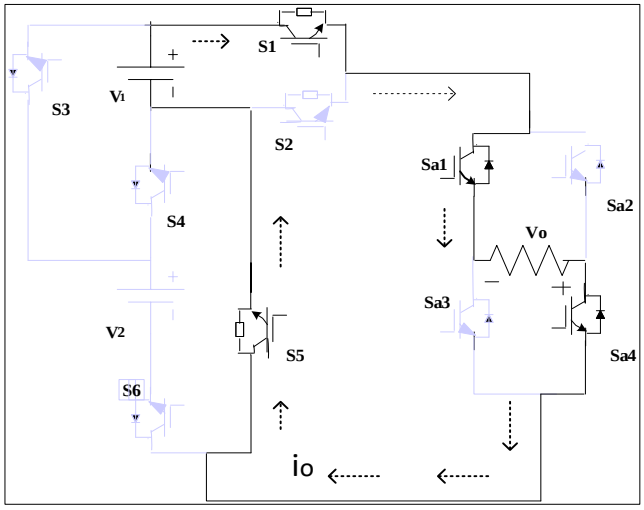


(d)

Fig. 3 Switching states for negative voltage levels

Mode III: The topology creates a voltage level of +20V during this mode. The switches S2, S3 and S6 are ON, thus, leading V0 = +20V. The current flows through Sa2-Sa3-S6-V2-S3-V1-S2, as shown in Figure 2(c).

Mode IV: The bidirectional switches S_{a2}, S_{a3}, and unidirectional switches S_1 and S_5 are triggered ON, and the remaining IGBTs are turned OFF. The load across voltage is +10V, current direction illustrated in Figure 2(d)

The switches S_{a1} and S_{a4} are kept ON till negative voltages are obtained.

Mode V: When S_1, S_4 and S_6 are triggered ON, and the voltage -40V is attained. The current flows through S_{a1}-S_{a4}-S_6-V_2-S_4-V_1-S_1, as shown in Figure 3(a).

Mode VI: This topology generates a -30V voltage level across the load during this mode. The switches S_1, S_3 and S_6 are ON, thus, leading V_0 = +20V. The current flows through S_{a1}-S_{a4}-S_6-V_2-S_3-V_1-S_1, as shown in Figure 3(b).

Mode VII: Triggering pulses provided to S_2, S_3 and S_6 turn ON IGBTs, and the achieved voltage across the load is -20V. The current flows through S_{a1}-S_{a4}-S_6-V_2-S_3-V_1-S_2, as shown in Figure 3(c).

Mode VIII: The bidirectional switches S_{a1}, S_{a4}, and unidirectional switches S_1 and S_5 are triggered ON, and the remaining IGBTs are turned OFF. The load across voltage is -10V, current direction illustrated in Figure 3(d). Table 1 displays the switching states needed to achieve the desired voltage levels for each phase.

Table 1. Various possible modes of proposed topology

Switches in Conduction		Voltage Level
S1, S4, S6	Sa2 & Sa3	V_1+V_2
S1, S3, S6		V_2
S2, S3, S6		V_2-V_1
S1, S5		V_1
-	-	0
S1, S5	Sa1 & Sa4	-V_1
S2, S3, S6		-(V_2-V_1)
S1, S3, S6		-V_2
S1, S4, S6		-(V_1+V_2)

The proposed topology results in reduced complexity of the circuit as well as it is economical. However, an unequal voltage source necessitates switching switches with lower ratings.

2.2. Topological Comparison

A comparative study among topologies observed in literature regarding the number of bidirectional devices, unidirectional devices, protective branches, and DC sources proves that the proposed topology has fewer switching losses, is more protective against overcurrents, and is reliable in nature. Comparative analysis is performed among present work and conventional topologies for desired output based on the number of switches, diodes, DC connections, and overall component count, as shown in Table 2.

Table 2. Comparison of other topologies and proposed topologies

Components Count	[17]	[25]	[26]	[27]	Proposed Topology
IGBTs	10	16	16	16	10
Diodes	10	9	16	16	7
Snubber Capacitors	0	0	0	0	3
DC Sources	2	4	7	4	2

3. Modulation Techniques

The performance of the proposed configuration is determined by both the number of switches and the modulation mechanism. To ensure the wellness of topological performance in achieving the required voltage levels, modules are realized or implemented using the appropriate PWM control. However, appropriate switching action and modulation schemes are required to achieve these output levels.

The most common carrier configuration reported for conventional MLIs is the multicarrier PWM [18-20] type, which uses either (n-1) or (n-1)/2 level shifted or phase shifted carrier arrangement to drive an "n-level" inverter. Both Level Shifted (LSPWM) [21] and Phase Shifted (PSPWM) are observed as the most common carrier arrangements with (n-1) carriers. LSPWM is divided into three sub-categories: IPD, OPD, and APOD. It involves identical carriers placed at shifted DC levels. PSPWM involves identical carriers with 360/(n-1) successive phases of delay [22]. LSPWM-IPD is often used for three-phase inverters due to its excellent harmonic spectra at line voltage. However, conventional PWM schemes are suitable only for MLIs as they conduct switches at lower and higher levels.

The realization of RSC-MLI needs an improved version of the PWM technique. Thus, a carrier-based PWM technique is the most straightforward and commonly used documented PWM technique. An initial category of carrier based PWM method is multi reference scheme. In accordance with the topological structure, switching pulses are generated by comparing a number of reference signals with a modulating signal.

Despite these arrangements, this strategy yields inefficient THD performance. It is efficient for limited topologies such as T-type and extended T-type configurations, but when applied to any RSC-MLI, it leads to poor total harmonic distortion in line voltage. A switching function PWM scheme is the other category of PWM technique. This scheme creates switching pulses by integrating each carrier's minimum and maximum limits.

In this scheme, realization is done by using plenty of comparators. However, the system becomes complex. Reduced Carrier PWM scheme is another prominent scheme comprising half the number of carriers compared with the former PWM scheme, and the modulating signal is a rectified sinusoidal pattern. The comparison of the signals as mentioned above yields switching pulses according to the switching logic of the configuration.

This study selects the reduced carrier scheme above all other carrier-based PWM schemes because it is simpler and improves THD performance at line voltages. Furthermore, reducing the number of carriers yields a reliable, efficient pulse width modulation scheme [23-27]. To obtain n number of levels, the number of carriers used in this technique are (n-1)/2 with frequency and amplitude assumed as fo and Xo, respectively. The modulating signal frequency and amplitude are fm and Xm, respectively.

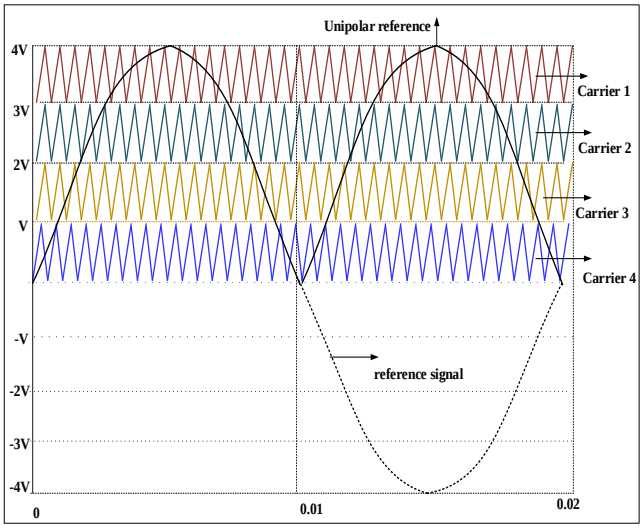


Fig. 4 Reduced carrier PWM

$$\text{Frequency modulation index } m_f = \frac{f_o}{f_m} \quad (1)$$

$$\text{Amplitude modulation index } m_f = \frac{2Xm}{(m-1)X_o} \quad (2)$$

This scheme compares unified modulating and reference signals, creating the switching pulses. These pulses offer positive voltage levels for the positive half of the modulating signal and negative voltage levels for the negative half.

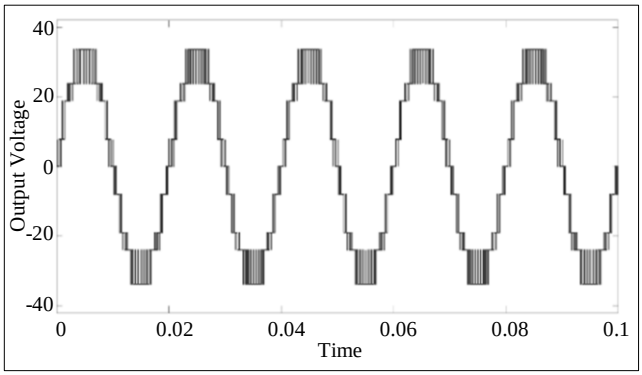
4. Simulation Results and Analysis

The performance of the proposed structure is investigated and verified using the MATLAB/ SIMULINK program. The execution of the designed configuration is registered for different loads. This section demonstrates the simulation of proposed inverter topologies for their expressed state of the art in order to evaluate the ability of the MLI and RSC-MLIs in addition to their PWM schemes. The parameters considered for analysing the proposed topology are tabulated in Table 3. Figure 5 depicts the simulation outcomes of 9 level output voltage waveforms and output current waveforms. The operation of IGBTs exploited in the proposed topology is shown in Figure 6. The harmonic spectra of output quantities at different values of amplitude modulation index ma=0.98 are depicted in Figure 7. Figure 8 shows the ZVS performance of topology.

According to observation from simulation results, it is worth noting that the proposed topology is advantageous over the conventional model as it uses fewer semiconductor devices, which reduces conduction losses and obtains appreciation in the values of total harmonic distortion. It is also observed that using the zero voltage switching concept leads to diminished switching losses and lessened voltage ratings of semiconductor devices.

Table 3. Simulation parameters of the proposed topology

	Component/Parameter	Specification
Control Circuit	Carrier Frequency(f_{cr})	2000Hz
	Modulating Frequency	50HZ
	Amplitude Modulation Index (m_a)	0.98
Power. Converter/ Inverter (IGBT Details)	Collector to Emitter Voltage (V_{CE})	1000V
	Collector current (I_C)	30A
	Internal Resistance (R_{on})	1 mΩ
DC Input Voltage (V_1) DC Input voltage (V_2)		10V 30V



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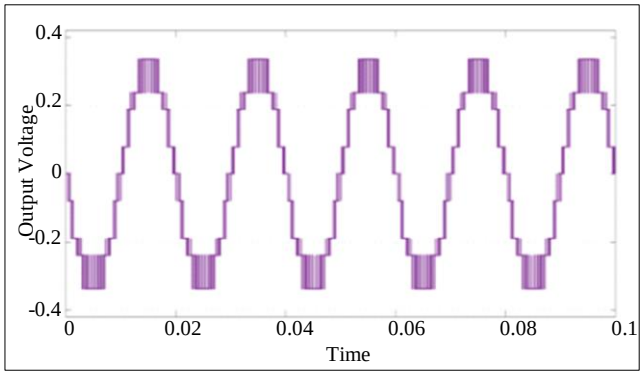
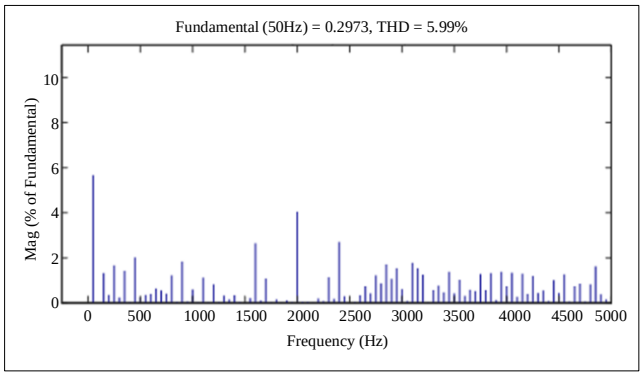


(b)

Fig. 5 (a) Output voltage waveform, and (b) Output current waveform.



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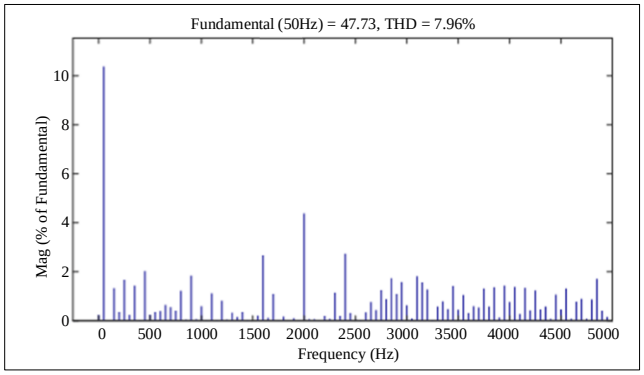
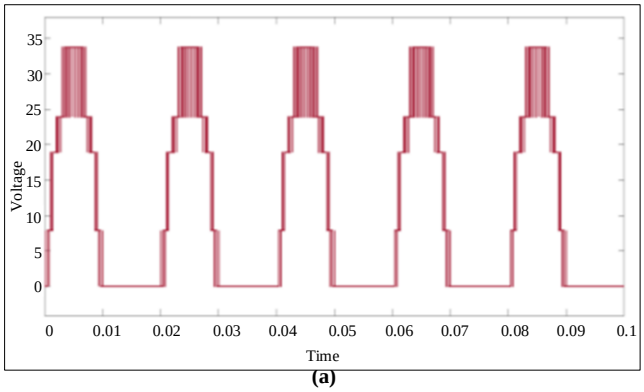


(b)

Fig. 6 At ma=0.98, Harmonic spectrum of (a) Output current, and (b) Output voltage.



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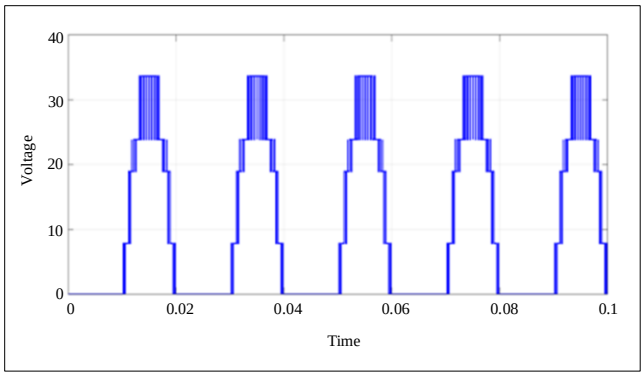

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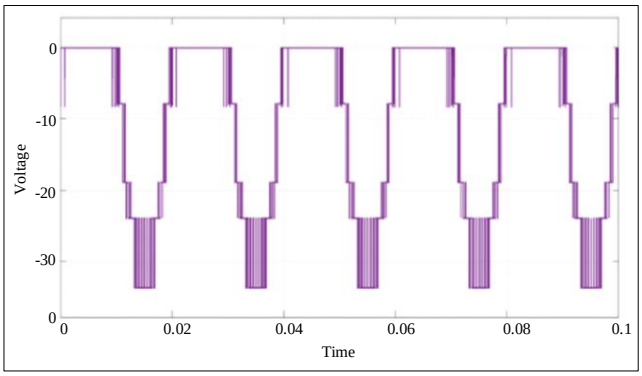

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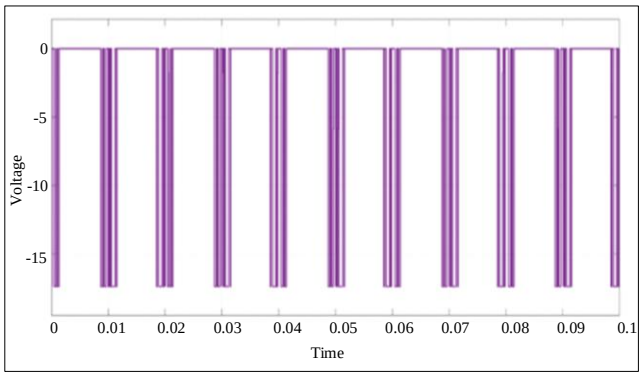

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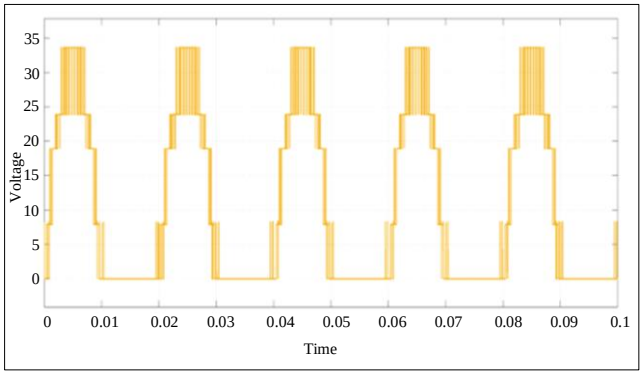

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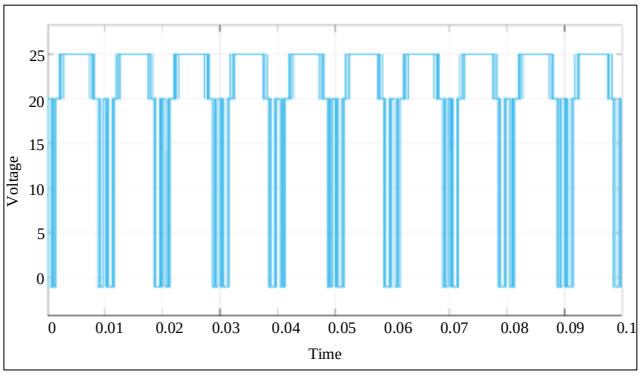

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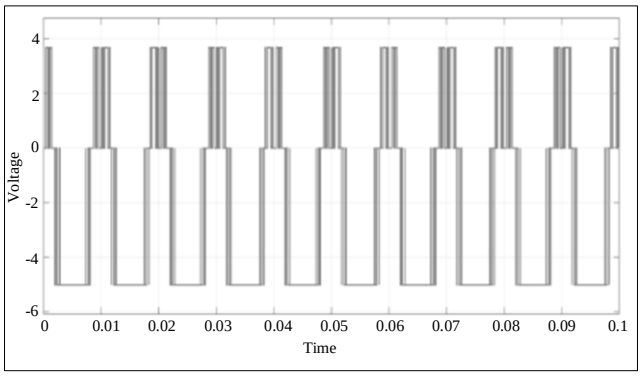

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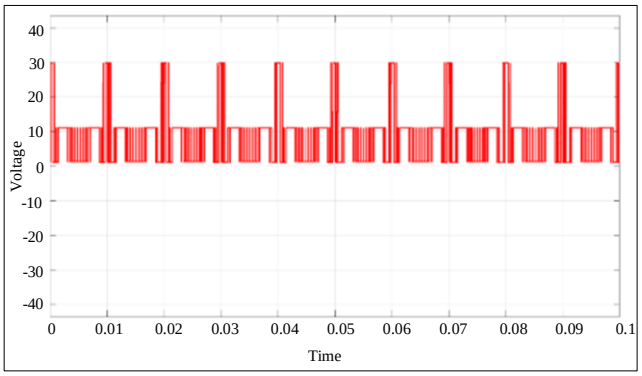

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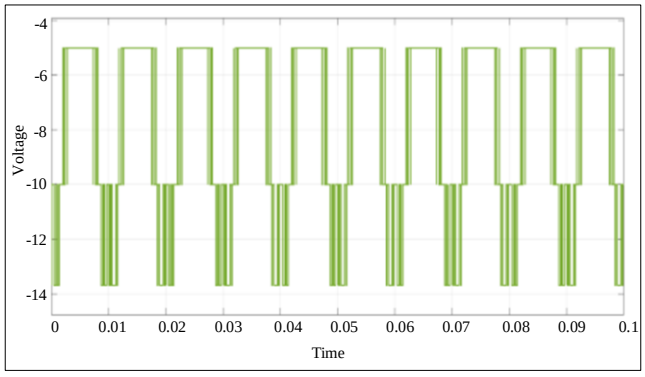

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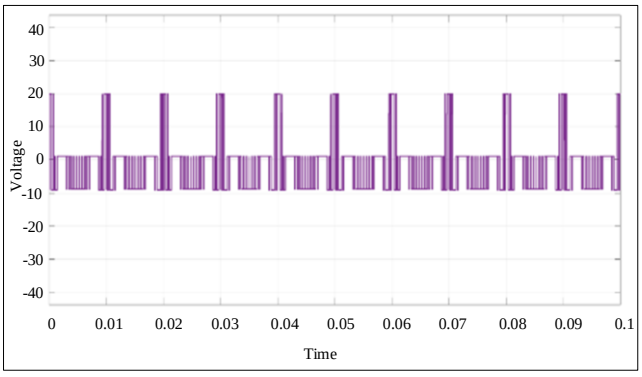

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Fig. 7 Operation of IGBTs

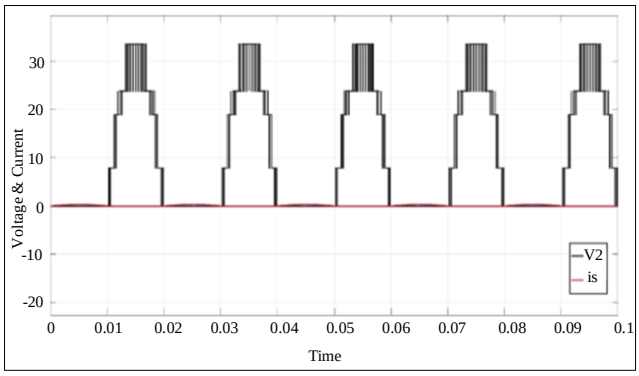

Fig. 8 ZVS waveform of output parameters

Table 4. Comparative analysis

Ref	No. of Levels	THD	ZVS	Control Method
[17]	9	9.6	Partially	LS-PWM
[25]	7	18.6	Partially	SF-PWM
[27]	7	20.1	Partially	SV-PWM
Proposed Topology	9	5.9	Fully	RC-PWM

A comparative study is performed among the proposed design and conventional topologies for desired output based on no. of levels, THD, ZVS and control method as shown in Table 4. The analysis shows that THD for the proposed topology is 5.99%, and the Zero Voltage Switching (ZVS) is achieved completely.

5. Conclusion

A trinary asymmetrical module based 9-level RSC-MLI is implemented. With the replacement of a few bidirectional switches with unidirectional switches, the number of semiconductor devices is reduced, voltage stress across each switch reduces along with this low THD, and improved efficiency with ZVS operation is achieved with the help of the LS-PWM technique.

The proposed topology provides a feasible solution to the flaws of typical multicarrier, switching function, and multi reference PWM schemes, and a reduced carrier PWM scheme is evolved. Comparative analysis performed among conventional and proposed configurations declares it economical, efficient and reliable.

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