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Original Article

Design and Analysis of High-Speed Sub-Threshold Operating Voltage Domino Logic

N. Kurumaiah[1], M. Kezia Joseph[2], P. Chandra Sekhar[3]

[1,3]*Department of E.C.E, College of Engineering, Osmania University, Telangana, India.*
[2]*Department of E.C.E, Stanley College of Engineering and Technology for Women, Telangana, India.*

[1]*Corresponding Author : kurmi4027@gmail.com*

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Abstract - *The development and application of CMOS VLSI semiconductor circuits employing sub-micron technology has faced significant challenges, specifically related to issues of latency and power usage. This paper presents the HSSODL technique, a novel approach for designing CMOS logic gates that minimize leakage current. The goal of this methodology has been to minimize energy consumption due to leakage while also improving digital circuit efficiency in terms of distortion. The suggested technique is utilized to create 16-bit OR gates, which are then simulated with Cadence's CMOS 45nm technology. The simulation results were evaluated by comparing Unity Noise Gain (UNG), power utilization, and latency. The findings from the simulation demonstrate that the suggested domino logic technique decreases the latency by a minimum of 35%. Overall, power usage and energy dissipation are lower than in contemporary domino logic techniques.*

Keywords - *CMOS, HSSOD, UNG, Power utilization, Delay.*

1. Introduction

The present investigation in digital circuits focuses on developing high-speed, low-power semiconductor devices that have decreased complexity. These investigative methodologies led to the development of portable technologies that include laptops, microprocessors, and handheld communication devices. When it comes to constructing high-speed digital devices, it is preferable to use dynamic CMOS logic instead of static CMOS logic since it consumes less Power and operates at a faster pace. As technology progresses, supply voltage decreases with the goal of reducing energy use [1].

The threshold voltage scalability is performed in conjunction with the scaling of supply voltage in order to preserve the transistor overdrive resulting from excessive ON currents. The noise sensitivity provided by domino circuits gets reduced by an insufficient voltage threshold. Moreover, as technology advances, gate oxide thickness decreases, leading to a substantial rise in current leakage through the gate. Consequently, the lowered voltage threshold and increased leakage current have a negative impact on the immunity to noise and overall strength associated with the domino circuitry [2, 3]. The Power consumed by the digital logic gate can be expressed as [4].

$$P_{\text{total power}} = P_{\text{short-circuit power}} + P_{\text{charging-discharging power}} + P_{\text{leakage power}}$$

Where,

P_{sc} - The power utilisation is short-circuited due to a shortfall connecting the power supply along with grounding.

P_{sw} - Power employed in the procedure of charging as well as discharging of circuitry capacitances.

P_{leak} - Whenever the transistors are switched off, they produce Power owing to leakage current.

When developing low-power, high-speed domino circuits, researchers investigate both dynamic and static power usage. Progressive scaling of CMOS circuitry presents many issues, including diminished short channel implications, increased leakage currents, and raised power usage [5, 6].

These issues diminish the assessed value of FOM for the CMOS circuitry. To lower numerous elements of power utilization, the dimensions of the devices and the supply of voltage with which they are supplied are decreased. Device scaling leads to an elevation in current leakage as a result of unwanted Short Channel Impacts [7, 8].

These effects diminish the desired length of the channel of the device, hence decreasing its maximum operating voltages. Earlier articles have proposed many techniques to minimise power consumption in domino logical circuits [9, 10].

This work presents a ground-breaking domino approach for designing high-speed circuits using advanced submicron technology. The suggested approach delivers a decrease in power leakage and an enhancement in noise efficiency by running a circuit within the sub-threshold area. Section 2 of this research looks at the current variations of Domino logic in use. Section 3 provides a comprehensive analysis of the planned domino logic design, utilising the 45nm CMOS manufacturing node. Section 4 contrasts the proposed circuit with conventional domino designs. The article concludes in Section 5.

2. Literature Review

Domino logic has become the preferred option for creating fast and exceptionally effective microprocessors as a substitute for other dynamic logic structures. This is because it necessitates fewer components and has reduced power requirements, resulting in reduced dimensions and more energy efficiency. In contrast, dynamic CMOS logic that employs PMOS devices in its PUN is not as advantageous in terms of size and power effectiveness [11].

Furthermore, the presence of subthreshold current leakage, including gate current leakages, poses significant obstacles in designing various circuits using domino logic. The initial method used to construct a domino logic structure is illustrated in Figure 1 [12]. An important drawback of the FLDL technique involves the fact that during the assessment step when every input continues to continue at the lowest possible level, there will be a flow of current leakage throughout the PDN due to subthreshold and gate tunnel current.

The current leakage associated with the Footed Domino Logic (FDL) approach is minimized by including a footer transistor N1 within the evaluation system, as seen in Figure 2. An inherent limitation of the FDL approach is the introduction of a delay within the circuit's operation caused by the footer transistor, resulting in a decrease in the circuit's efficiency. The FDL's resilience diminishes when dealing with gates with significant fan-in [3].

In order to minimize the delay, the FDL circuitry demonstrated in Figure 3 incorporates the current mirroring transistors N2 and N3. In order to mitigate power leakage caused by the stacking operation, an additional transistor N1 is included in the fundamental FLDL circuit. The circuit shown in Figure 4 is referred to as High-Speed Clock Delay (HSCD) [6].

In order to minimize the current leakage of the assessment system, transistors named N2, N3, and P3 have been incorporated into the FDL circuitry to provide a direct current-biased voltage across the foot terminal N. Logic speed has become directly proportional to the dimensions of N1, N2, or assessment transistors.

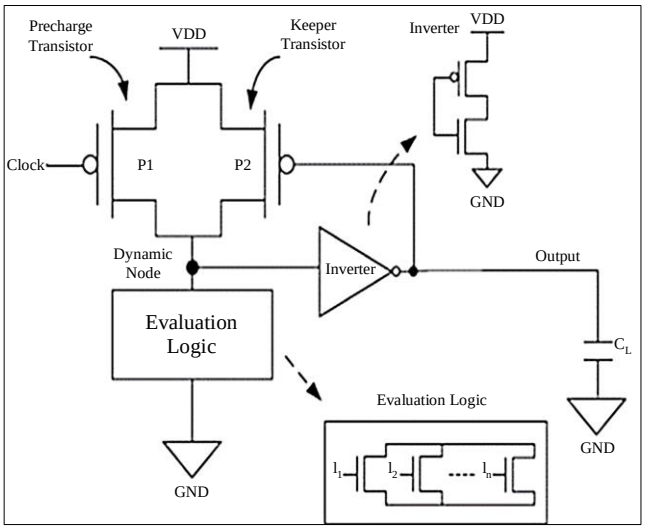

Fig. 1 Representation of FLDL

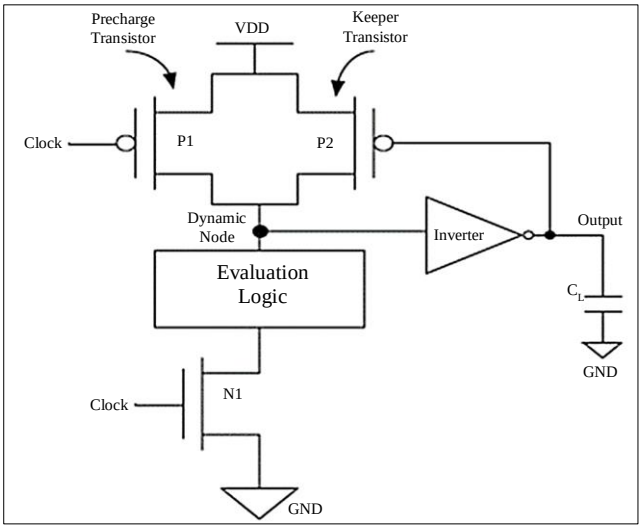

Fig. 2 Representation of FDL

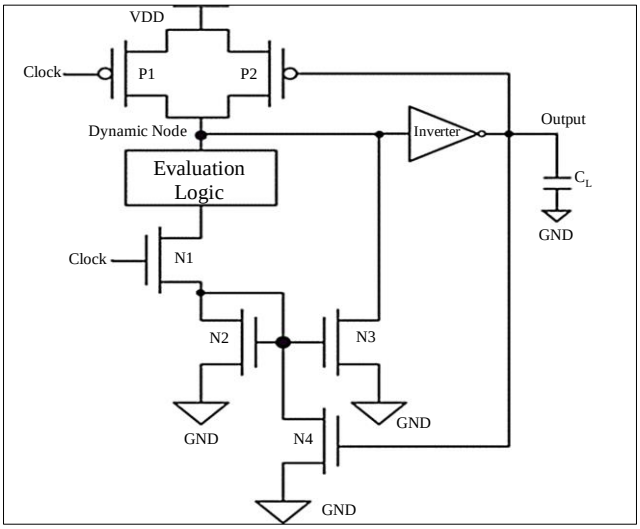

Fig. 3 Representation of CMFDL

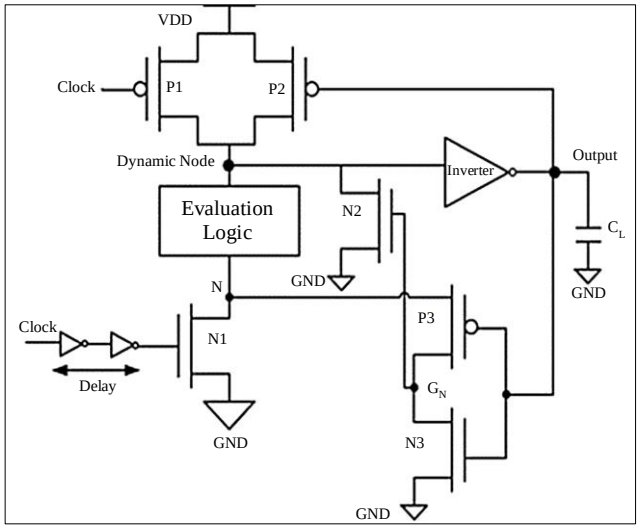

Fig. 4 Representation of HSCD

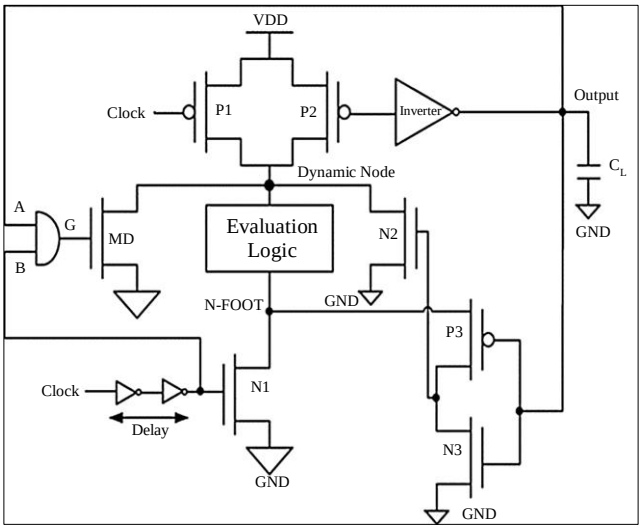

Fig. 5 Representation of M-HSCD

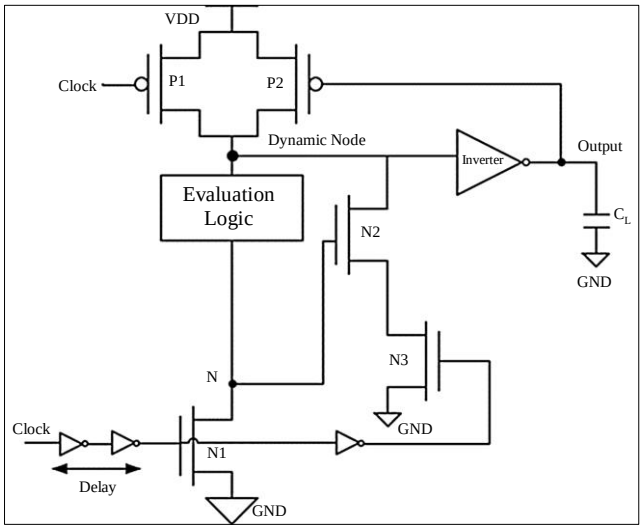

Fig. 6 Representation of CEDL

The HSCD technique integrates an AND gate known as G using a transistor made from NMOS in order to optimise the effectiveness of logic evaluation by improving its rate of operation. The circuit at issue is a modified version of the HSCD approach [6]. Thus, it is referred to as Modified HSCD (M-HSCD), as seen in Figure 5. The M-HSCD approach involves the discharge of a dynamic terminal whenever any of the inputs become significant throughout the evaluation phase. An important issue within the circuit involves the fact that during the pre-charge stage, the terminal of the gate of the N2 transistor falls into a high impedance condition, leading to extra power usage [9].

The circuit demonstrated in Figure 6 effectively addresses the issue of the floating gate when using the M-HSCD approach. The name used to describe this method is Conditional Evaluation Domino Logic (CEDL) [6]. In the fundamental footed domino logic, stacking transistors N2 and N3 are incorporated to ensure that the voltage level at foot terminal N remains stable, hence minimizing current leakage. Node N controls the operation of N2, whereas M3 is driven by clock pulses that are deliberately delayed.

Figure 7 illustrates a domino logic approach where the voltage on node N can be employed as feedback to discharge the dynamic node via transistors N2 and N3 [6]. In this context, transistor N2 functions to decrease the potential at junction Q towards VDD -Vth, resulting in an amplification of the current flowing via the keeper transistor. As a result, the circuit's durability increases, but its noise effectiveness decreases. In their research, Pooria Parvizi et al. [13] introduced a novel CMOS domino logic design that utilizes a memristor with GDI technology.

This high-speed, low-power full adder circuitry offers improved performance. A dynamic logic system has significance because it offers superior speed and uses fewer transistors as compared to a static CMOS-based logic circuit. The suggested approach exhibits peak power usage. Furthermore, the suggested approach demonstrates maximum latency. The suggested full adder has been modeled, and its power usage and efficiency are investigated utilizing HSPICE.

In their research, Gurjeet Kaur et al. [14] introduced architecture for broad fan-in highly efficient current comparative domino circuitry. The main objectives of the design were to minimize energy usage and delay within the 90nm and 45nm technological nodes. The schematic design and evaluation approach uses a 32-input width footless OR gate circuitry termed the Current Comparison Domino (CCD).

Singhal S et al. [15] introduced a domino logic called "Gated Clock and Revised Keeper (GCRK)" with a 16nm CMOS technological node. The recommended domino logic includes an improved keeper circuit designed to reduce power consumption within the circuit. The suggested concept

exhibits significant enhancements in PDP compared to the current approaches. The noise analysis, as well as Monte Carlo simulation results, demonstrates that the suggested design is impervious to noise and dependable in the face of various parametric fluctuations.

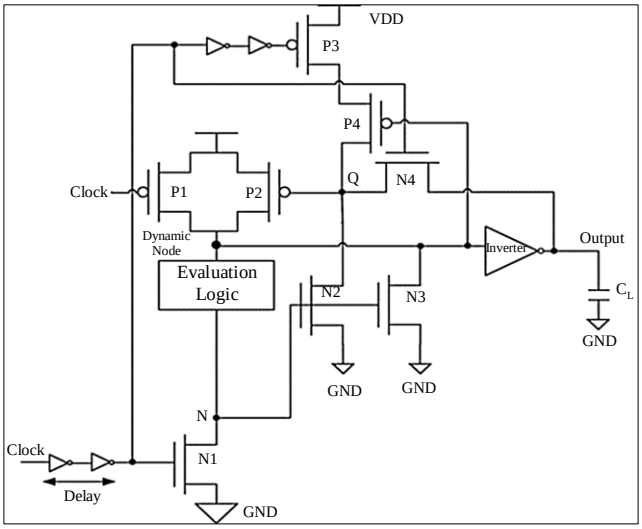

Fig. 7 Representation of CSK-DL

Vikash Vishwakarma et al. [16] suggested the use of dynamic buffering with a twist connection inverter (T-NOT) along with a sleep transistor to reduce energy usage and improve circuit performance. A twisted inverter has substituted the standard inverter within the current circuit. A weak keeper transistor has been employed to supply minimal Power at a dynamic terminal in order to minimize charge dissipation and enhance noise immunity.

In order to minimize the amount of Power lost due to leakage, a sleeping transistor has been incorporated into the dynamic node, thereby deactivating the extremely high threshold voltage transistor. The simulation was conducted using the Cadence Virtuoso simulation tool, using the 90nm technology with multiple voltage levels.

Garg S et al. [17] developed a new and innovative High Speed Stacked Transistor Logic (HSSTDL). The suggested and previously known circuits for domino OR gate designs have been simulated employing HSPICE 32 nm technology. The recommended circuit exhibits a reduced maximum power output in comparison to the existing conditionally stacked keeper domino logical circuitry. The recommended HSSTDL circuitry decreases the optimum delay when compared to the prevailing M-HSCD circuitry.

Komal et al. introduced a new method [18] that demonstrated the utilisation of AND and OR gates in domino logic. The circuits above operate inside the sub-threshold voltage region, resulting in a significant reduction in power usage. The circuits have been built utilizing the 180 nm CMOS design approach with the assistance of the LTspice tool.

3. Proposed High-Speed Sub-threshold Operated Domino Logic

The research analysis described in Section 2 explores different approaches to developing logic circuits using domino logic. The following section elaborates on a new approach to improve the basic idea of domino logic. Figure 8 illustrates the HSSODL technique.

Figure 8 illustrates a high-speed domino logic design, including an input portion and a result segment. The input part has been constructed up of pre-charge as well as keeper devices, while the assessment circuitry contains device PM3 including the footer circuit. The PM2 semiconductor device inversion circuits and NM3 devices make up the resultant unit.

The circuit functions in two distinct phases:

1. Pre-charge, and
2. Evaluate phases.

3.1. The Pre-Charge Phase of Operation

During the pre-charging period, the clock input keeps running at lower levels, causing the pre-charge device and PM2 to be activated. The pre-charged transistor PM0 has the responsibility for charging the dynamic node towards the voltage level of VDD. The node has a connection to the inverter, causing the resultant signal to be pulled downwards. Now, while the resultant signal is within the LOW state, MP1 (keeper) transitions into the ON position since PM2 had been within the ON position. The keeper prevents the connected node from getting released. Whenever the clock has reached a low condition, MN2 remains deactivated.

Changing the input within this mode of operation has no impact on the result. Throughout this stage of the process, the potential voltage at the drain terminal of NM2 is proportional to the voltage at the drain terminal of the keeper transistor, causing PM3 to switch off and prohibiting the drain terminal of the keeper transistor from discharging. The inclusion of PM3 efficiently increases the interference tolerance of the circuitry.

3.2. The Evaluation Phase of Operation

During this stage, the clock signal is adjusted to a high voltage level, which results in the activation of NM2. As a result, the source terminal of NM2 discharges by flowing via NM3. The voltage at the source terminal of NM2 decreases when the PM3 is turned up. The PM3 device activates the drain terminals of the connection of PM0 and PM1 (Dynamic Node), causing its output to switch to a HIGH state. The resultant signal has been subsequently connected to a feedback device PM4, which allows for the discharge of the outcome.

This is due to the fact that there is no discharge path that allows the PM3 to switch to active. However, when in the evaluation mode, when every input is set to LOW, the final result is identical to the clock signal. Whenever a HIGH feed has been detected during this period, the voltage level at the switching node will fall, causing the consequent signal produced to become ON.

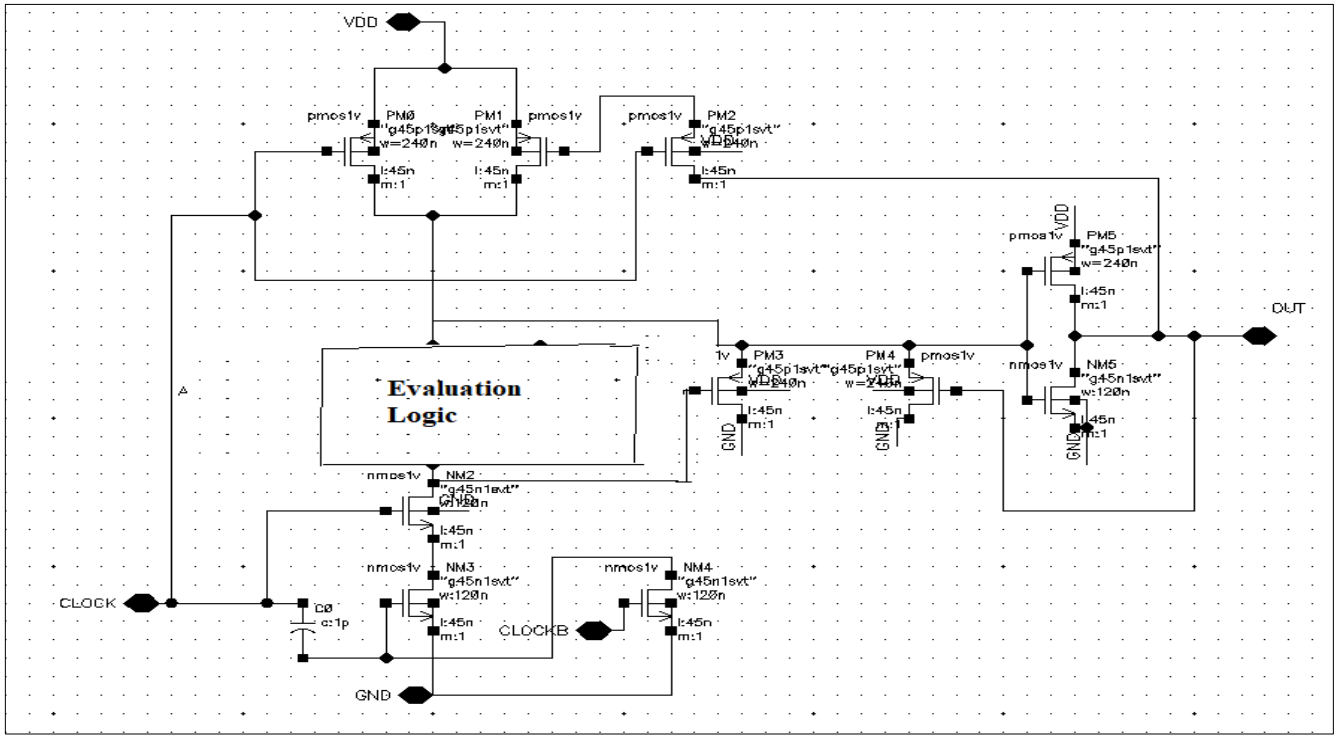

Fig. 8 Representation of proposed HSSODL

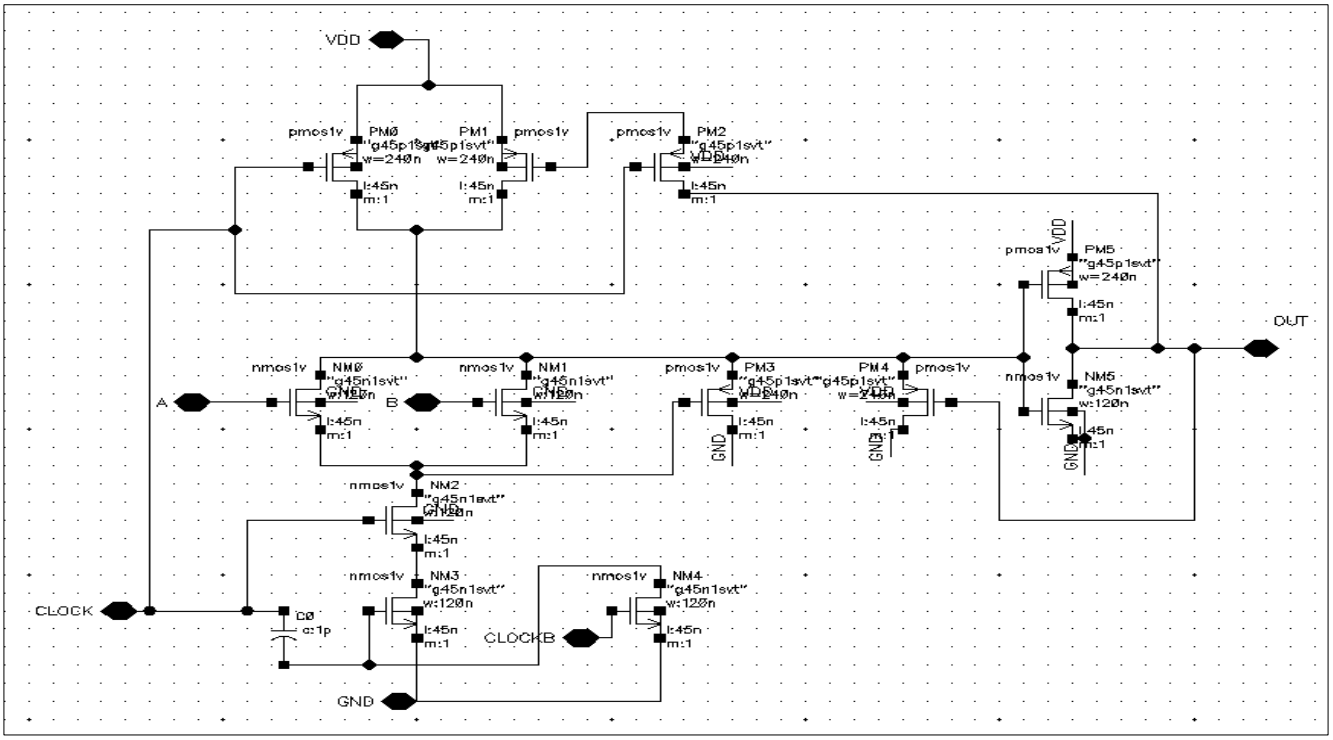

Fig. 9 Proposed HSSODL-based 2-input OR gate

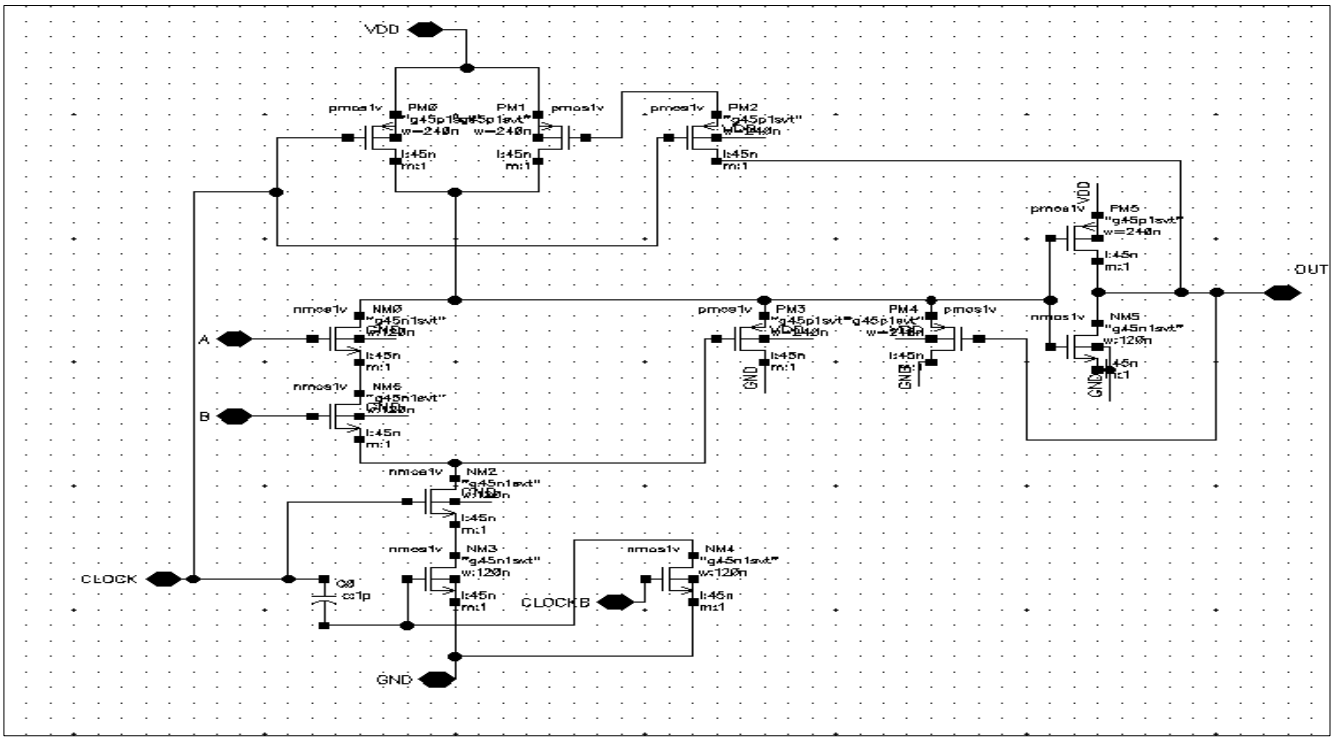

Fig. 10 Proposed HSSODL-based 2-input AND gate

An HSSODL-implemented two-input OR gate is illustrated in Figure 9. An OR gate has been employed to carry out a logical evaluation by connecting NM0 & NM1 devices in series. During the pre-charge stage, the circuit's operating voltage maintains at zero unless the CLOCK signal lowers to zero. The CLOCK signal has been appropriately modified to "1" throughout the active state. During idle operation, the clock signal remains at a low level, resulting in the activation of the pre-charge transistor PM0 and the transistor PM4. The pre-charged device provides a mechanism for elevating the voltage threshold of the dynamical node to match that of VDD.

The node has been coupled to the inverter, causing the resultant signal to be pulled downward. The dynamic node would discharge throughout the evaluation procedure in the event that one or more of its input signals attain high levels. Following the discharge of the dynamic node, the presence of an inverter inevitably results in a delay prior to an increase in the circuit's output.

An HSSODL-implemented two-input AND gate is illustrated in Figure 10. To carry out logical evaluation, an OR gate connects NM0 & NM6 devices in series. During the pre-charge stage, the circuit's operating voltage maintains at zero until the CLOCK pulse lowers to zero. The CLOCK signal has been appropriately modified to "1" throughout the active state.

During idle operation, the clock signal remains at a low level, resulting in the activation of the pre-charge transistor PM0 and the transistor PM4. The pre-charged device provides a mechanism for elevating the voltage threshold of the dynamical node to match that of VDD. The node has been coupled to the inverter, causing the resultant signal to be pulled downward. After the dynamic node discharges, there is an unavoidable delay induced by the presence of an inverter before the output of the circuit turns higher.

4. Results and Discussion

The proposed investigation utilizes both current and novel approaches using CMOS semiconductor technology. Subsequently, the Cadence virtuoso 45 nm technological node is used for simulating each of these designs and providing a comparison of the findings. In order to reduce the latency of the circuitry under consideration, the breadth of the PMOS transistor employed has been expanded to a total of four times the minimum channel length (Lmin), in contrast to prior iterations that utilized a width of two times Lmin.

The channel length, denoted as Lmin within this specific instance, is set to 45 nanometers. The physical parameters of the parallel-coupled NMOS device in the testing circuitry have been regarded as adjusted to increase the minimum channel length (Lmin) by a factor of two. The width proportion (Wp/Wn) of PMOS and NMOS devices had been set at 2. Various methodologies have been employed to evaluate the durability and resistance to interference of domino logical circuits. Figure 11 unambiguously illustrates that any time the CLOCK signaling is set to a logically lower voltage, the resultant value remains in a logically negative state.

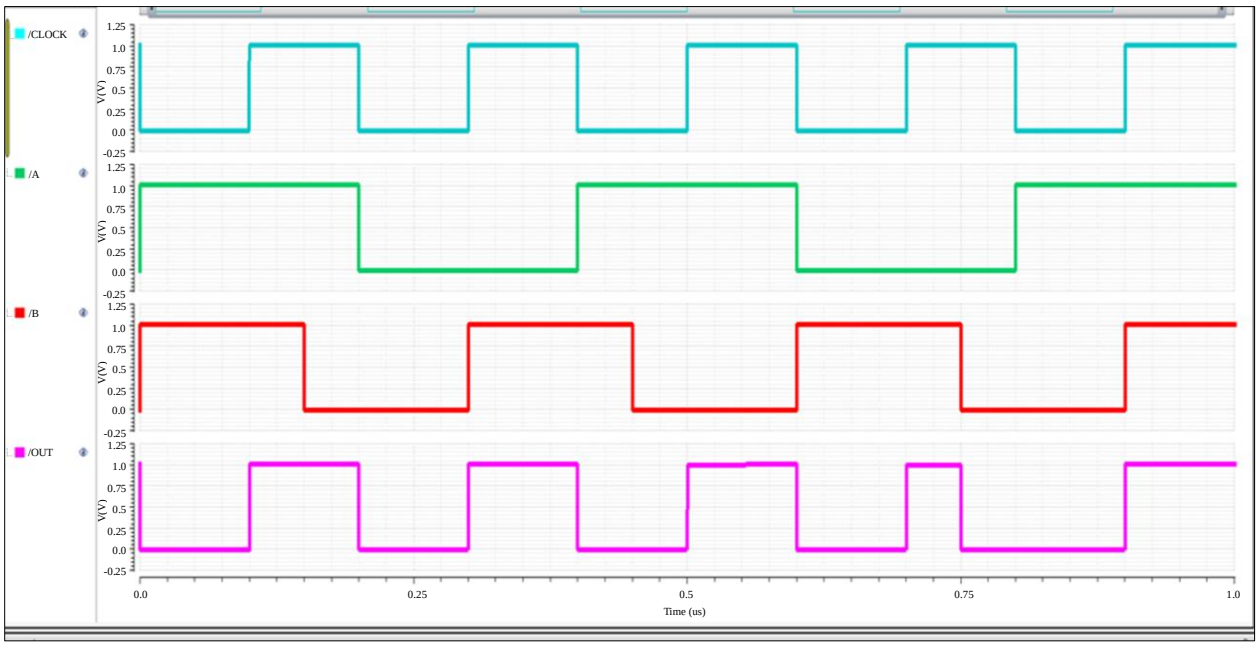

Fig. 11 Transient analysis of suggested HSSODL-dependent OR gate featuring 2-inputs

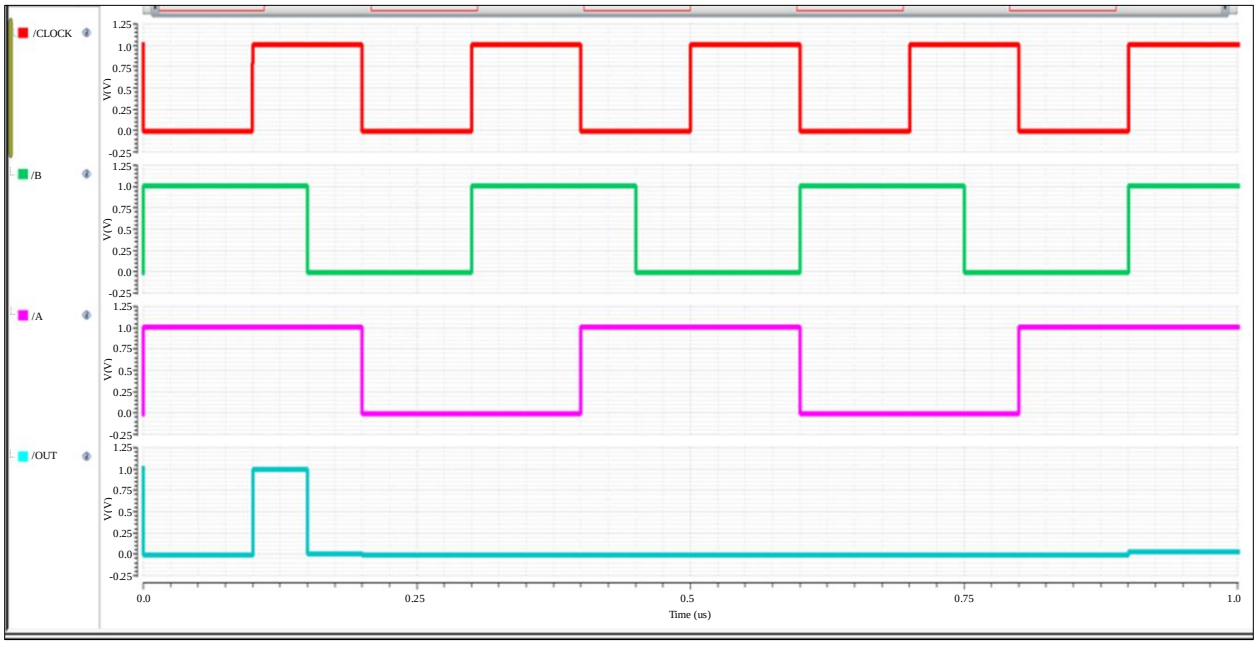

Fig. 12 Transient simulation waveform of proposed HSSODL-based 2-input AND gate

Whenever the CLOCK pulse has been configured to a higher logic level, the output will also be changed to a higher logic level. However, if either of the inputs has been configured for a high logic level, the output will continue to operate at a low logic level. Figure 12 demonstrates that whenever the CLOCK pulse has been configured to a low logic level, the resulting signal continues at a low logic level. While the CLOCK input is set to a higher logic threshold, the resultant value becomes high merely because both inputs have been likewise high. Otherwise, the results will stay minimal.

Table 1 demonstrates the average power usage, and delay, along with PDP results for the various domino logic approaches employed within a 16-bit logic OR gate. The suggested solution outperforms all other domino logic systems with regard to power efficiency, delay suppression, and higher Power-Delay Product (PDP) value, grater Energy-Delay Product (EDP). The logic OR gate with sixteen inputs functions as a validation circuit. As denoted by VDD, the supply voltage has been adjusted to 1 volt. The proposed approach entails the clustering of transistors in order to

mitigate noise and minimize power leakage simultaneously. The objective of the proposed method is to eradicate conflict both within the guardian and the evaluation network, leading to reduced energy consumption and latency.

Table 1 clearly demonstrates that the suggested domino logic approach exhibits a minimum improvement of 35% with respect to latency. The suggested domino logic approach uses a little higher amount of power compared to the domino logic method provided in reference [20]. Nevertheless, the combined PDP and EDP are lower in comparison to the current domino logic methods. The purpose of the current investigation is to decrease power utilization through minimizing the device's dimensions and lowering the supply values. Device scalability leads to an expansion of current leakage due to unwanted Short Channel Impacts. A shorter channel results in a reduction in the entire channel length that eventually gives rise to a fall in the optimum voltage required for the operation of the circuitry.

Table 1. Evaluation of current domino logic configurations in relation to the recommended domino technique

Domino Approach	Power Usage (uW)	Delay (pS)	PDP $X10^{-15}$ WS	EDP x 10^{-21} WS
CMFD [19]	1.19	91.8	109.28	10.03
CEDL [20]	0.939	69.9	65.79	4.60
HSCD[20]	1.238	49.04	60.81	2.99
CSK-DL[20]	1.8	57.3	104.84	6.005
GPKD[21]	1.009	48.3	48.80	2.36
FDSTDL[21]	0.9	45.21	40.24	1.82
LLCKDL [22]	0.121	40.12	4.85	0.19
Proposed	0.129	29.61	3.82	0.113

Consequently, the ongoing increase in circuit leakage will persist. The UNG could have been attributed to the conduct of a noise study. The acronym "UNG" denotes the extent of DC distortions at the source nodes, resulting in a corresponding amount of distortions at the subsequent nodes [14]. In order to determine the UNG, a fraction of the voltage supplied may be used as a momentary burst of energy that is sent to the input connections of the assessment circuitry. Figure 13 depicts an analysis of the UNG, which consists of several conventional domino logical circuits and a novel domino logic approach. An enhanced UNG result indicates a robust capacity to endure and resist noise. A changing amplitude noise pulse with an unchanged width has been used as an input signal for calculating UNG. The findings indicate that the proposed method displays greater noise resistance compared to the previously employed domino approaches.

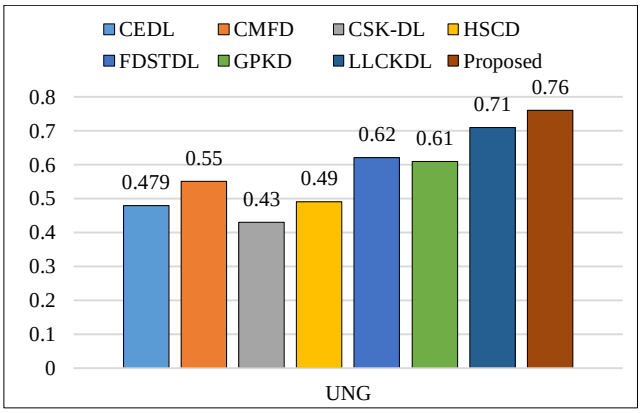

Fig. 13 Performance evaluation of recommended domino logic circuit in terms of UNG

The circuit's effectiveness was evaluated under various scenarios employing a Monte Carlo calculation. Throughout the circuit modeling, the values of oxide thickness, mobility, minimum voltage, and transistor size have changed without any specific reason or pattern. A selected variation achieved the generated random results for the variables. Table 2 shows the estimated standard error and mean-variance of power use and delay across one hundred Monte Carlo trials. The recommended circuit has a lesser variation and standard deviation. As a consequence, the proposed circuit is reliable and resilient.

Table 2. Investigation of the suggested domino logic circuit employing Monte Carlo computation

Parameter	Average Power (µW)	Delay (ps)
Mean value (µ)	3.957	33.49
Standard Deviation (σ) Value	0.205	0.73
Variability (σ/µ) Value	0.051	0.021

5. Conclusion

This investigation presents a new domino logic architecture with the sub-threshold voltage implementation of domino logic. The computational simulation involving a 16-bit OR gate has been done using both aspects of the recommended structure and widely used methods, including domino logic. The proposed system demonstrates substantial improvements in power performance, latency, EDP, and PDP as compared to conventional domino logic methods. The circuit remains steady and immune to perturbation. As a consequence, the recommended design is suitable for use in scenarios which require low power consumption while retaining high efficiency. The modelling findings reveal that the planned domino's power use has become more efficient. Future studies might concentrate on developing on-chip training circuitry while employing low-power design techniques to minimise energy usage.

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