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Original Article

Performance Evaluation of Ultra-Low Power ADCs in Energy Harvesting Systems

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Abstract *- Quality healthcare has become more relevant than ever before in the history of humanity. There is an ardent need to develop affordable remedies in the healthcare sector. The contemporary market landscape insists that all upcoming designs are low power and portative. This necessity peaked during the COVID-19 pandemic. In any biological data acquisition/monitoring system, the signals are continuous. These analog signals are usually amplified, filtered and converted into digital codes for ease of further processing. Thus making an Analog to Digital Converter (ADC) an integral part of every bio-medical data acquisition system. Successive Approximation Register (SAR) ADCs have many potential biomedical applications due to their ability to accurately convert analog signals into digital form. SAR ADCs used in biomedical applications include Electroencephalography (EEG), Electromyography (EMG), Electrocardiography (ECG), Blood glucose monitoring, and Magnetic Resonance Imaging (MRI). These versatile ADCs are essential components in advancing healthcare technology facilitating accurate diagnosis and treatment. The proposed ADC consumes low power and, hence, is suitable for mobile healthcare devices.*

Keywords *- Analog to Digital Converter, Electrocardiography, Digital to Analog Converter, Sample and hold, Logarithmic search, Bandwidth of operation.*

1. Introduction

The rapid advancement of biomedical engineering has significantly transformed the landscape of modern healthcare. Innovations in this field have enabled the development of sophisticated devices capable of real-time monitoring, diagnosis, and treatment, thereby enhancing the quality of patient care. At the heart of these advancements lies the ADC, a critical component that converts continuous analog signals, such as those produced by the human body, into digital form for processing and analysis. The design of a low-power ADC for biomedical applications is a crucial challenge due to the inherent constraints and demands of such applications, including the need for high accuracy, low noise, and minimal power consumption.

Biomedical signals such as ECG, EEG and EMG are essential for diagnosing and monitoring various health conditions. These signals typically possess low frequencies and small amplitudes, requiring ADCs with high resolution and excellent noise performance to accurately capture the subtle variations inherent in biological signals [1]. For instance, an ECG signal that measures the electrical activity of the heart typically ranges from 0.05 to 100 Hz with amplitudes in the millivolt range. Accurate digitization of these signals is vital for reliable analysis and interpretation, making the performance of the ADC a critical factor in the overall effectiveness of biomedical devices. Power consumption is a paramount concern in the design of ADCs for biomedical applications, particularly for wearable and implantable devices. These devices often rely on limited power sources, such as small batteries or energy harvesting systems, necessitating the development of ADCs that consume minimal power while maintaining high performance [2].

Low power consumption extends the operational life of these devices, reducing the frequency of battery replacements or recharges, which is especially critical for implantable devices where surgical procedures are required for battery replacement. Moreover, minimizing power consumption helps in reducing the heat generated by the device, enhancing patient comfort and safety. The design of a low-power ADC for biomedical signal processing involves a delicate balance between several factors: resolution, sampling rate, noise performance, and power efficiency. Different ADC architectures offer various trade-offs in these aspects, and the choice of architecture depends on the specific requirements of

the application [3]. For instance, Sigma-Delta (Σ-Δ) ADCs are known for their high resolution and excellent noise performance, making them suitable for low-frequency biomedical signals. However, they typically consume more power compared to other architectures. On the SAR ADCs offer a good balance between power consumption and resolution, making them a popular choice for many biomedical applications [4]. Several strategies can be employed to achieve low power consumption in ADC design. These include optimizing the analog front-end, reducing the supply voltage, utilizing low-power circuit techniques, and incorporating power management features. Advanced fabrication technologies, such as Complementary Metal-Oxide-Semiconductor (CMOS) processes, also play a crucial role in enabling the development of low-power ADCs [5].

Furthermore, digital calibration techniques can be used to correct for errors and improve the accuracy of the ADC without significantly increasing power consumption. This article explores the fundamental principles and design considerations for creating low-power ADCs tailored for biomedical signal digitization. It examines various ADC architectures, highlighting their advantages and limitations in the context of biomedical applications [6].

The discussion extends to innovative design strategies and optimization methods that can be employed to reduce power consumption while maintaining the necessary accuracy and reliability of signal conversion. By addressing these design challenges, the development of efficient low-power ADCs can significantly enhance the functionality and sustainability of modern biomedical devices, ultimately contributing to better patient care and improved health outcomes. The quest for low-power ADCs in biomedical applications is driven by the need to create compact, efficient, and reliable devices capable of accurate real-time monitoring and diagnosis [7].

The design of such ADCs requires a comprehensive understanding of the trade-offs involved in different architectures, as well as the implementation of advanced techniques to optimize power consumption. As technology continues to evolve, the development of next-generation low-power ADCs will play a pivotal role in advancing biomedical engineering and improving healthcare delivery [8].

Table 1. Biomedical signals

Signal	Location	Amplitude in Volts	Bandwidth in Hz
EMG	Muscle	1-10m	1-3k
ECG	Heart	0.1-1m	0.05-100
EEG	Brain	10-100u	0.5-100
EOG	Retina	15-200u	38

2. Literature Review

The design of low-power ADCs for biomedical applications has been a significant area of research, driven by the increasing demand for portable and implantable medical devices. This literature review explores the advancements, methodologies, and challenges in the design and implementation of low-power ADCs, focusing on various architectures, power optimization techniques, and their application in biomedical signal processing [9].

2.1. ADC Architectures

1. SAR ADCs are widely used in biomedical applications due to their balance between resolution, speed, and power consumption. Recent research has focused on enhancing the energy efficiency of SAR ADCs. For instance, Sanyal and Sun (2013) proposed an energy-efficient SAR ADC that employs a variable resolution technique to adapt power consumption based on the signal's amplitude.
2. Sigma-Delta (Σ-Δ) ADCs Sigma-Delta ADCs are known for their high resolution and excellent noise performance, making them ideal for low-frequency biomedical signals. A study by Park and Temes (2007) demonstrated a low-power, high-resolution Σ-Δ ADC for ECG signal acquisition. They used a multi-bit quantizer and dynamic element matching to enhance performance while reducing power consumption.
3. Pipeline ADCs Pipeline ADCs offer high speed and resolution but traditionally consume more power. Recent innovations have aimed at reducing power usage while maintaining performance. For example, Chen et al. (2012) introduced a power-efficient pipeline ADC using a novel calibration technique to minimize power consumption without sacrificing accuracy.
4. Flash ADCs Flash ADCs provide high-speed conversion but are typically power-hungry. However, applications requiring rapid signal acquisition, such as neural recording, can be optimized for low power. Murmann et al. (2008) explored a low-power flash ADC design using a reduced comparator array to decrease power usage.

2.2. Power Optimization Techniques

1. Sub-threshold Operation Operating ADCs in the sub-threshold region can significantly reduce power consumption. Mandal and Visvanathan (2006) investigated the use of sub-threshold operation in SAR ADCs, achieving substantial power savings at the cost of reduced speed, suitable for low-frequency biomedical signals [10].
2. Clock Gating and Dynamic Voltage Scaling Clock gating and dynamic voltage scaling are effective techniques for reducing dynamic power consumption. Bai and Shi (2011) demonstrated these techniques in the context of a Σ-Δ ADC, achieving significant power reductions by dynamically adjusting the clock and voltage based on the workload [11].

3. Capacitive DAC Optimization the Digital-to-Analog Converter (DAC) is a critical component in SAR ADCs, and optimizing its design can lead to lower power consumption. Liu et al. (2010) proposed a capacitive DAC optimization technique that reduces switching energy, thereby decreasing the overall power consumption of the ADC [12].
4. Analog Front-End (AFE) Design Optimizing the analog front-end can also contribute to lower power consumption. Xu et al. (2015) designed a low-power AFE for ECG signal acquisition, incorporating a Low-Noise Amplifier (LNA) and a low-power ADC, achieving high fidelity with minimal power usage.

2.3. Biomedical Applications

1. Electrocardiogram (ECG) Monitoring Low-power ADCs are crucial for continuous ECG monitoring. Chi and Cauwenberghs (2010) developed a low-power ECG acquisition system utilizing a Σ-Δ ADC with a power-efficient filter to ensure accurate and reliable signal acquisition.
2. Electroencephalogram recording is essential for EEG recording, where signals are weak and susceptible to noise, and high-resolution and low-power ADCs are essential. Chae et al. (2009) presented a 128-channel low-power EEG acquisition system employing SAR ADCs, demonstrating significant power savings while maintaining signal integrity [13].
3. Implantable Devices Implantable medical devices require ultra-low-power ADCs due to their reliance on limited power sources. Harrison (2008) reviewed various techniques for designing low-power ADCs for implantable applications, emphasizing the importance of minimizing power to extend device longevity.

2.4. Challenges

Despite significant advancements, challenges remain in the design of low-power ADCs for biomedical applications. One major challenge is achieving the desired trade-off between power consumption, resolution, and speed. Additionally, ensuring the ADC's robustness against process, voltage, and temperature variations is crucial for reliable operation in diverse biomedical environments [14].

Future research is likely to focus on the integration of ADCs with other low-power components in system-on-chip (SoC) designs, further miniaturizing biomedical devices while enhancing their functionality. Advanced fabrication technologies, such as Fin-FET and nanotechnology, may also offer new avenues for reducing power consumption and improving performance [15].

3. Different Methods of Low Power designs

As it is necessary to choose the design in accordance with the constraints of the project at hand. Several low power options have been developed. The Sample and hold circuit, D flip flop [16]. The basic building blocks of register, DAC, and comparator are crucial blocks of the SAR ADC that contribute to total power consumption. The sections that follow analyze these crucial blocks.

3.1. Sample and Hold

Sample and hold are an un-expandable sub-block in every Analog to Digital converter. Based on the requirements, the desired sample and hold circuit are chosen. The simplest sample and hold circuit can be realized using a CMOS switch. It consists of a single transistor and a holding capacitor. This circuit tracks the input signal when the transistor is ON and holds that value when the transistor is OFF. However, in all practical applications, the signal integrity is compromised due to limitations like Channel Charge injection and Clock feed through [17].

Channel Charge injection - This occurs when the transistor is OFF. Due to the difference in the charge densities across the channel and output capacitor, the charge is redistributed. This redistribution causes variations from the desired value.

Clock Feedthrough - This occurs due to the inverse relation between the impedance of the capacitor and the hold sub-block; the gate oxide acts as the capacitor while the sampling clock is analogous to the applied signal. Therefore, for higher sampling frequency, the sampled output is corrupted with clock transitions [1].

To address these limitations while keeping the energy requirements to a minimum, we choose a passive free op-amp sample and hold the circuit with and without bootstrapping. In non-bootstrapping, replacing a single transistor with a transmission gate reduces the charge injection. However, transmission gates use inverting clocks, which is not a wise design choice when the objective is to stretch out battery longevity [18].

In Bootstrapping, we have implemented two techniques. The boosted drive and the bootstrapped. The below table summarises the concept illustrated above. When the constraints of silicon die area and wider operating bandwidth are influencing factors, the boosted driver is a suitable architecture. Figure 1. Shows the boosted driver of the Sample and Hold.

Table 2. Power analysis of sample and hold circuit

Architecture	Transistor	Power Consumed
Bootstrapped	14	6.27uW
Boosted Driver	8	2.26uW
Transmission gate	2	42.25nW

3.2. D Flip Flop

The D-Flip flop is a commonly used sub-block in register design. The conventional Master and Slave D flip flops have eight NAND gates and a NOT gate. If this functionality is achieved through traditional complementary-ratioed logic, it claims the area equivalent of thirty-four MOSFETs. [22] As the number of active transistors (turned on) increases, their energy efficiency decreases. Hence, the first logical way forward is to reduce the number of active transistors at every instant. Below are the results of such attempts.

The circuit in Figure 2 consists of two cross-connected inverters coupled with a slightly modified CMOS inverter-like arrangement. This configuration behaves as a Master-Slave D- Flip flop [19].

Table 3. Power analysis of D flip flop

Architecture	Transistor	Power Consumed
Bootstrapped	14	6.27uW
Boosted Driver	8	2.26uW
Transmission gate	2	42.25nW

3.3. Digital to Analog Converter

The principal algorithm that the SAR DAC employee uses is binary search. The accuracy of the digital counterpart of the input signal is improved with every iterative cycle. During each of these iterations, the sampled value is compared with an adaptive reference value. In order to generate a reference signal corresponding to the previous digital output, a digital-to-analog converter must be used for feedback. DAC, being one of the complex sub modules, demands ingenuity. There are many off-the-shelf DAC designs like R2R, charge scaling, current steering, and pipeline architectures. In practice, the design of the current steering DAC is increasingly complex. It is a Herculean task to achieve perfect mirroring, making designs like R2R and charge scaling the only viable choices [20].

The ease of implementing a capacitor outweighs that of implementing resistors. In the literature, one may also come across diode-based DACs. However, due to the inherent non-linear characteristics of diodes, the impact of noise becomes dominant [21]. Due to the above stated observations, charge scaling DAC is an attractive solution, although the area consumption approximately doubles for every one-bit increase in resolution. Figure 3. Shows the Charge scaling DAC

Table 4. Power analysis of DAC

Architecture	Power Consumed
Charge scaling DAC	45.14uW
R2R DAC	98.8u W

3.4. Comparator

The most energy-efficient way of realizing voltage comparison is through a dynamic comparator. The operation of the dynamic comparator comprises Input Comparison. The dynamic comparator receives two input voltages: the analog input voltage (VIN) to be digitized and a reference voltage (VREF) that represents a specific threshold value. The comparator's objective is to determine whether VIN is greater than or less than VREF.

Pre-charging: Before the comparison, the dynamic comparator goes through a pre-charging phase. During this phase, the internal nodes of the comparator are charged to appropriate voltage levels [23]. This ensures that the comparator operates within a known and valid voltage range.

Comparison Phase: Once the pre-charging is complete, the comparison phase begins. The inputs of the comparator are fed with the input voltage VIN and the reference voltage VREF. If VIN is greater than VREF, the dynamic comparator generates a logic high output, indicating that the Most Significant Bit (MSB) of the digital output should be set to 1. If the magnitude of the difference between Vref and VIN is non-positive, the output is pulled down to logic low. The dynamic comparator generates a logic low output, indicating that the MSB of the digital output should be set to 0. Decision Process: Based on the output of the dynamic comparator, the SAR ADC's control logic determines the subsequent bit values of the digital output [24].

This decision process involves a binary search algorithm, where the control logic successively approximates the digital value by comparing the remaining bits with different reference voltages. Iteration: The SAR ADC iterates through the comparison process for each bit, starting from the MSB and proceeding to the Least Significant Bit (LSB). For each bit, the dynamic comparator compares the analog input voltage with the appropriate reference voltage, providing the necessary information for the control logic to determine the corresponding bit value [25].

The dynamic comparator's nominal power consumption and fast operation make it an appealing choice for SAR ADCs, where high-speed, moderate-resolution conversions are required. Figure 4 shows the dynamic comparator, and Figure 5 presents the graphic abstract of the design.

Table 5. Power analysis of comparator

Architecture	Transistor	Power Consumed
Differential with buffer	13	63uW
Differential with CS amplifier	10	52.4uW
Dynamic Comparator	9	25.44uW

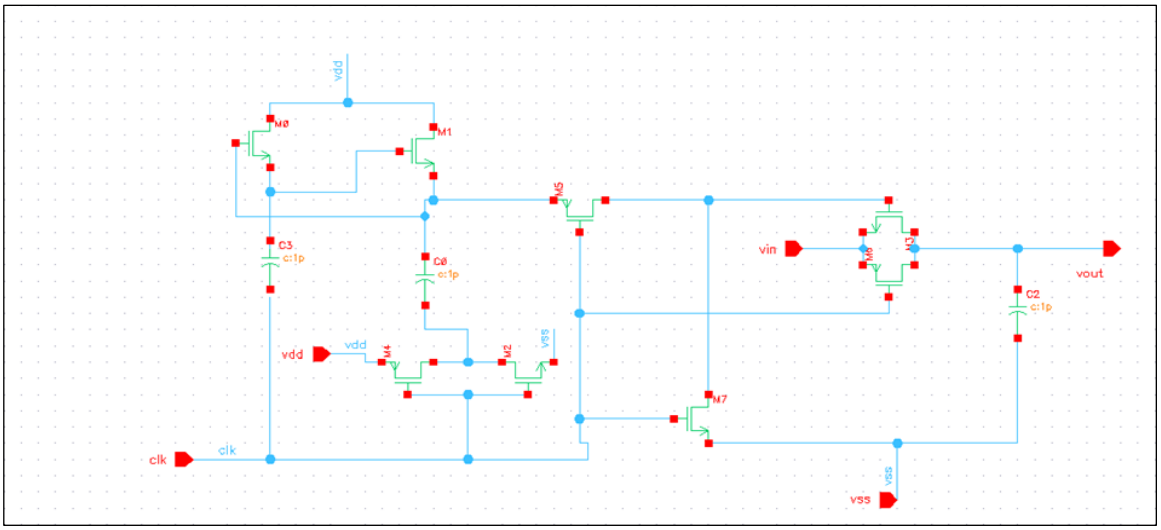

Fig. 1 Boosted driver sample and hold

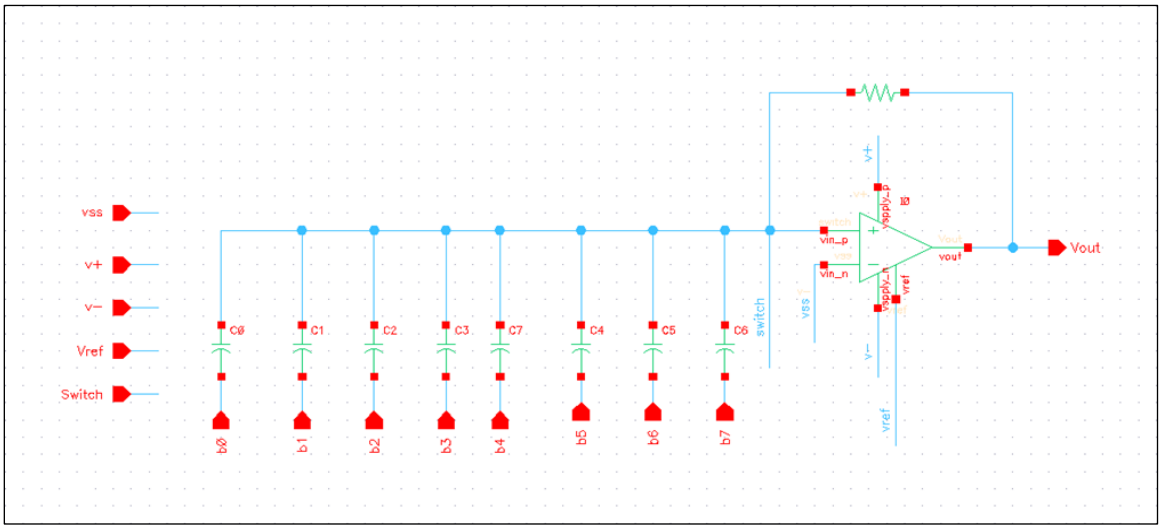

Fig. 2 Master slave D flip

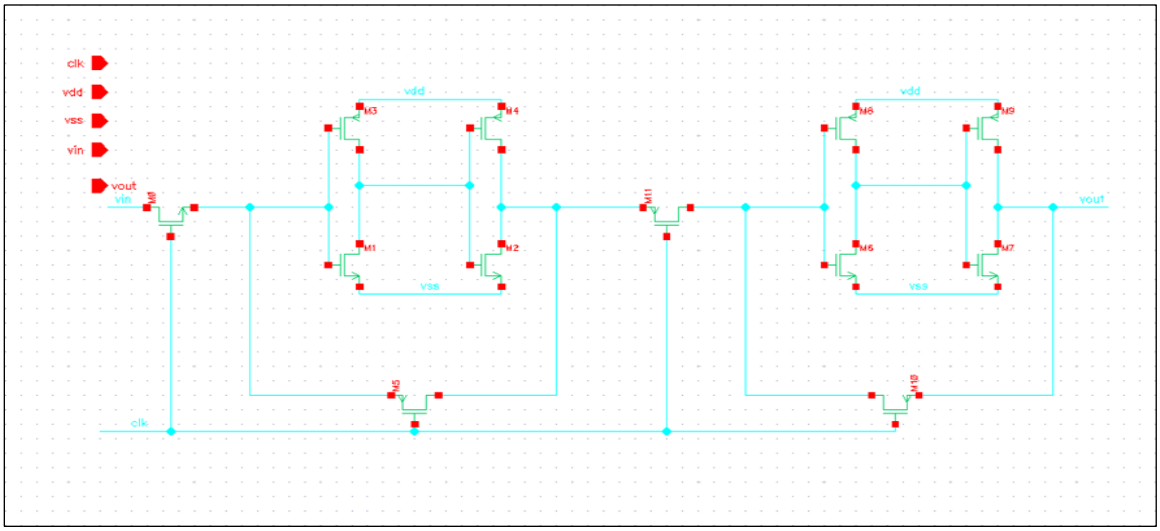

Fig. 3 Charge scaling DAC

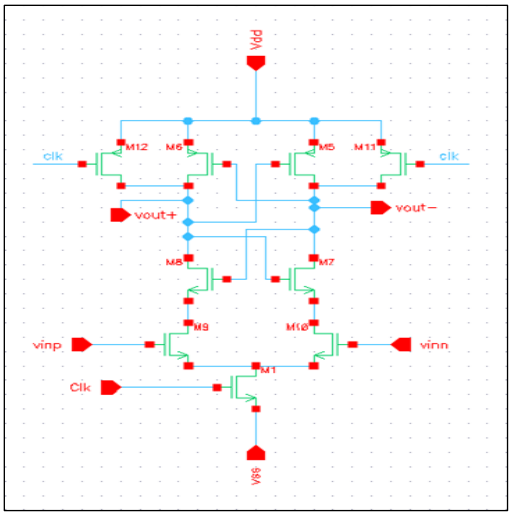

Fig. 4 Dynamic comparator

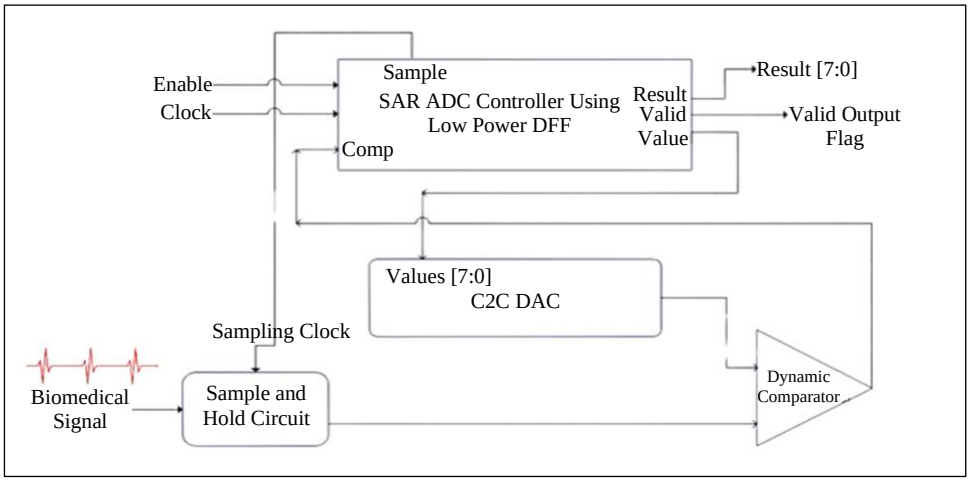

Fig. 5 Graphical abstract of the design presented

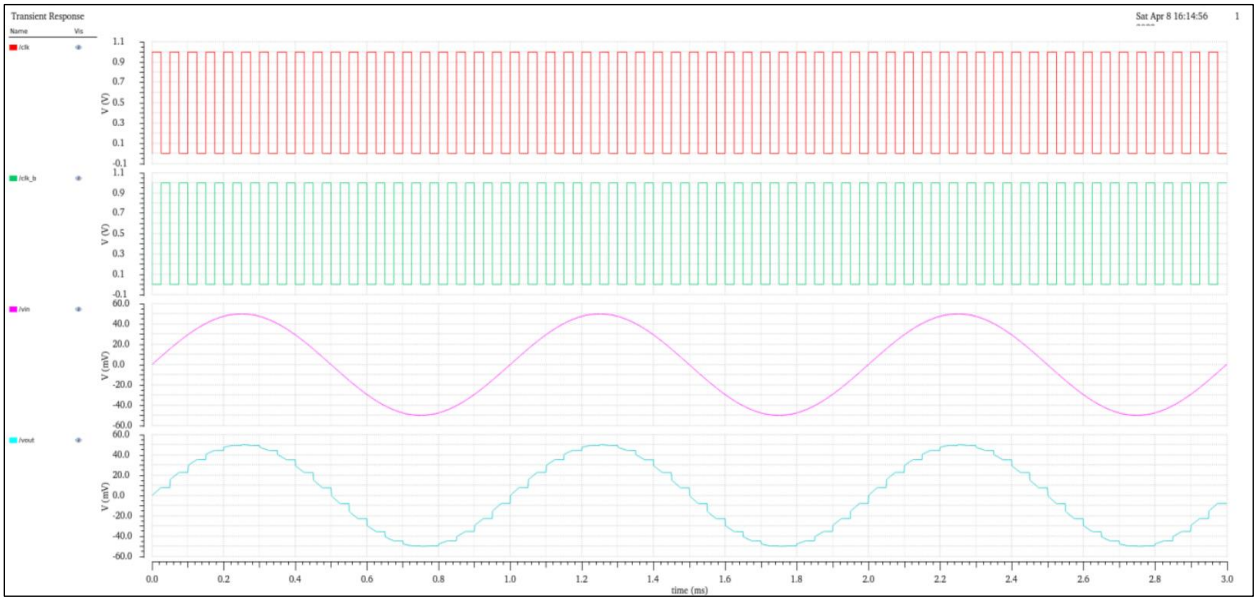

Fig. 6 Simulation result of sample and hold circuit

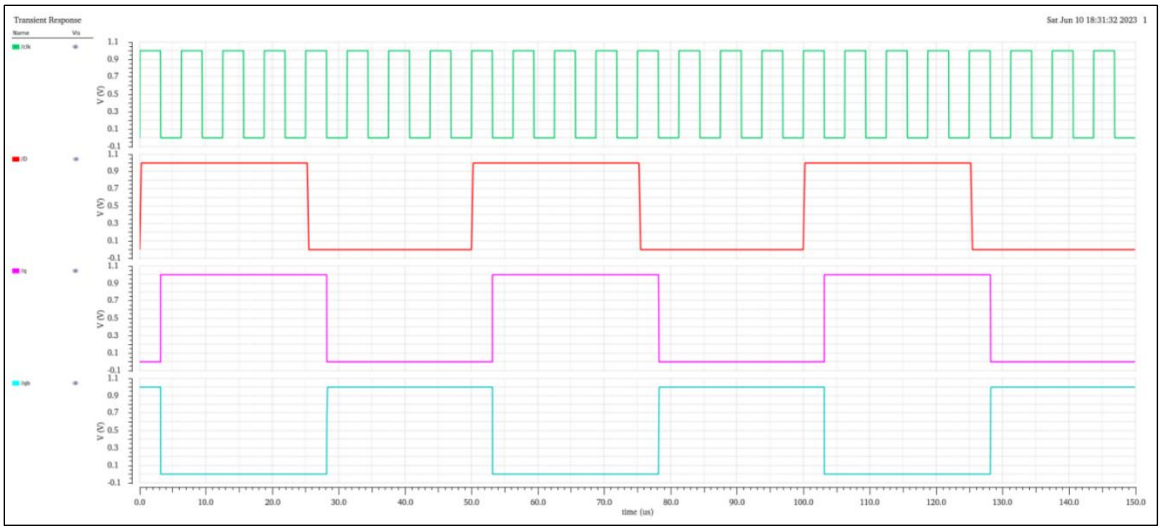

Fig. 7 Simulation result of D flip flop

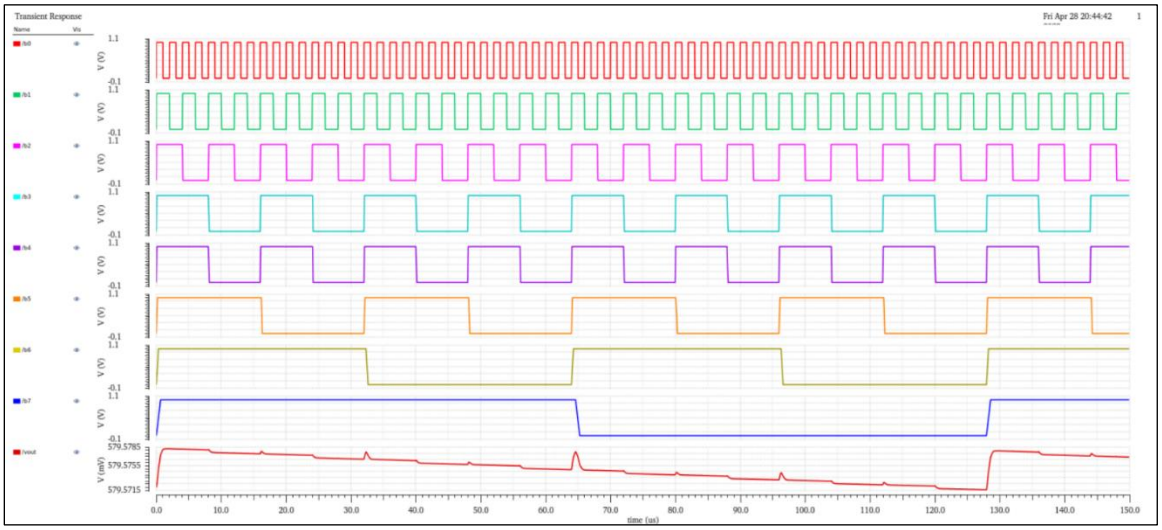

Fig. 8 Simulation result of digital to analog converter

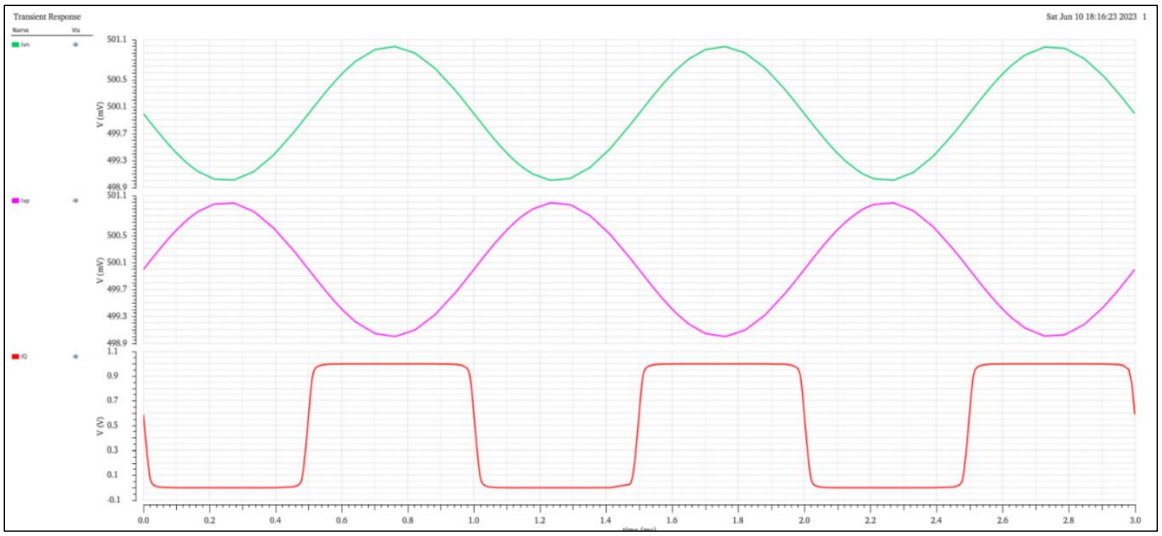

Fig. 9 Simulation result of comparator

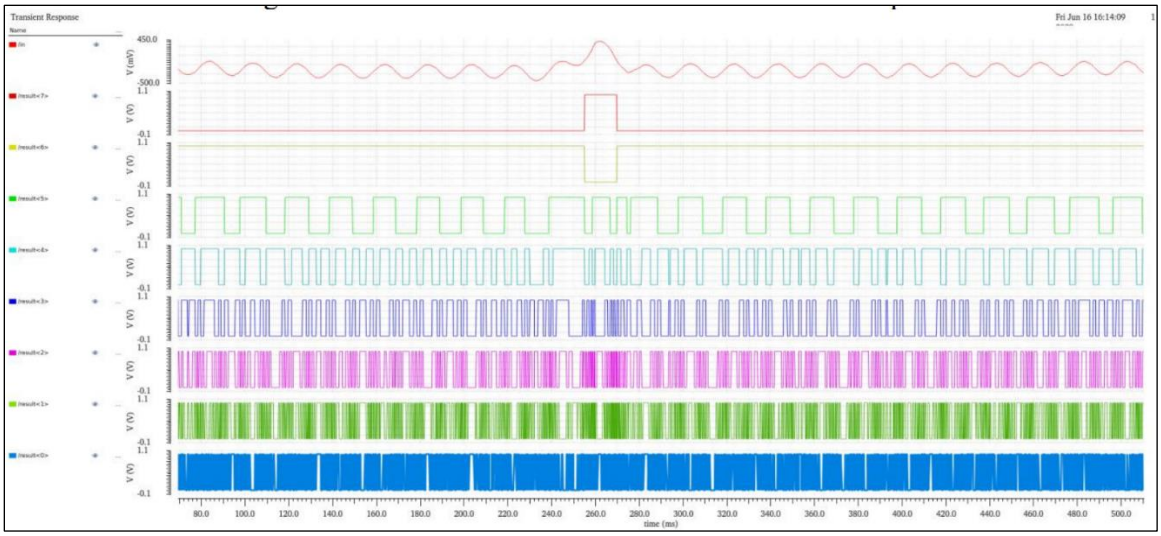

Fig. 10 Simulation result of SAR ADC

4. Simulation Results

In this article, a thorough examination and simulation of the critical components of a SAR-ADC and the components analysed include the Sample and Hold circuit shown in Figure 6, D Flip-Flop shown in Figure 7, the Digital to Analog Converter in Figure 8, and Comparator simulation results in Figure 9. The simulations showcase the sample and hold circuit's ability to accurately sample and hold the input signal, the D Flip-Flop's reliability in storing digital data, the DAC's precision in converting digital output back to analog, and the Comparator's speed and accuracy in signal comparison. Integrating these components, the SAR ADC simulation demonstrates efficient and precise analog-to-digital conversion, validating the design's overall performance and suitability for applications requiring high-resolution and accurate conversions.

5. Conclusion

In conclusion, we can say that the SAR ADCs are suitable for medical applications for the following reasons. It consumes low power, making it suitable for mobile devices and invasive implants. Although the operating frequency is low, it is sufficient as most biomedical signals do not have useful information at high frequencies. Since we are dealing with life-critical signals, certain measures must be employed to combat the effect of noise. The harmful effects of noise can be managed by the efficient design of pre-amplifiers, which can later be integrated easily with SAR ADC. In summary, the objective of the project is very relevant to the needs of society, and the results obtained are promising. Optimizing the design for a particular application by exploiting the advances in process technology. The social and market value of the project may also be enhanced by increasing resolution while decreasing the area occupied. As a way to enhance the power performance while reducing area, we propose a bold way to build SAR ADC by using a cyclic DAC, which consumes far less area. However, this design choice is expensive in terms of conversion time and may not be suitable for applications demanding higher data rates. Further, we are optimistic about the possibility of innovating newer topologies of pre-amplifier and dynamic comparators to meet the expected standards.

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