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Original Article

Design and Implementation of Low Power 1 and 2 Trit Multipliers

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Abstract *- Multipliers are combinational logic circuits used in applications like computers, calculators, general-purpose processors and digital signal processors. They are widely used in a variety of signal-processing applications, as 70% of these applications use algorithms which include addition and multiplication operations. In VLSI/embedded applications, power consumption is an important factor to lessen the cost of the chip and enhance battery life. Traditional multipliers are implemented using binary logic, in which each line carries two signal levels, logic 0 or logic 1. In contrast, Ternary logic uses circuits, which carry three levels 0,1, and 2, known as trits. Ternary gates, which are required for ternary multipliers, are implemented using multi-threshold MOSFETs. Leakage current and, hence, static power can be reduced by a forced stack that deploys additional transistors to split the current. In this paper, low-power ternary gates are realized using the forced stack technique. This work mainly designs and implements 1-trit and 2-trit multipliers utilizing low-power ternary logic gates, using Cadence Virtuoso using 45nm Technology. The power of the 1-trit multiplier and 2-trit multiplier is compared with that of its counter binary multipliers, which show reduced power consumption. Further, this work proposes a novel technique to implement a ternary multiplier using Single Pole Triple Throw (SPTT) switches, resulting in a reduced number of transistors.*

Keywords *- Ternary, Multiplier, Low power, Logic Circuit, STI.*

1. Introduction

1.1. Ternary Logic

Conventional logic circuits use two voltage levels called binary data to represent any information. Most of the digital circuits are designed to operate on binary data. Apart from Binary, there exists Multiple-Valued Logic (MVL), where information is represented using multiple voltage levels based on the radix used for representation.

One of the MVLs is called Ternary, where information is represented using three different voltage levels with radix 3. In contrast to binary, every single line in a ternary digital circuit is capable of representing three levels of information 0, 1, 2 [1]. This reduces the frequency of data switching compared to binary digital circuits. In ternary, the decimal value (D) of any n trits can be calculated using Equation (1).

$$D = \sum_{i=0}^{n-1} X_i \ 3^i \quad \text{Where Xi } \epsilon\{0,1,2\} \qquad (1)$$

For example, if 4 trit number 1021 can be converted into a decimal value of 34. In the same way, 34 can be converted into a ternary by successive divisions of 3, considering the reminders. To represent the same in binary, it requires 6 binary digits, each having 2 levels. Whereas in ternary, it requires 4 ternary digits, each having 3 different voltage levels. If an 8-bit microprocessor supports2^8=256 instructions, an 8-tit microprocessor can have 3^8=6561 instructions.

Having an optimum radix of 3, which is close to e=2.718, ternary logic circuits reduce the number of lines/interconnects by 36.9% with its counter-binary circuits [2]. In ternary logic, since the number of signal levels is increased to 3, the number of switching will also be reduced, thereby reducing the Power consumption. A ternary multiplier's fundamental concept is the same as that of a binary multiplier, but it is expected to operate with ternary numbers.

It generates its product as an output after receiving two ternary numbers as inputs. Managing the extra state and guaranteeing accurate multiplication results while taking into account the three potential values for each digit is the biggest problem when building ternary multipliers.

1.2. Ternary Logic Gates

A ternary logic gate takes 2 ternary inputs and produces one ternary output based on the logic. The following truth Table 1 shows the relation between the input and output of Simple Ternary Inverter (STI), Positive Ternary Inverter (PTI)

and Negative Ternary Inverter (NTI) logic gates. The outputs for all these inverters are the same when the input is 0 or 2. It varies only when the input is 1.

Ternary logic functions on two or more inputs are defined as follows:

TAND=X1.X2.X3….Xn= Min(X1,X2,X3…..Xn)

$TAND = \overline{X1.X2.X3 \ldots . . Xn} = \overline{Min(X1, X2, X3 \ldots . . Xn)}$

$TOR = X1 + X2 + X3 + \cdots . Xn = Max(X1, X2, X3, \ldots \ldots Xn)$

$TNOR = \overline{X1 + X2 + X3 + \cdots Xn} = \overline{Max(X1, X2, X3 \ldots . . Xn)}$

$TNOR=\overline{(X1+X2+X3+….+Xn)} = \overline{(Max(X1,X2,X3…..Xn))}$

TXOR=X1 ⊕X2=X1'X2 + X2X1'

Table 2 depicts the truth table of all the 2 input ternary logic gates.

Table 1. Truth table: Ternary inverters

Input (X)	STI	PTI	NTI
0	2	2	2
1	1	2	0
2	0	0	0

Table 2. Truth table: Logic gates

Inputs (A, B)		T-NAND	T-AND	T-NOR	T-OR	T-XOR
0	0	2	0	2	0	0
0	1	2	0	1	1	1
0	2	2	0	0	2	2
1	0	2	0	1	1	1
1	1	1	1	1	1	2
1	2	1	1	0	2	0
2	0	2	0	0	2	2
2	1	1	1	0	2	0
2	2	0	2	0	2	1

1.3. Low Power Techniques in VLSI

In embedded systems, power is regarded as the most significant restriction. High-performance systems require low-power design because excessive power dissipation lowers reliability and raises the cost of packaging, cooling systems, and portable systems.

Multipliers are the building blocks of any processing unit, so there is a potential opportunity to reduce the power of a multiplier. In the VLSI system, static power is mainly caused by leakage current, and dynamic power consumption is directly proportional to the switching frequency of the input.

Various techniques, namely power gating, forced stack, sleepy stack, sleepy stack, and input vector control, are adapted in order to reduce leakage current and hence the static power. A solitary transistor of width W is swapped by a pair of transistors having identical width W/2, which is called the forced stack approach. Forced stacking is seen in Figure 1. During the OFF state, two transistors are switched off simultaneously, and leakage power is minimized because of the reduction in the reverse (V_{gs}) gate to source voltage. But this increases delay and area [7].

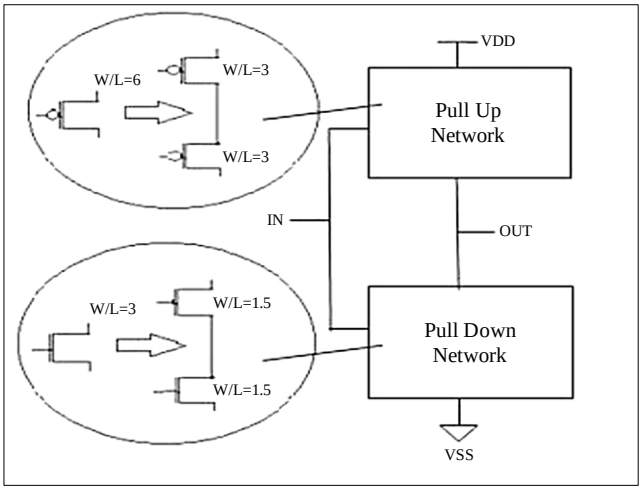


Fig. 1 Forced stack structure in CMOS

2. Literature Review

The recent trends in integrated circuit technology have faced major advancements. One of them is using multi-valued logic circuits, which use two discrete levels of signal. The application includes memories and multipliers. The paper by Kesta focuses on the above mentioned topic. It provides an overview of MVL circuits with the help of information regarding number representation and design of MVL circuits [5].

According to V.T. Gaikwad, about 70% of the space in a VLSI circuit is used for connectivity, 20% for insulation, and 10% is used for devices. A considerable portion of a VLSI device is devoted to interconnect, which limits the binary logic. Compared to multi-valued logic, the designs of ternary-valued logic circuits have been investigated in this paper.

V.T. Gaikwad et al. explore ternary logic gate design in VLSI circuits to address interconnect-related limitations in binary logic. It uses Micro wind EDA tools to simulate CMOS ternary logic gates for potential VLSI implementation, focusing on 45nm technology [3, 11]. Furqan Zahoor et al. [4] present designs for a Ternary logic gate and full adder using Carbon Nanotube Field-Effect Transistors (CNTFET) and

Resistive Random Access Memory (RRAM). These gates offer benefits in terms of chip area, component count, and consumption of power, enabling the implementation of arithmetic modules. Simulations using HSPICE confirm the design's viability.

Author Erfan Shahrom [10] presents a single-bit ternary multiplier that makes use of a Carbon Nanotube Field-Effect Transistor (CNTFET). In order to eliminate direct current from source to ground, the circuit in this paper is intended to allow VDD/2 to be transferred to output directly for logic '1.'

This is accomplished by using two supply voltages, VDD and VDD/2. This is achieved by employing two level output gates and properly dividing the truth table. Ternary approximate full adders are implemented to approximate the result for lower trit positions using CNTFETs [15].

A.P. Dhande, in his paper, discusses the importance of ternary gates in present technology as well as future technology. This paper discusses the simulation of ternary logic gates (TNOT, TNAND, TNOR) by employing the method of injected voltage. The power dissipation is measured using the tanner tool [6].

The author Sneh Lata Murotiya [7] proposed a 4-input Ternary XOR function for carbon nanotube field effect transistors, which possess low power. A unique property of obtaining desired threshold voltage based on the diameter of CNTs has gained immense appreciation for research. The paper further implements the transistor-level Ternary function, thereby drastically reducing the number of transistors and helping attain low-power operation.

The main target of a digital circuit designer is to reduce chip delays and power consumption. Most of the designers sacrificed chip area and power consumption to reduce the delay. The author Ahmet Unutulmaz [8] proposes to combine the threshold logic with the ternary logic. A comparator and arithmetic operators are implemented as subparts of an ALU. With the help of simulations, the author was able to provide evidence that the proposed gate may be utilized to reduce delay, power consumption, and chip area in the ternary circuits.

The paper by G. Thrishala et al. focuses on the implementation of ternary digital circuits for VLSI applications. Ternary logic uses three symbols, 0, 1, and 2, and has more advantages over binary logic in digital circuit design. The paper proposes the implementation of a half adder using a ternary 3:1 multiplexer. It compares the ternary half-adder design using the k-map method. The proposed technique using Mux is analyzed in terms of propagation delay, power dissipation, and transistor count.

The paper also discusses the design and realization of ternary inverters, gates, decoders, and the results of the proposed ternary half-adder circuit [9]. Ternary gates are also designed and implemented using Graphene Nano Ribbon Field Effect Transistor (GNRFET) and FinFETs [12, 13]. Novel techniques are used to implement Ternary full adder and multiplier [14]. Fast ternary adders are proposed, and ternary multipliers are implemented using multi-threshold MOSFETS [16].

3. Methodology

In digital systems, multipliers are most frequently utilized to carry out the various algorithms in a variety of applications, particularly in the area of digital signal processing. In this work, 1-trit ternary multipliers are realized using two different techniques:

i) Using Ternary logic expressions
ii) Using Single Pole Multiple Throw (SPMT) switches.
iii) Further, 1-trit multipliers are cascaded to realize 2-trit ternary multipliers and the DC power is compared with a 3-bit binary multiplier.

3.1. Single Trit Ternary Multiplier Using Logic Expressions

3.1.1. Low Power Ternary Gates

As discussed in Section 1.2, the functionality of ternary logic gates required for multipliers is implemented using Multi-threshold voltage MOSFETs (MVTs) [3]. MOSFETs of two different threshold voltages, 0.9V (High MVT) and 0.4V (Low MVT), are used along with the forced stack technique to obtain Low Power ternary gates.

Three different output voltage levels of 0V, 0.9V and 1.8V are generated at the output corresponding to logic levels 0,1and 2. As discussed in Section 1.3, in pull-up and pull-down structures, each of the transistors is replaced by two identical transistors to reduce the leakage power [6, 7].

The implementation of low-power STI, PTI, and NTI is shown in Figure 2. The implementation of low-power Ternary NAND and NOR gates is shown in Figure 3 and Figure 4. AND and OR gates are obtained by cascading these gates with STI.

3.1.2. Ternary Decoder

The ternary decoder circuit (Figure 5) has one input and 3 outputs, which are either at 0 or 2. It decodes single ternary input to unary output, as per the truth table. As shown in Table 3, when Vin is 0, 1, 2, the corresponding decoded outputs Vout0, Vout1, and Vout2 will be 2.

In expressions 2 and 3, A0, A1, A2, and B0, B1, and B2 are generated using decoders from single inputs of A and B that have 3 different voltage levels.

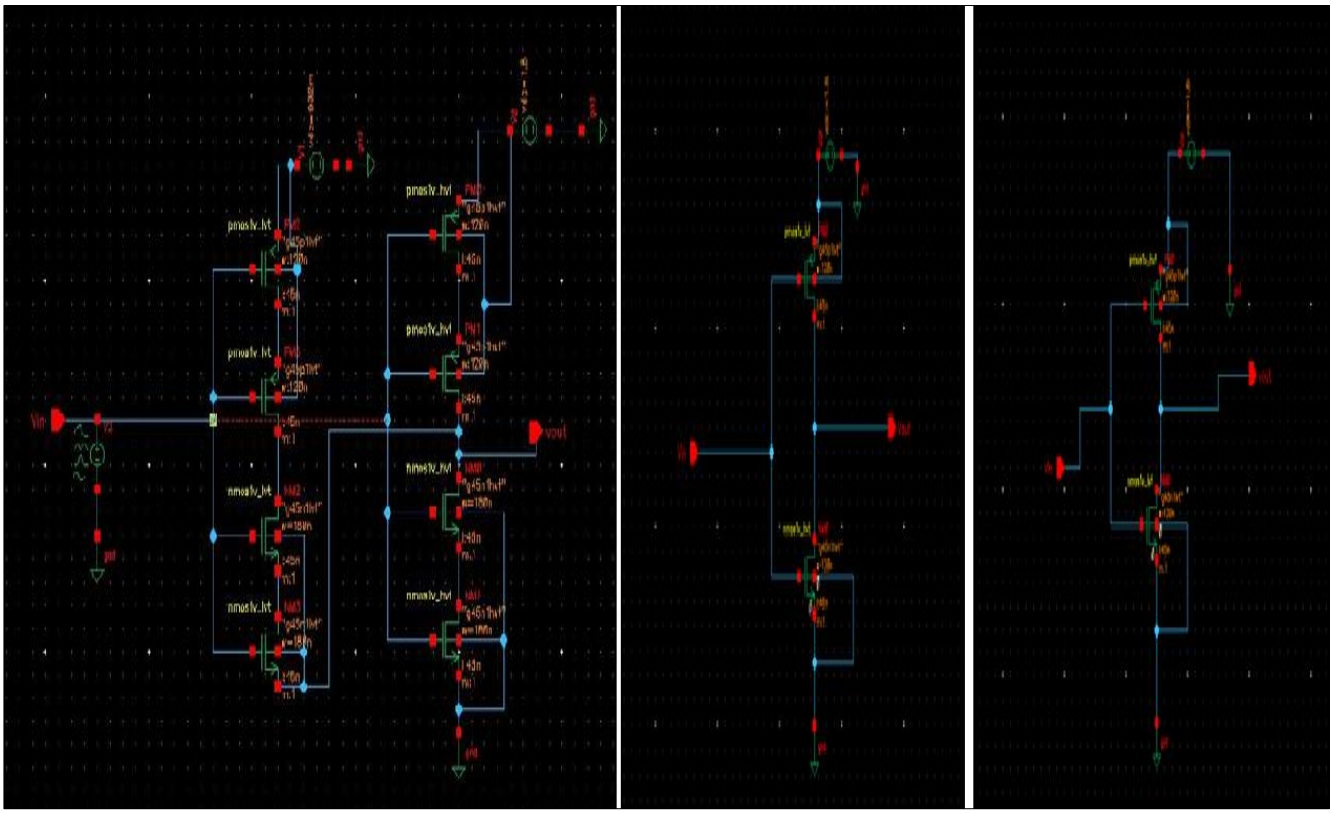


Fig. 2 Schematics of forced stack ternary STI, PTI and NTI

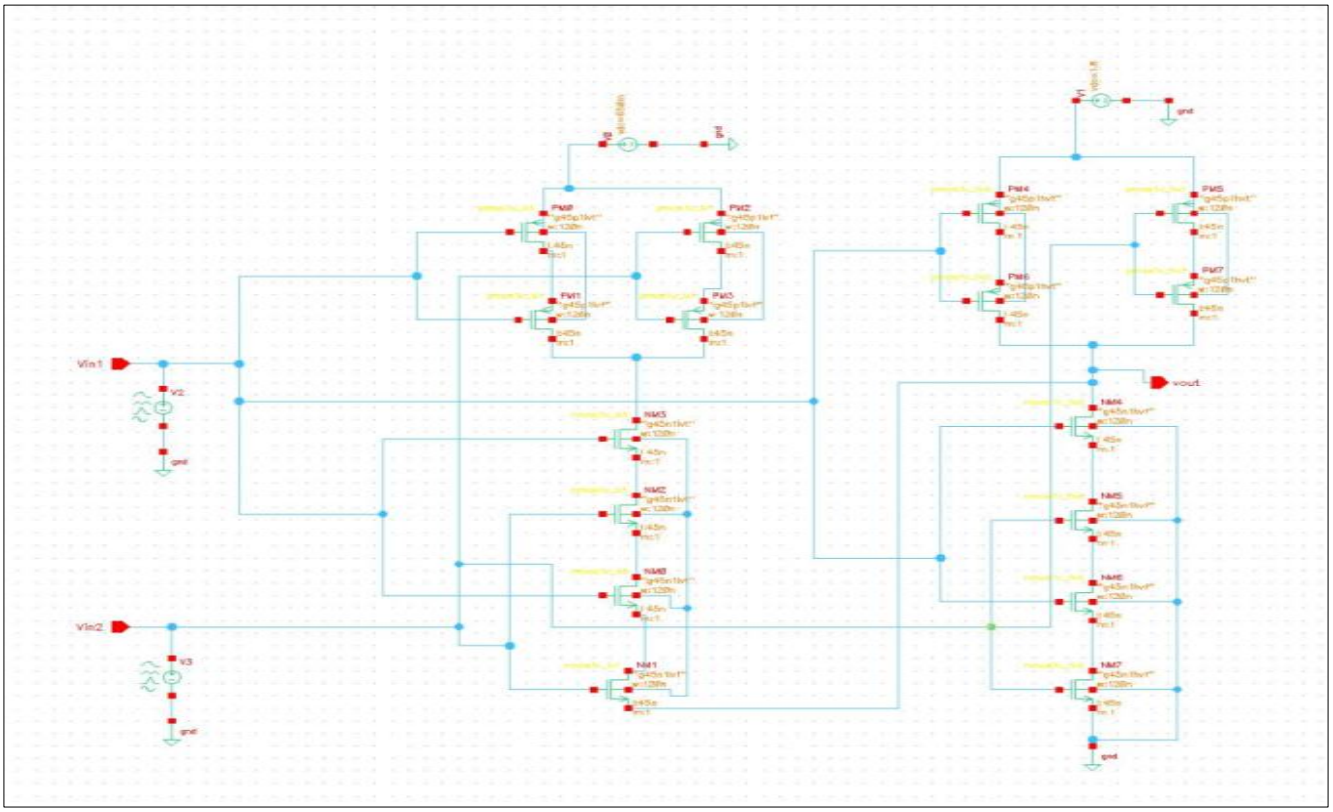


Fig. 3 Schematics of forced stack ternary NAND gate

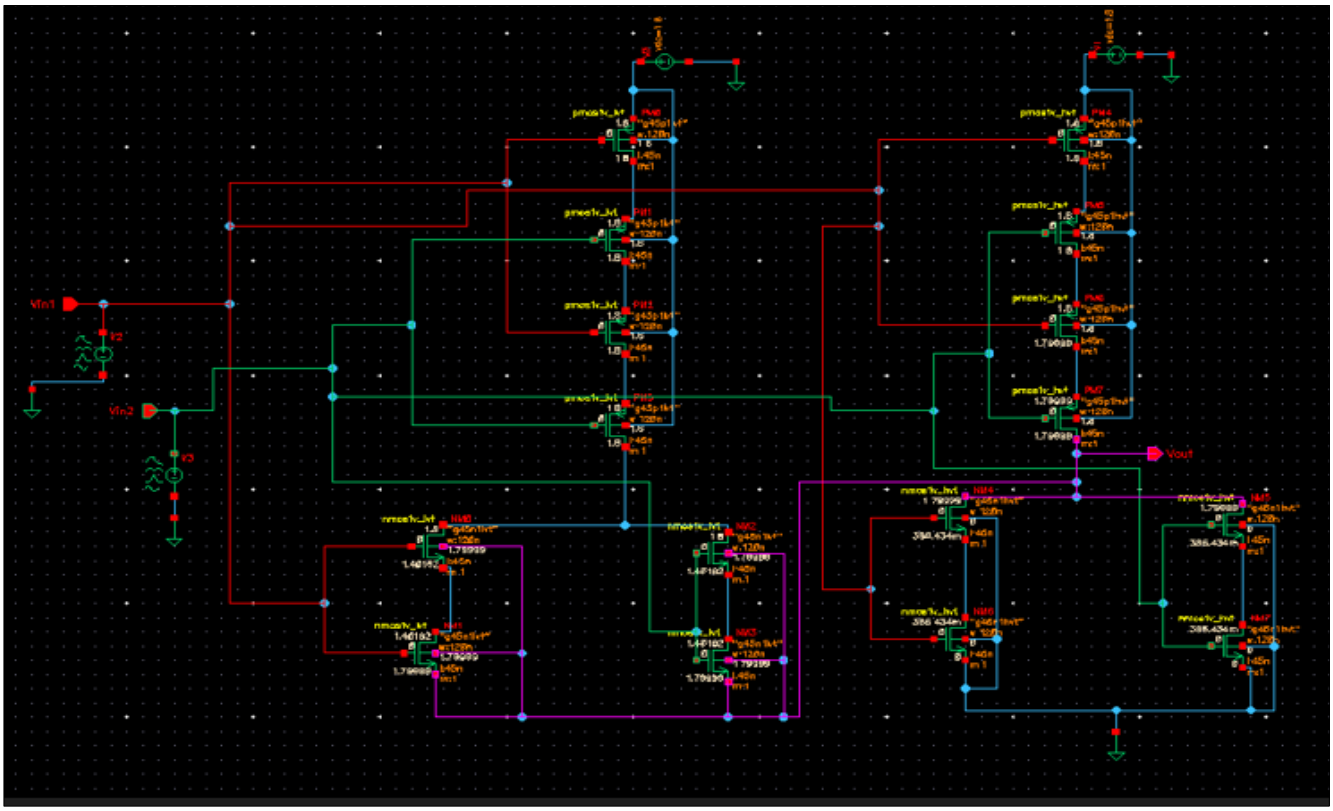


Fig. 4 Schematics of forced stack ternary NOR gate

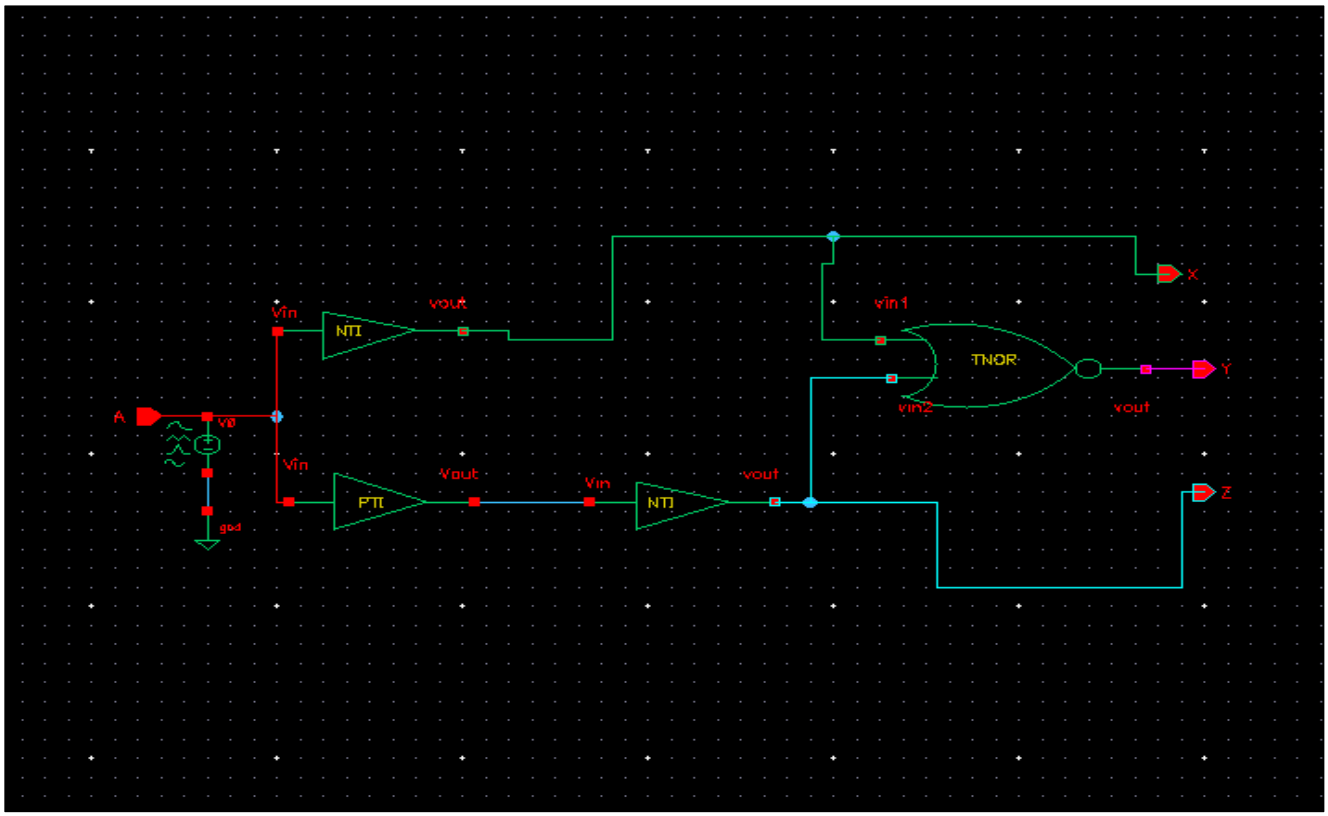


Fig. 5 Schematics of ternary decoder

Table 3. Ternary decoder truth table

Vin	Vout0	Vout1	Vout2
0	2	0	0
1	0	2	0
2	0	0	2

3.1.3. Realization of 1-Trit Ternary Multiplier

Table 4 shows the truth table to realize the proposed 1-trit multiplier, each input having logic '0','1' and '2' levels. This truth table has 3^2=9 combinations in contrast to 2^2=4 combinations in binary counterpart.

Table 4. 1-trit ternary multiplier truth table

A	B	Product	Carry
0	0	0	0
0	1	0	0
0	2	0	0
1	0	0	0
1	1	1	0
1	2	2	0
2	0	0	0
2	1	2	0
2	2	1	1

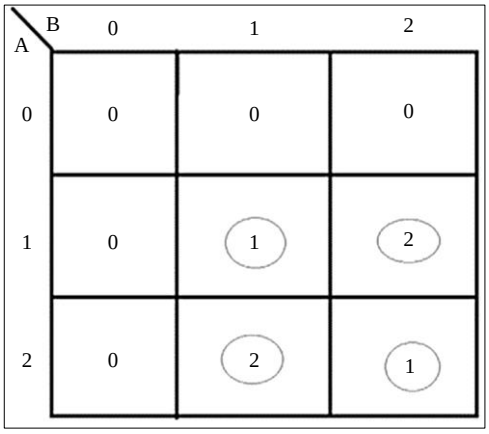


Fig. 6 k-map

From the truth table, ternary logic expressions are realized for the product (PP0) and carry (PP1) by grouping the logic levels in the k map, as shown in Figure 6.

The expression obtained for product (PP0) and carry (PP1) are as follows:

$$PP0 : A^2B^1 + A^1B^2 + 1.(A^1B^1 + A^2B^2) \quad (2)$$

$$PP1 : 1.(A^2B^2) \quad (3)$$

To implement ternary logic expressions 2 and 3, we need decoded inputs, i.e. A^0, A^1, A^2 and B^0, B^1, and B^2 which are generated by decoders. The following diagrams in Figure 7 show the block diagram of the ternary multiplier, which requires TNAND, TNOR, STI, PTI, and NTI gates as well as a Ternary decoder. These gates are realized with the Forced Stack technique to implement low power ternary multiplier, as elaborated in earlier sections.

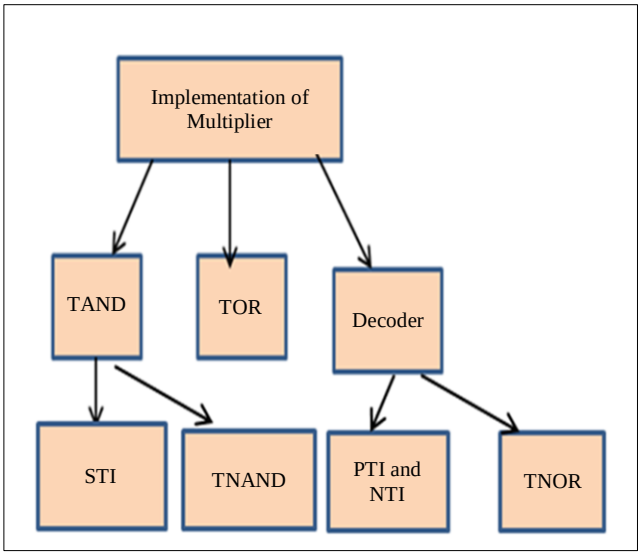


Fig. 7 Implementation of 1-trit multiplier

3.2. Single Trit Ternary Multiplier Using SPMT Switches

A Single Pole Multiple Throw (SPMT) switch has a single port as input and connects one of the ports among multiple output ports. An alternate approach is used to obtain the product of a 1-trit multiplier using SPMT switches. From the truth Table 4 of the multiplier, it is observed that PP1 is 0 for all the combinations except for A=2 and B=2. Hence, the SPDT switch is used to switch between 1 and 0 depending on the input combinations.

The Value of PP0 is obtained using Ternary AND gate as a primary component. Further, based on the specific input combinations, operations are controlled using SPMTs. The table depicts the implementation of a multiplier using these switches. This reduces the transistor count compared to an implementation using logical expressions, as in Table 5. This technique uses 5 low power ternary AND gates and two SPMT switches, as shown in Figure 9. Table 5 depicts the implementation of multiplier using these switches.

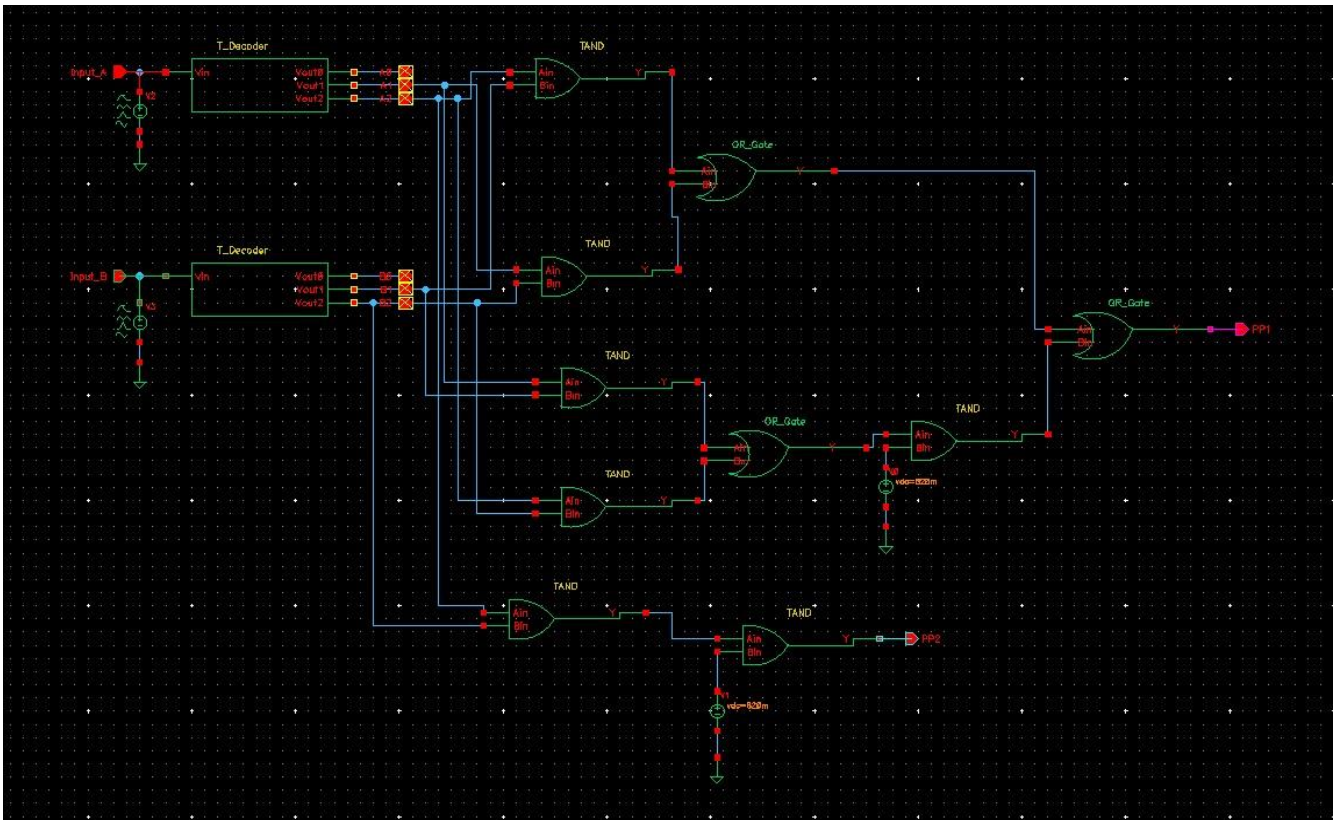


Fig. 8 Schematic of 1-trit multiplier

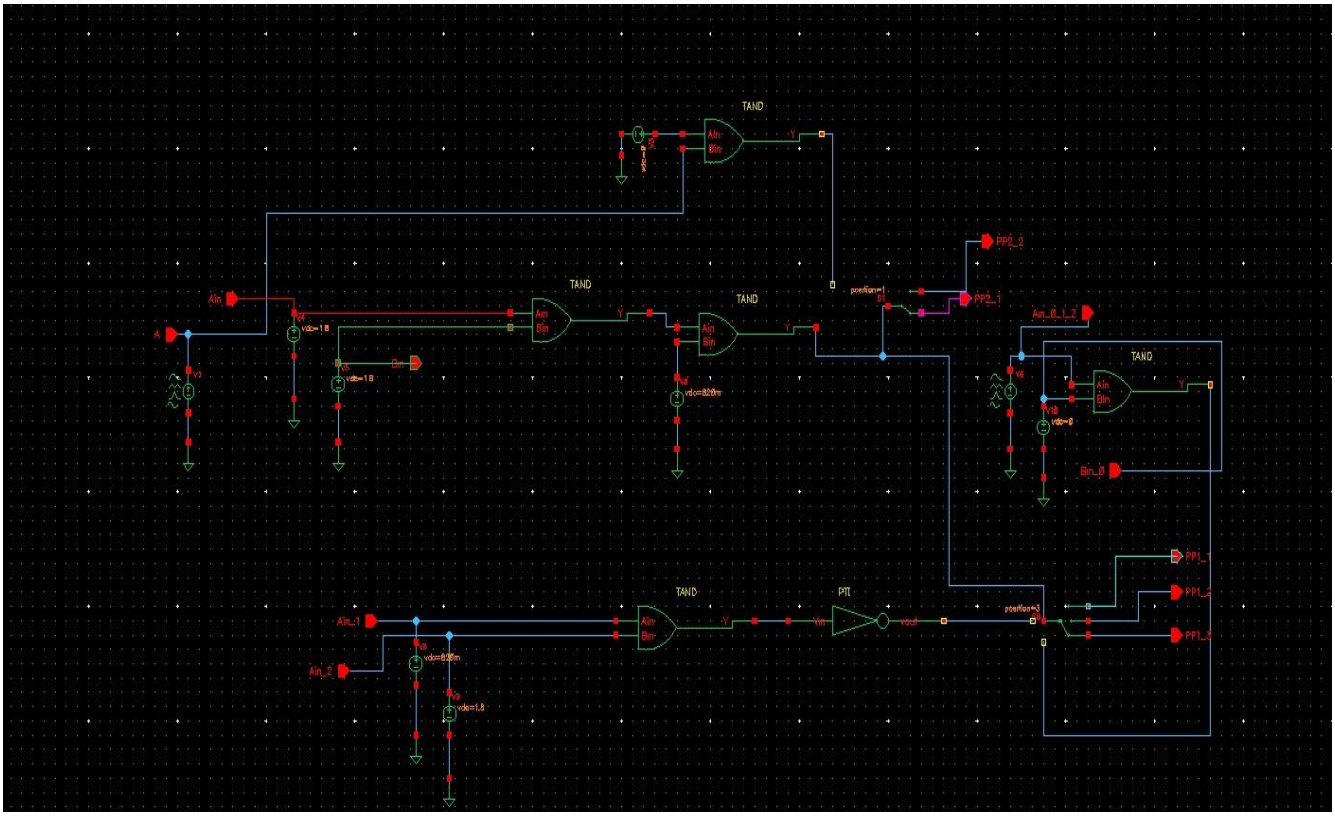
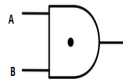
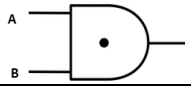
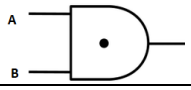
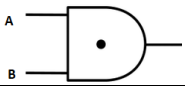
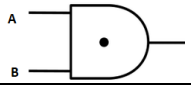
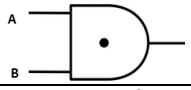
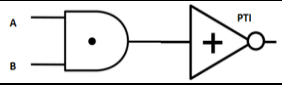
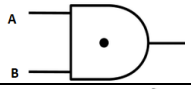
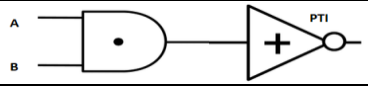
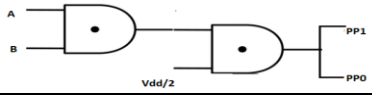


Fig. 9 Schematic of 1-trit multiplier using SPMT switches

Table 5. Reduction of gates

A	B	Ternary AND Gate 	Modular Product		Logic Circuit for Obtaining Partial Product
			PP1	PP0	The Value of PP0 is obtained using ternary AND gate as a primary component. Further based on the specific input combinations, operations are controlled using single pole multiple throw switches.
0	0	0	0	0	
0	1	0	0	0	
0	2	0	0	0	
1	0	0	0	0	
1	1	1	0	1	
1	2	1	0	2	
2	0	0	0	0	
2	1	1	0	2	
2	2	2	1	1	

3.3. Two-Trit Ternary Multiplier by Cascading 1-Trit Multiplier

3.3.1. 2-Trit Multiplier Realization

The proposed 2-trit multiplier is realized using 1-trit multipliers and Ternary Half Adders (THA), as seen in Figure 10. It requires 4 single trit multipliers to multiply each of the two trits of input A with two trits of input B. Intermediate partial products thus obtained from each multiplier are added using half adders. Each half adder realized using 18 two input ternary AND and OR gates (Figure 11) adds 2 trits of the same place value (3^i). This design requires a total of 10 half-adders, consuming 180 gates, as shown in Figure 12. 2-trit multipliers can also be implemented using 4 single trit multipliers, 3 full adders and 1 half adder. Each full adder is realized with 41 three-input ternary logic gates, which increases the transistor count. The functionality of THA is shown in the Table 6. Functionality is designed using low power AND and OR gates, as shown in Figure. This is implemented as per the logical expression.

$$Sum= A^0B^2 + A^2B + A^1B^1 + 1.(A^0B^1 + A^1B^0 + A^2B^2)$$

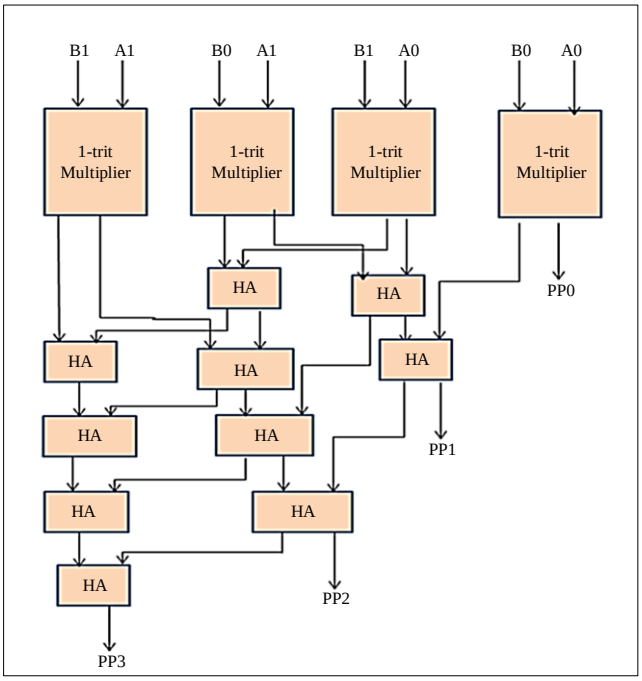


Fig. 10 2-trit multiplier using 1-trit multipliers and half adders

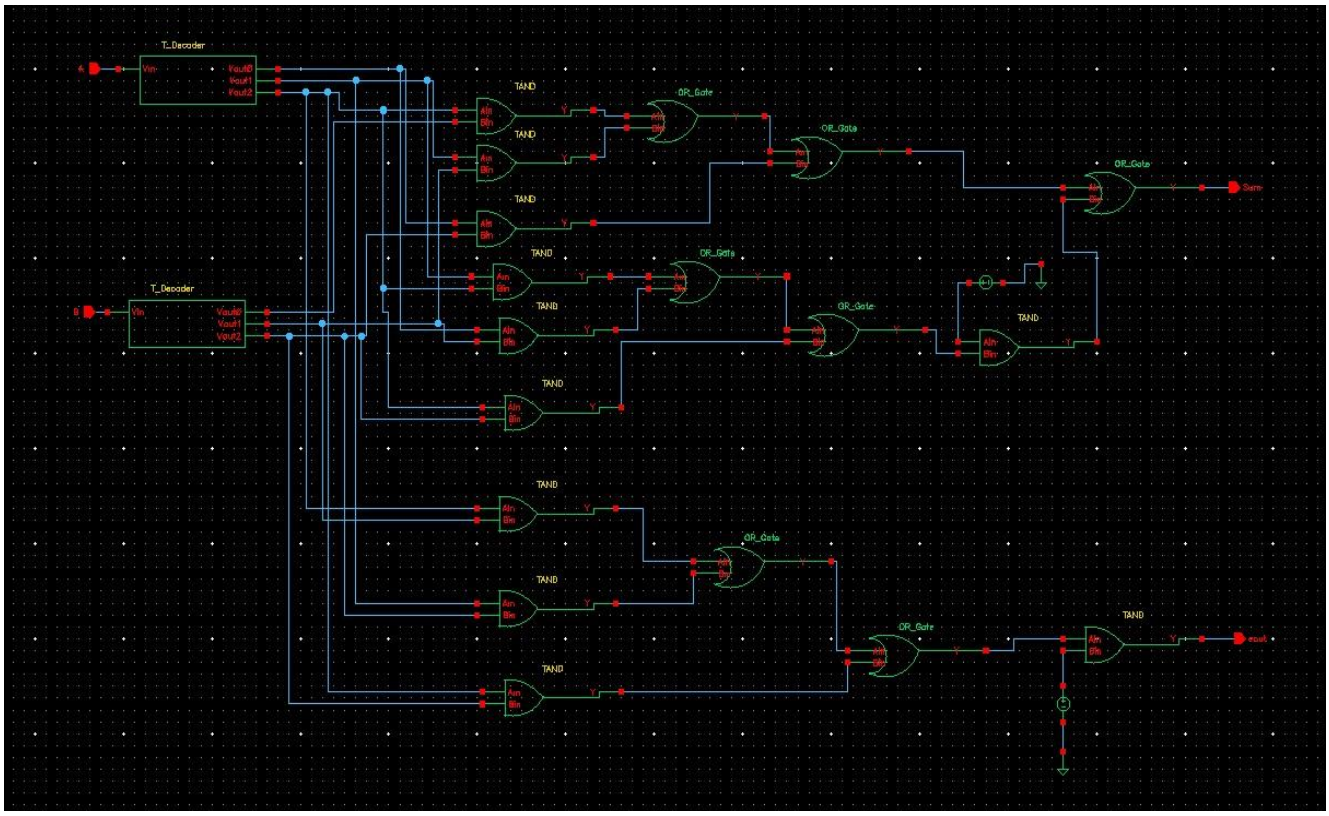


Fig. 11 Schematic of ternary half adder

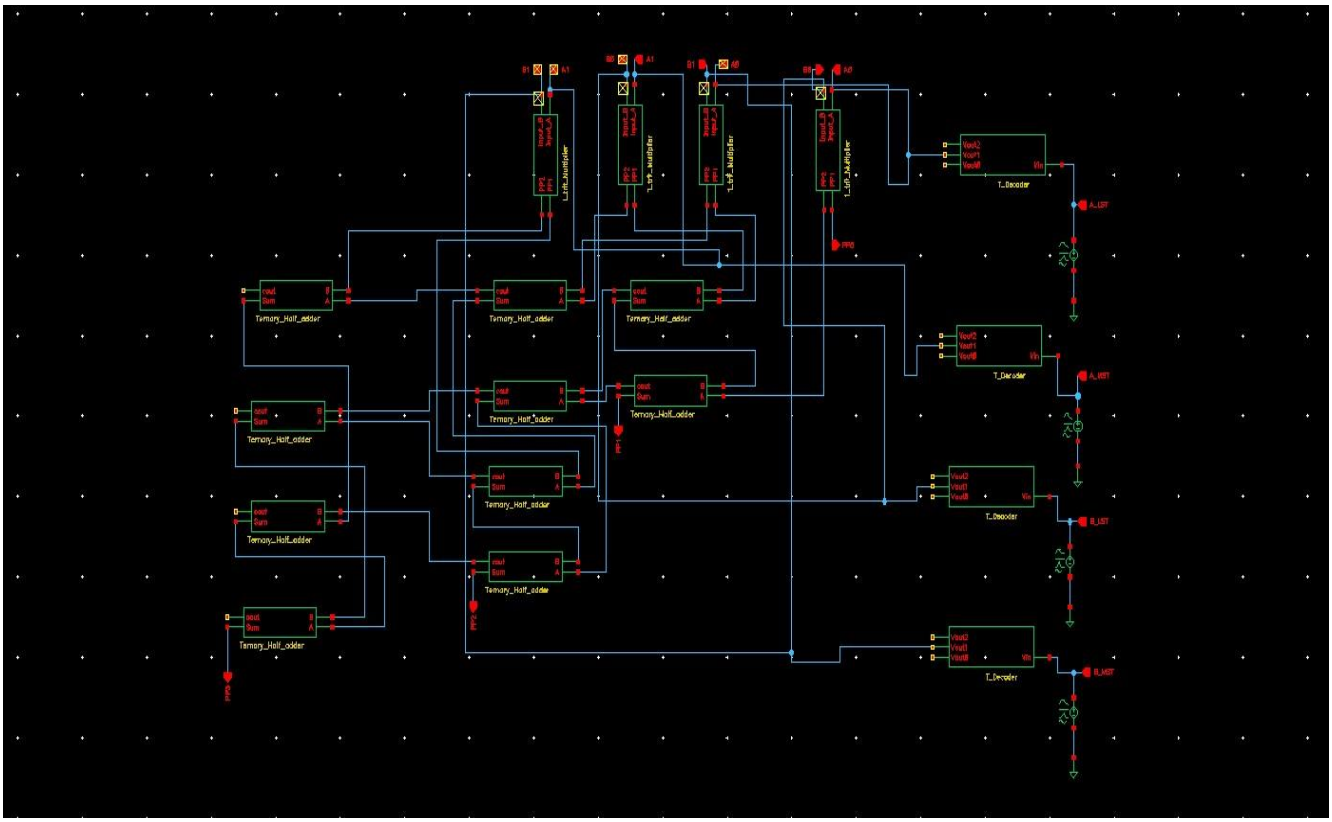


Fig. 12 Schematic of 2-trit multiplier

Table 6. Truth table: THA

Inputs (A, B)		Sum	Carry
0	0	0	0
0	1	1	0
0	2	2	0
1	0	1	0
1	1	2	0
1	2	0	1
2	0	2	0
2	1	0	1
2	2	1	1

3.3.2 Two-Bit and Three-Bit Binary Multipliers

A 1-trit multiplier is compared with a 2-bit binary multiplier as a 1-trit could hold more data than binary. In the same way, a 2-trit multiplier is compared with a 3-bit binary multiplier. The schematic for two and three-bit multipliers are as follows:

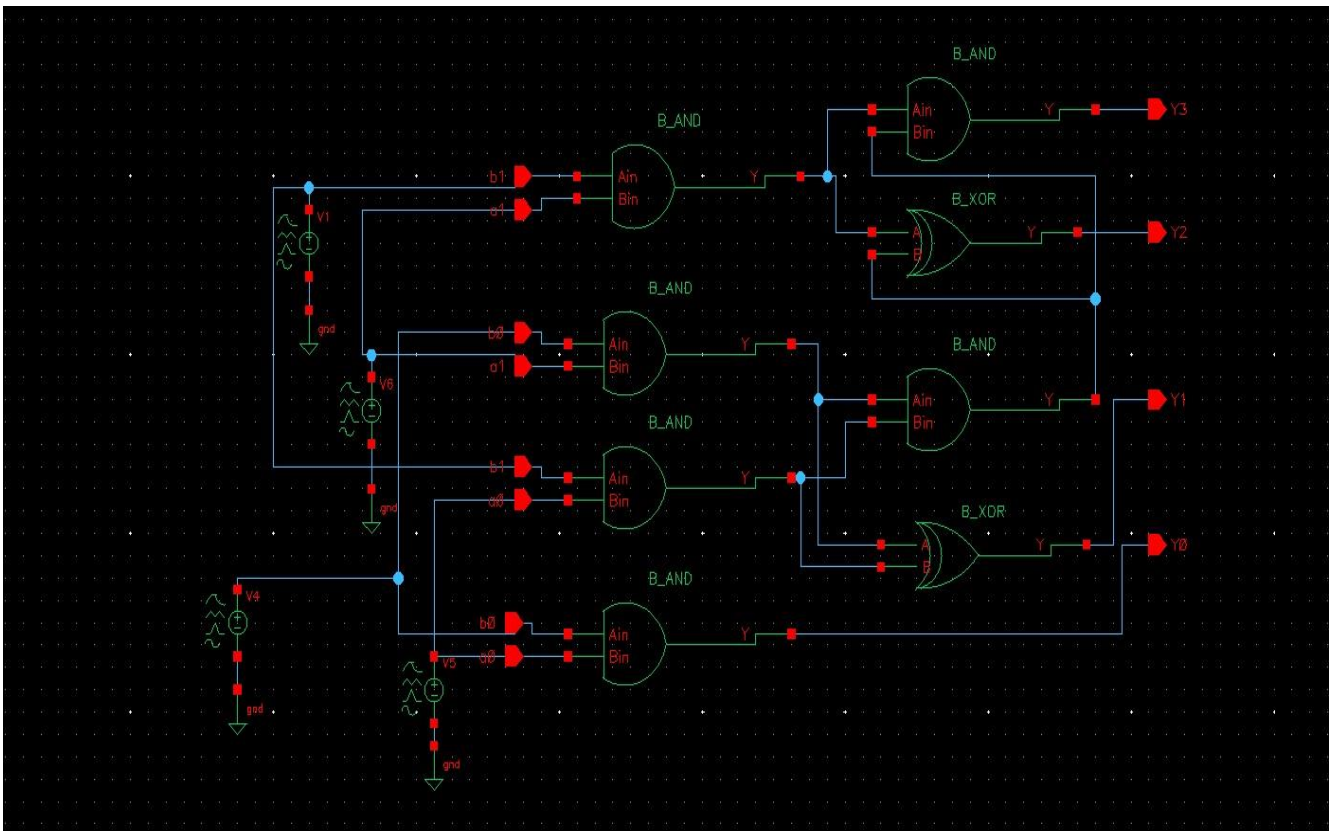


Fig. 13 Schematic of 2 bit binary multiplier

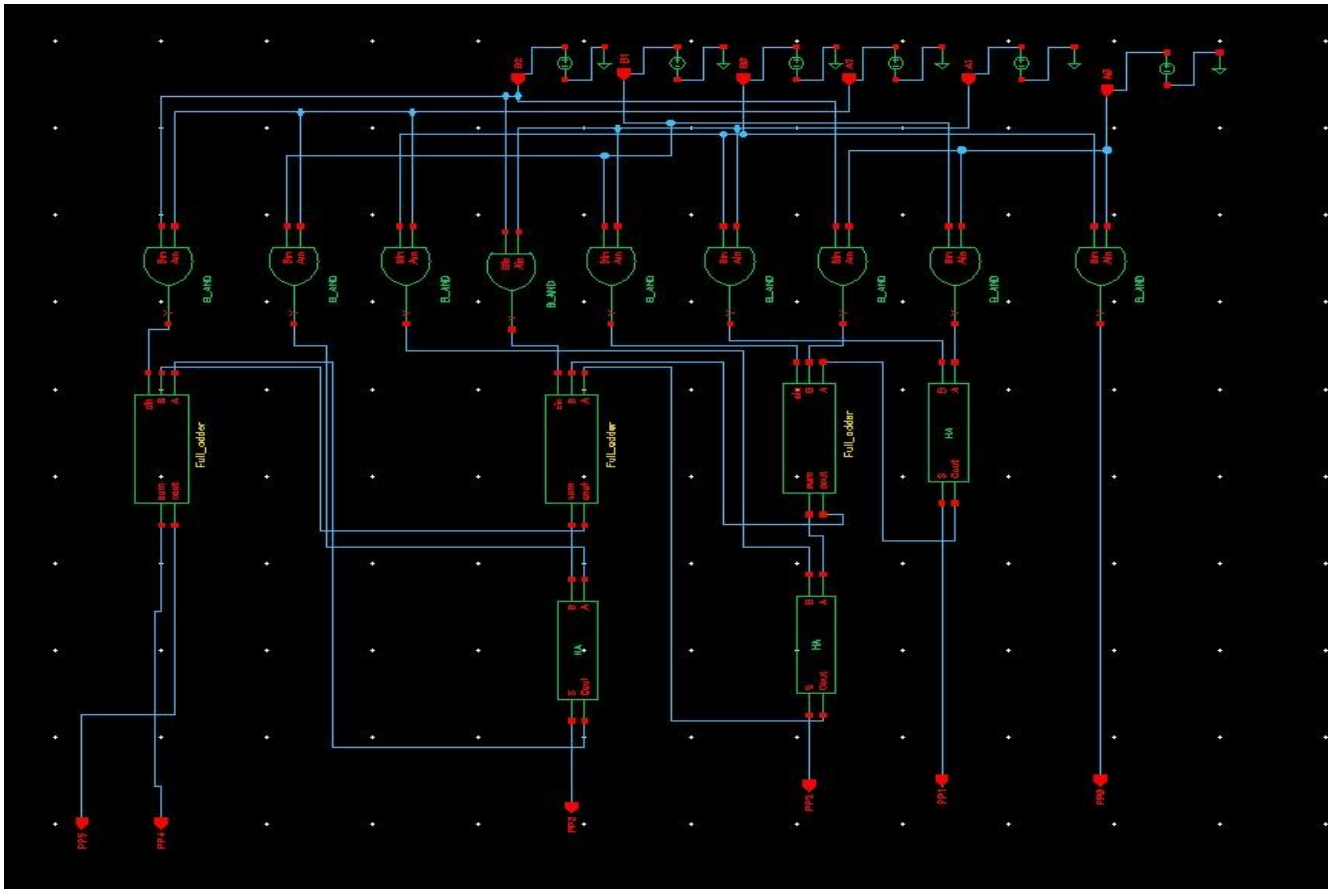
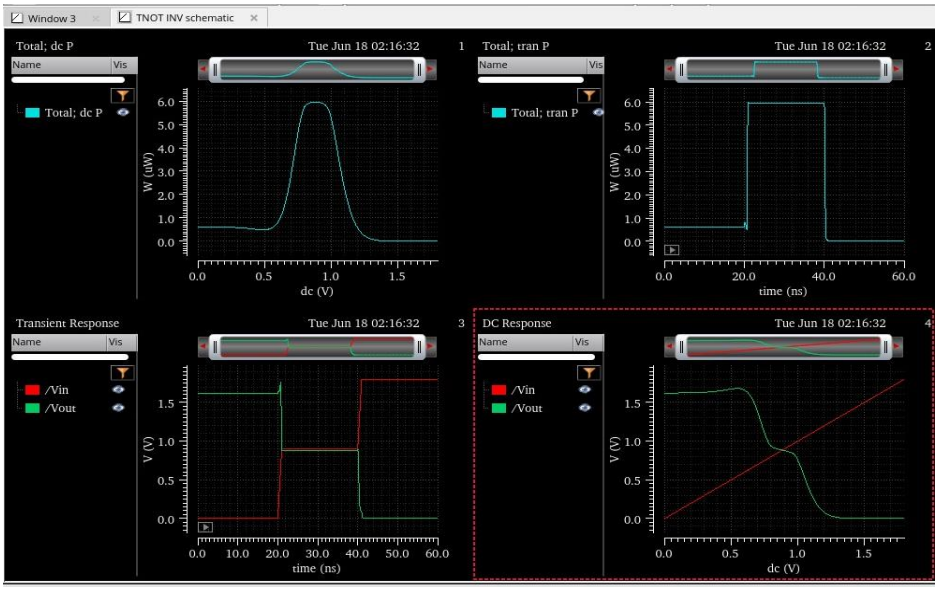


Fig. 14 Schematic of 3 bit binary multiplier



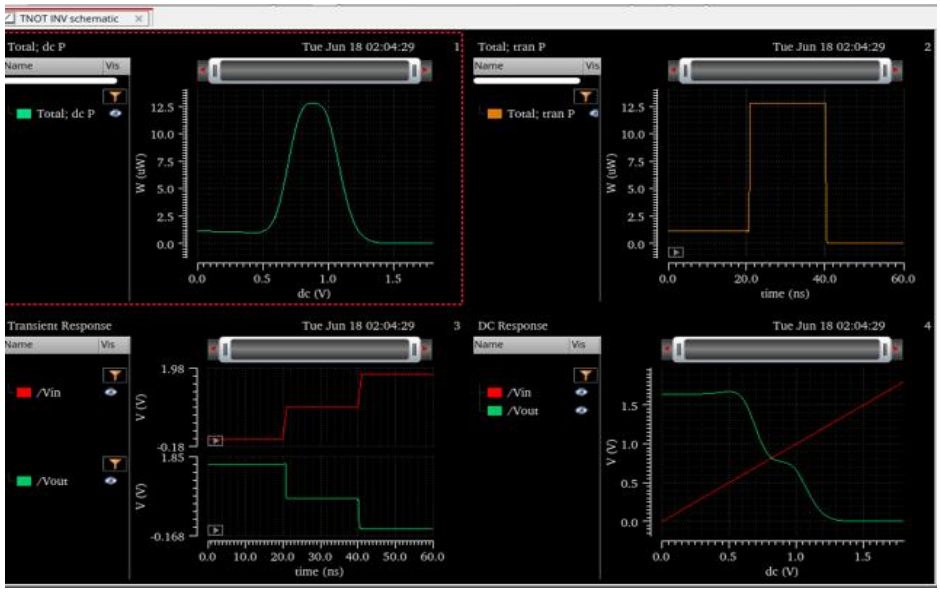


Fig. 15 DC and transient power of STI with forced stack and without forced stack

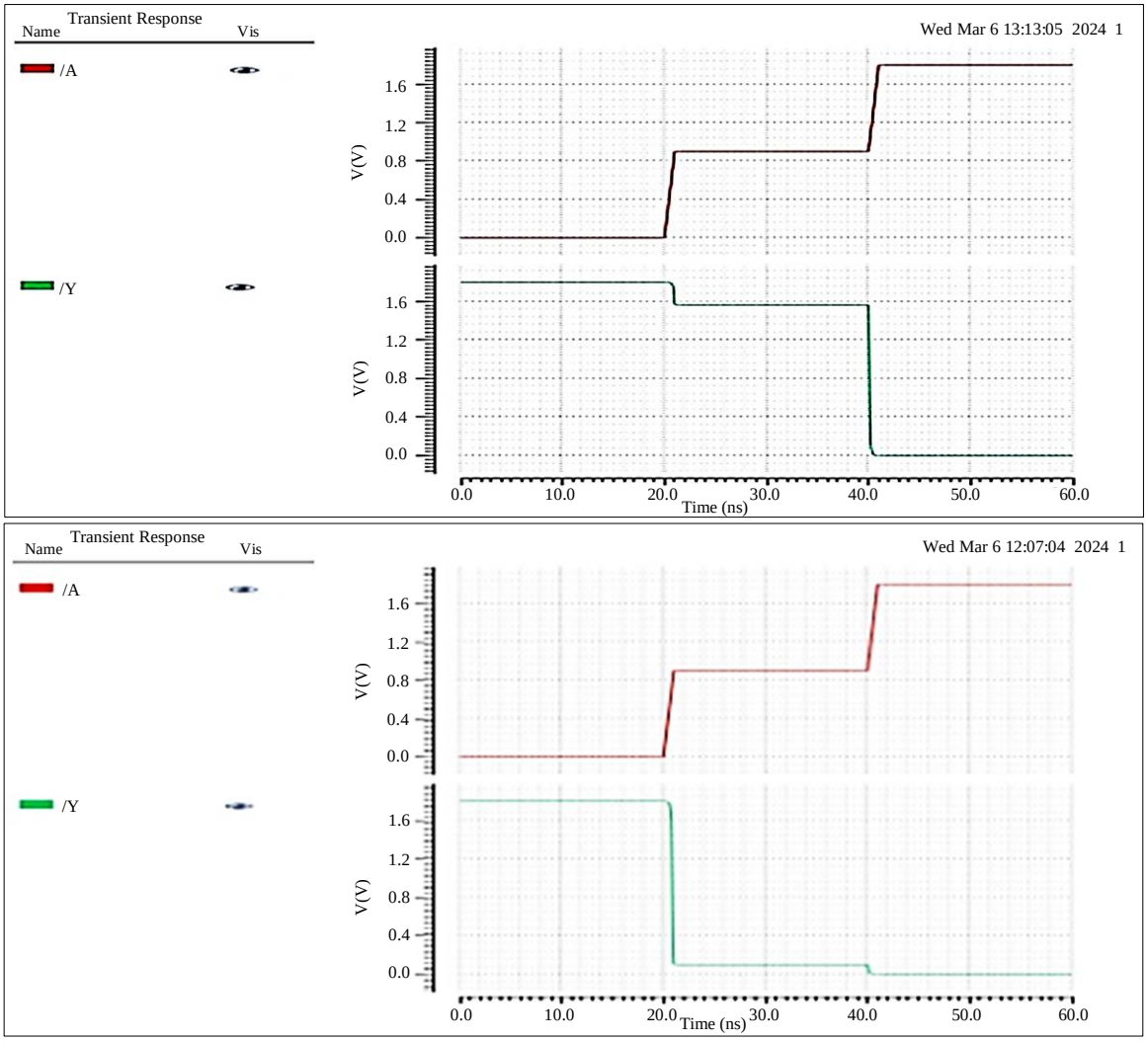


Fig. 16 Transient response of PTI and NTI

4. Results and Discussions

4.1. Transient Response of Ternary Inverters

Figure 15 shows the output of STI using the forced stack technique. When the input of the inverter is at 0V, 0.9V and 1.8V, the output will be 1.8V, 0.9V and 0V, as per Table 1. DC and Transient power of the conventional STI and forced stack low power STI are 12.5 µW and 6.0 µW, respectively. Figure 16 shows the responses of PTI and NTI for three different levels of input voltages. The output of PTI will be at 1.8V when the inputs are less than 1.8V, and the output will be 0V when the input voltage is 1.8V. Similarly, the output of PTI will be at 0V when the inputs are greater than 0V, and the output will be 1.8V when the input is at 0V (Section 1.2).

4.2. Ternary NAND and NOR Gates

Figure 17 shows the transient responses of TNAND and TNOR gates. This follows the functionality as per the truth table discussed in Section 1.2. The figure shows the response of TNAND when the inputs are at logic 0 and logic 1, forcing the output to logic 2 (as pointed out by the pointer). In TNOR, the outputs are at logic 2, logic 1, and logic 0, while the inputs are at logic 0, logic 1, and logic 2, respectively.

4.3. Ternary Decoder

Figure 18 shows that when the input of the decoder is at logic 0, logic 1 and logic 2, the respective decoded outputs X, Y and Z produce output logic 2.

4.4. Single Trit Multiplier Using Logical Expressions

The Figure 19 shows the input/output response for a 1-trit multiplier. When the inputs are at logic 1, PP0 will be at 1, and PP1 will be at 0 as $1X1=(01)_3$. Whereas when the inputs are at logic 2, both PP0 and PP1 will be at logic 1(voltage ranging 0.5 V to 0.9V), as $2X3^0+2X3^0=2X2=4=3^0X1+3^1X1=(11)_3$.

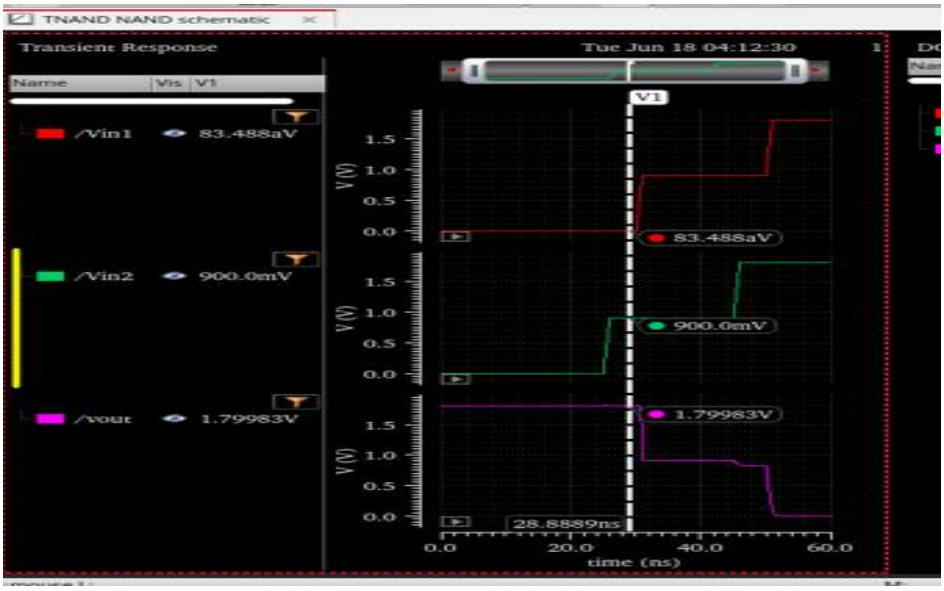
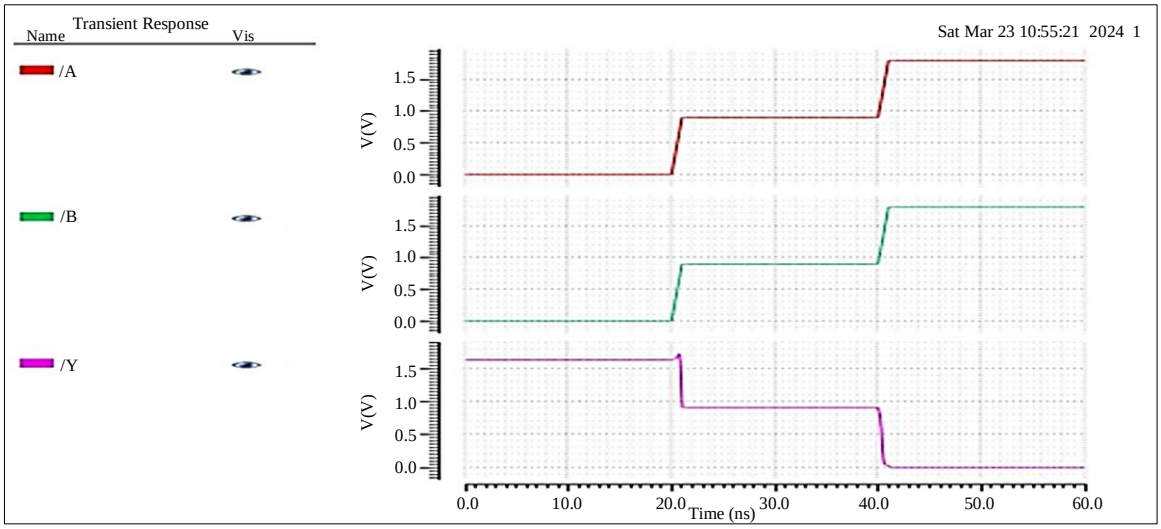


Fig. 17 Transient response of TNAND and TNOR gates



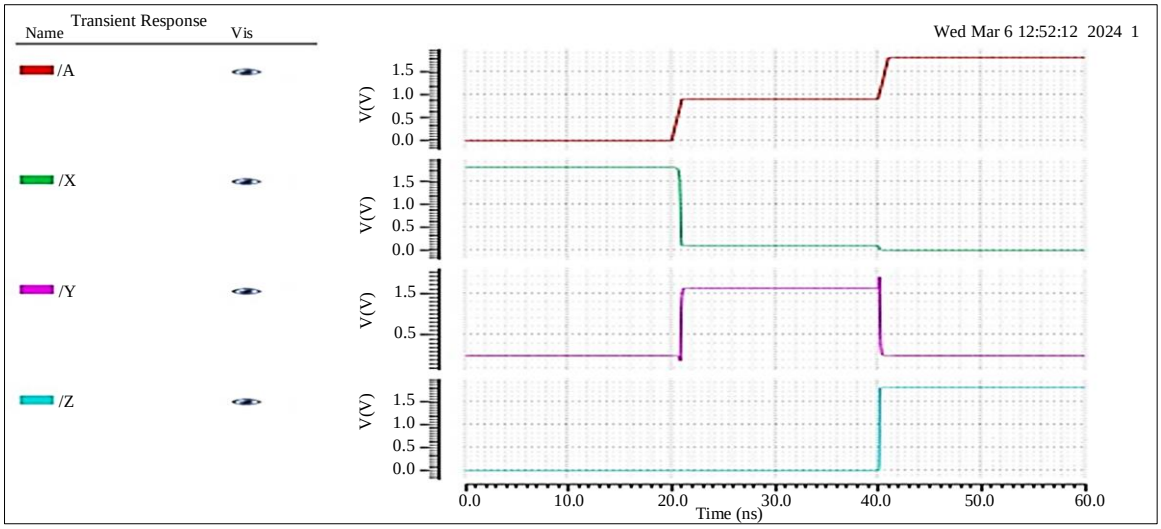


Fig. 18 Transient response of ternary decoder

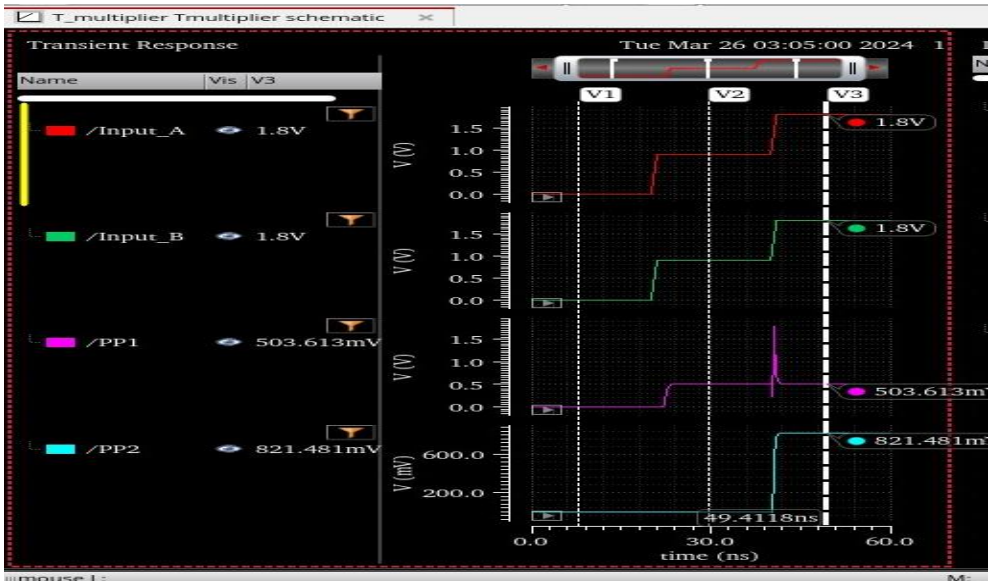


Fig. 19 Output response of Single trit multiplier using logical expressions

4.5. Single Trit Multiplier Using SPMT Switches

The outputs of the SPMT switch based on a 1-trit multiplier for different logic level inputs are shown in Figure 20.

4.6. Ternary Half Adder (THA)

THA is implemented to construct a 2-trit multiplier using 1-trit multipliers. The output of THA is shown in Figure 21, which follows the truth Table 6. The inputs at logic 0, logic 1, and logic 2 force the Sum to logic 0, logic 2, and logic 1, respectively, and carry to logic 0, logic 0, and logic 1, respectively.

4.7. Two Trit Multiplier

Figure 22 shows the response for two trit multipliers when the inputs A_1A_0 and B_1B_0 are at maximum, i.e. at logic 2. This producing result of $(22)_3X(22)_3=(64)_{10}=(2101)_3$ and hence making PP0,PP1,PP2 and PP3 at logic levels logic 1,0,1 and 2 respectively.

4.8. Binary Multipliers

Figure 23 shows the response for two-bit and three-bit binary multipliers. When the binary inputs $A_2A_1A_0$ and $B_2B_1B_0$ are at logic 1, they produce the result of $(111)_2X(111)_2=7X7=49=(110001)_2$. It is evident that to multiply the same value in binary, we require 3 bits as inputs and 6 bits as outputs, whereas in ternary, we require 2 trits as inputs and only 4 trits as outputs.

4.9. Power Analysis of Binary and Ternary Multipliers

DC and Transient Power of 3-bit Binary and 2-Trit Ternary multipliers are depicted in Figure 24. It is noticed that the total power in the 3-bit binary multiplier is 700.005µW, and the 2-trit multiplier is 570µW.

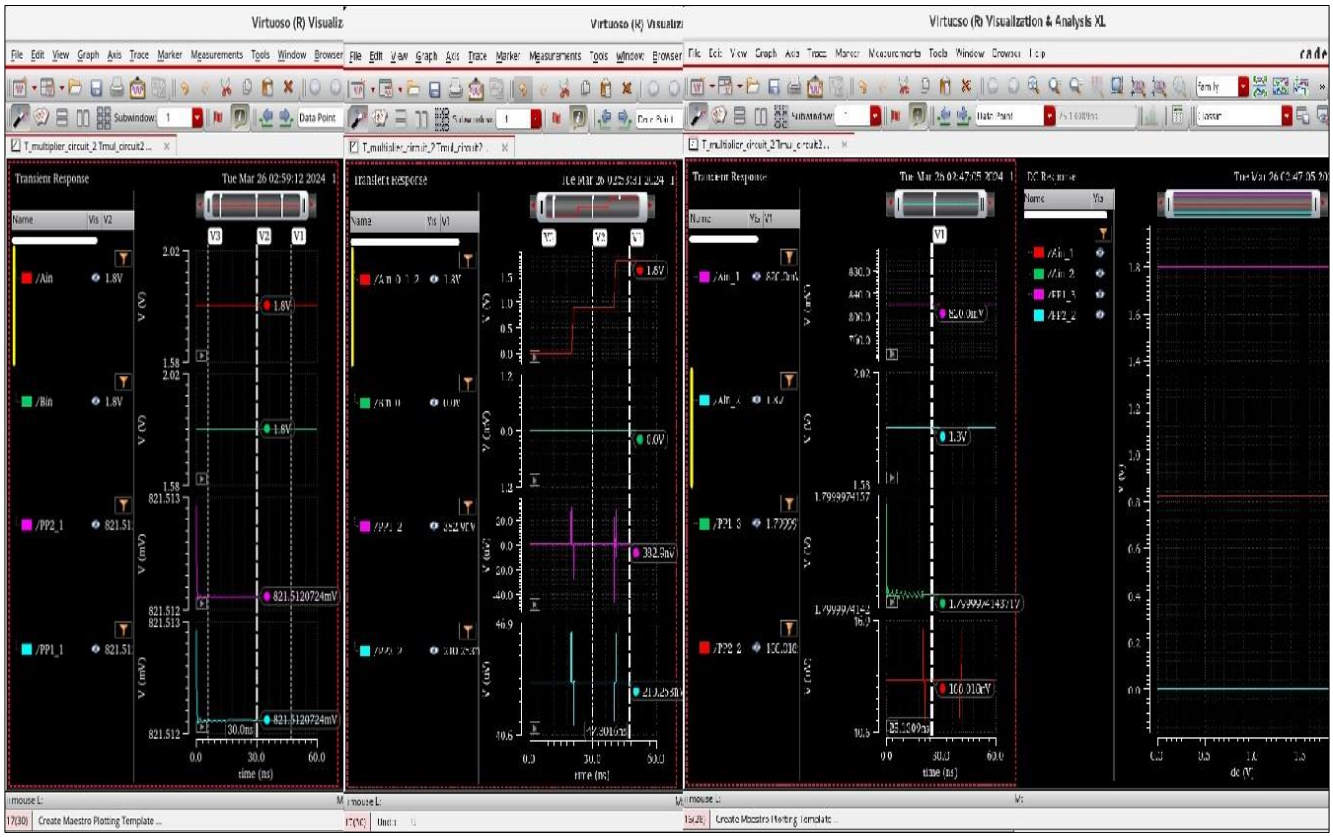


Fig. 20 Output response of single trit multiplier using SPMT switches

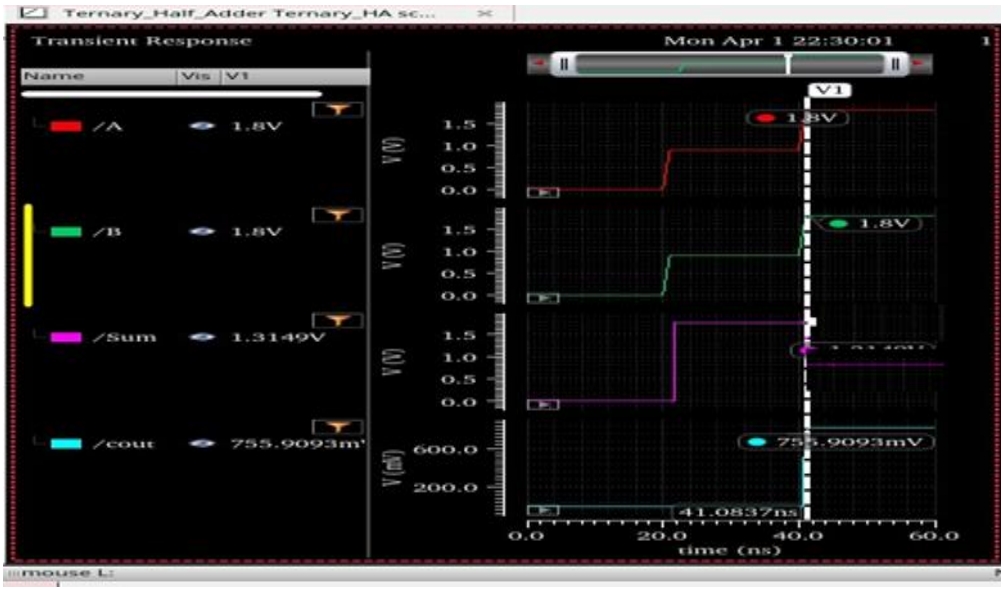


Fig. 21 Output response of ternary half adder

Fig. 22 Output response of 2 trit multiplier

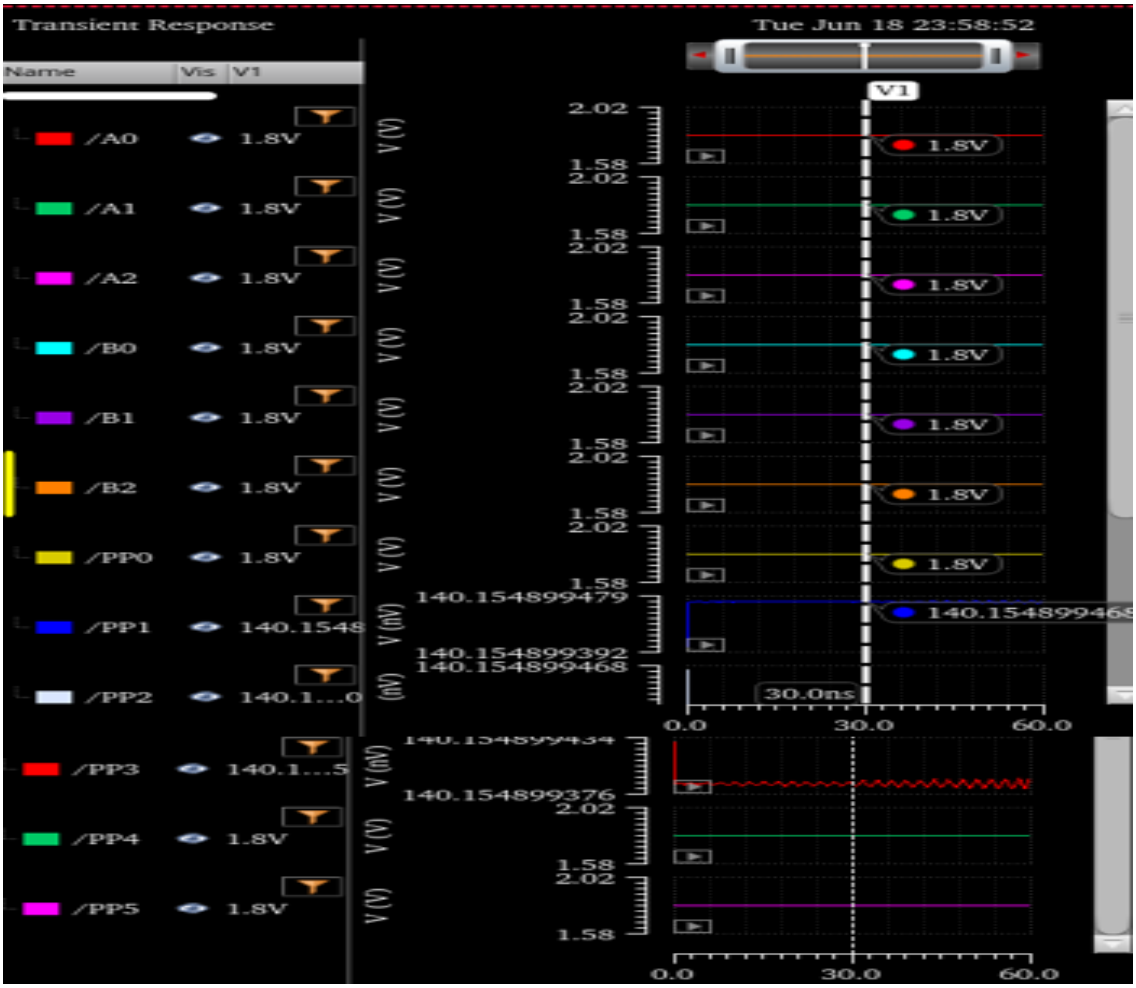


Fig. 23 Output response of 3 bit binary multiplier

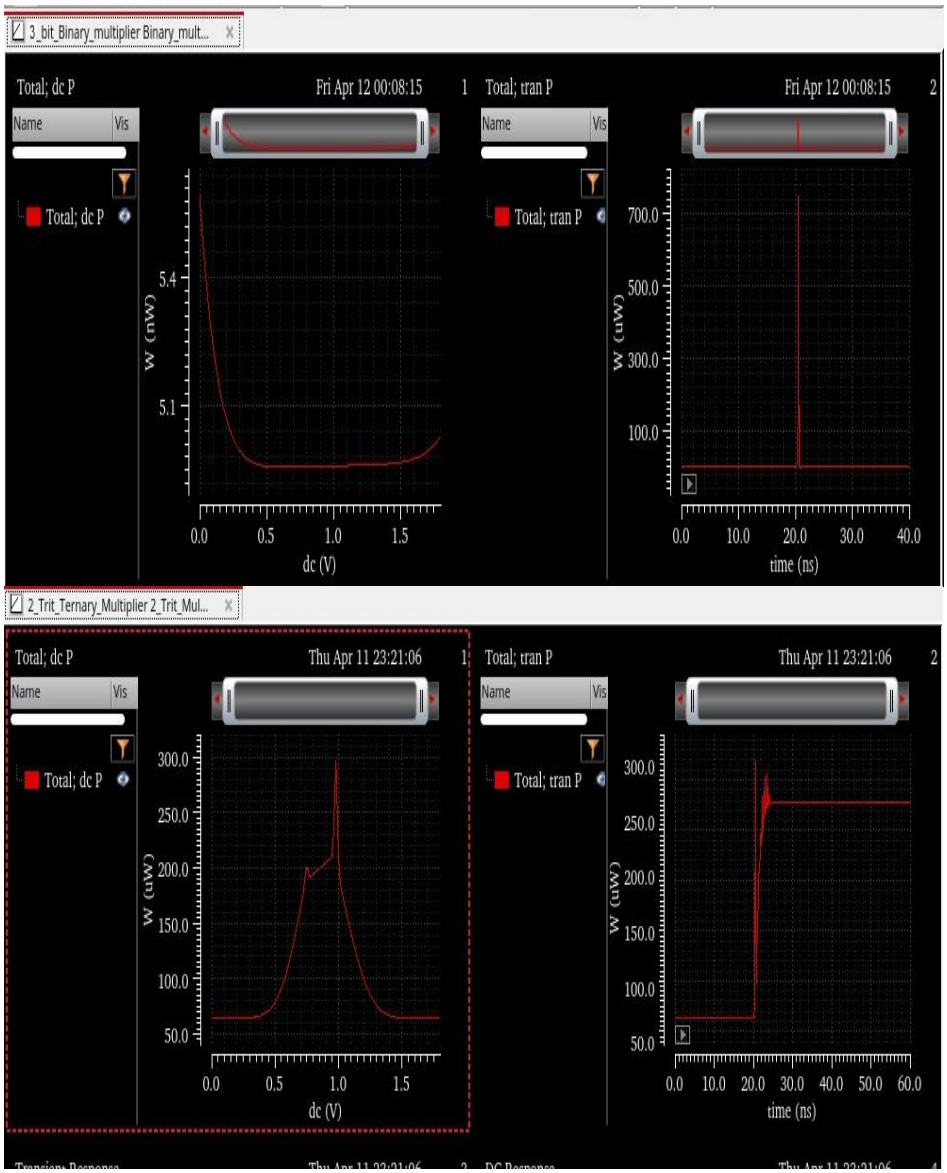


Fig. 24 DC and transient response: 3 bit binary multiplier and 2 trit multiplier

Table 7. Comparative analysis of DC and transient power

Sl. No.	Circuit	DC Power (Micro Watt)	Transient Power (Micro Watt)
1	Ternary Inverter	12.5	12.5
2	Forced Stack Ternary Inverter	6	6
3	2 Bit Binary Multiplier	144.55	185.44
4	3 Bit Binary Multiplier	0.005	700
5	1 Trit Ternary Multiplier	121.242	108.89
6	2 Trit Ternary Multiplier	300	270

Table 8. Comparative analysis of the number of ports

Sl. No.	Circuit	Number of Inputs	Number of Outputs	Total	Maximum Value of Input and Product
1	2 Bit Binary Multiplier	2+2=4	4	8	3X3=9
2	3 Bit Binary Multiplier	3+3=6	6	12	7X7=49
3	1 Trit Ternary Multiplier	1+1=2	2	4	2X2=4
4	2 Trit Ternary Multiplier	2+2=4	4	8	8X8=64

5. Conclusion

From the above schematics, functional verification of all the ternary logic circuits (as described in the article) is carried out. DC power and Transient power for these circuits are measured to construct Power analysis and Port analysis tables. As in Table 7, it is clear that a 1-trit multiplier consumes less DC power than a 2-bit binary multiplier, and a 2-trit multiplier consumes less transient power than a 3-bit binary multiplier. The total power in a 2-trit multiplier is 81.5% that of a 3-bit binary multiplier. From the Table 8, the number of total ports required to find the product in ternary circuits is 66.6% of ports required in binary.

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