Original Article

A Physical LDMOST Model and Predictive Simulations for Advanced Technology CAD

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Abstract - *This article describes a compact Lateral DMOS Transistor (LDMOST) model incorporated directly into SPICE source code and presents its application to power IC technology CAD. The complete model combines a previously developed semi-numerical static model and a built-in parasitic component model with a charge-based dynamic model. This composite model is based on device physics; thus, it accounts well for important power MOSFET characteristics such as non-uniformly doped channels, reverse-recovery transients and the non-planar drift region. The measurements from the power MOSFET samples support the predictive model, verified in extensive SPICE simulations of several high-voltage circuits. This LDMOST model might be useful in computer-aided optimal design of smart power ICs.*

Keywords - *Charge-based dynamic model, High-voltage MOSFET, Lateral DMOS transistor, Parasitic BJT model, Power IC technology CAD.*

1. Introduction

Today, power MOSFETs are extensively used in a variety of high-voltage ICs and power applications like switch-mode power supplies, automotive ICs, power amplifiers, and consumer and telecommunication applications [1]. The optimal design of such high-voltage/power ICs requires SPICE-compatible power MOSFET models, which can predict accurately the static and dynamic performance over a wide operating range.

Power MOSFETs are commonly modeled with sub-circuits composed of conventional low-voltage SPICE elements [2-7]. But, the sub-circuit models are inadequate and often suffer from convergence issues. They cannot account properly for the unique device characteristics of high-voltage MOSFETs over a wide range of biases and operating frequencies. While several analytical or physical models for the power MOSFETs have been described in the literature [8-13], an accurate and practical approach for modelling power devices remains elusive yet.

This work develops a compact physical model for Lateral DMOS Transistors (LDMOSTs) and their application to power IC technology CAD. The cross-section of the LDMOST investigated in this study is shown in Figure 1. The p-body is diffused vertically and laterally from the source end, and thus, the device shapes a non-uniformly doped channel region. The poly-silicon gate extended over the thick field oxide forms an accumulation layer in the non-planar drift region. Thus, if V_{GS} exceeds the channel threshold Voltage (V_T), electrons can transit from source to drain through the inverted channel. Figure 2 depicts a network representation of the complete LDMOST model. Every DC current and each regional charge in the network are expressed as a function of node voltage differences (V_{DS}, V_{GS}, V_{EB}, V_{CB}). The time derivative of each regional charge represents the capacitive transient current. This charge dynamics assures carrier conservation in the simulations. When all network elements in Figure 2 are implemented in SPICE, the complete model will provide the element currents and the partial derivatives of charges and currents needed for the Newton-Raphson iteration in the SPICE program.

The drain-source DC current model for the LDMOST shown in Figure 1 has been addressed in the previous publication [14]. The static model, which is notated with a current source I_{DS} in Figure 2, is the base of parasitic and dynamic models described in this article; therefore, the symbols and equations in [14] are used in this paper without restatement. The rest of this article is organized as follows. In succession to the I_{DS} model in [14], Section 2 describes an analytical model for parasitic Bipolar Junction Transistor (BJT) action inherent to this LDMOST structure. Section 3 details the transient behaviours of the device, which are expressed by quasi-static models of the regional charges. Section 4 demonstrates the effectiveness of the complete model through representative power circuit simulations. Finally, the conclusion is provided in Section 5.
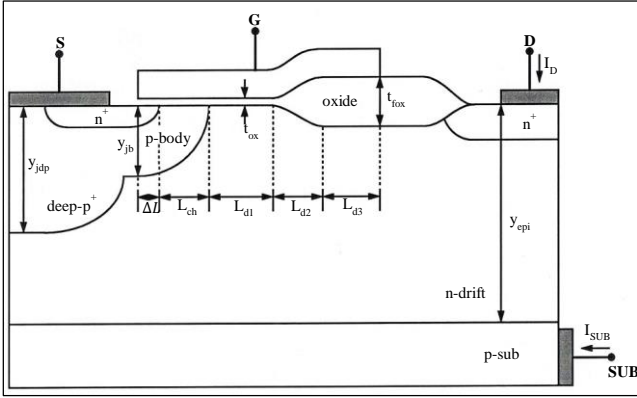
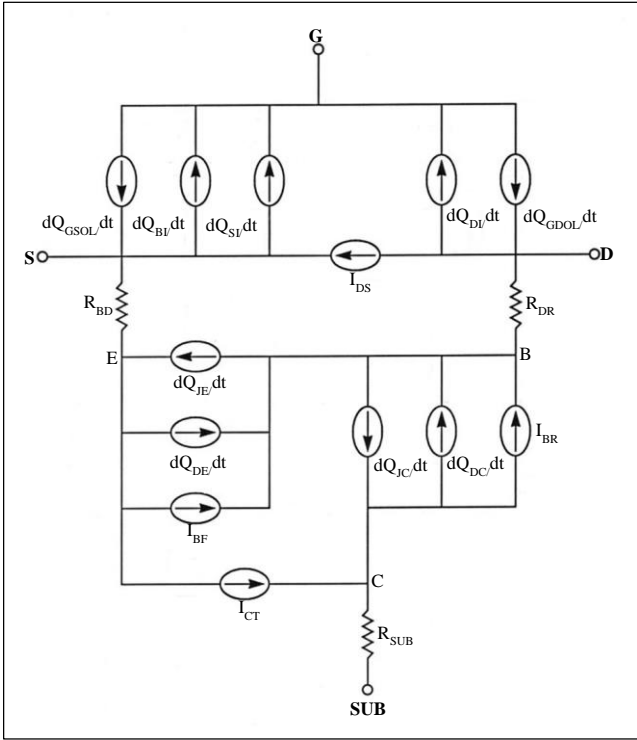**Fig. 1 LDMOST structure, geometrical parameters are defined**

Fig. 2 A network representing the LDMOST model

2. Parasitic BJT Model

In the investigated power MOSFET, there are two p-n junctions (Body-Drift And Substrate-Drift) that form a parasitic p-n-p (Body-Drift-Substrate) BJT. Under normal applications, these built-in junctions are reverse-biased and thus do not influence the circuit operation. However, depending on bias conditions, these two junctions act like a parasitic transistor. For example, V_{DS} could happen to be negative for a moment during transient switching of the LDMOST in a power IC. If the substrate is tied to the lowest voltage in the high-voltage IC, this negative bias turns on the body-drift junction; thus, the parasitic BJT enters the active mode. If the source and substrate are tied together, the negative value of V_{DS} activates both junctions; thus, the parasitic BJT operates momentarily in saturation. In either

case, the terminals labelled SUB (substrate), D (drain) and S (source) behave like the collector, base and emitter of the junction transistor. Thereby, the resulting parasitic current might overwhelm the entire device. Here, this parasitic component is modelled with I_{CT} (base transport current), I_{BF} (forward base current), I_{BR} (reverse base current) and 3 ohmic resistances: R_{BD} (p$^+$-body), R_{DR} (n-drift) and R_{SUB} (p-substrate).
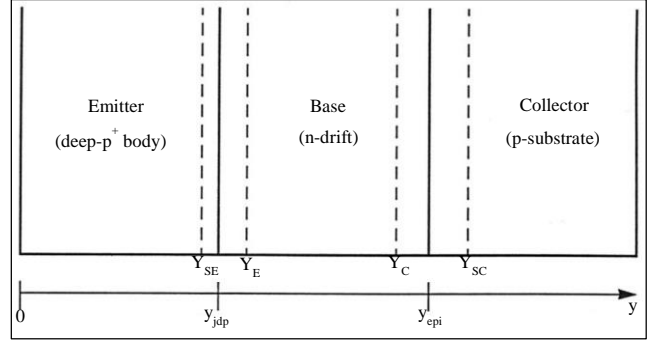

Fig. 3 One-dimensional representation of the parasitic pnp bipolar junction transistor

Figure 3 represents a one-dimensional p$^+$-n-p structure for the parasitic BJT, in which $y_{SC}, y_C,$ y_{SE} and y_E denote the boundaries of the Space Charge Region (SCR) at the Collector-Base (C-B) and Emitter-Base (E-B) Junction. With two basic assumptions: 1) wide collector/base/emitter region and 2) high-level carrier injection [15], solving the Ambipolar Transport Equation (ATE) yields the minority mobile hole concentration in the base:

$$p(y) = p_{BF}(y) + p_{BR}(y) \tag{1}$$

$$p_{BF}(y) = \frac{p(y_E)}{\sinh(W_{BN})} \sinh(\frac{y_C - y}{L_{AB}}) \tag{2}$$

$$p_{BR}(y) = \frac{p(y_C)}{\sinh(W_{BN})} \sinh(\frac{y - y_E}{L_{AB}}) \tag{3}$$

Where L_{AB} represents the length of ambipolar diffusion at the base and $W_{BN}(\equiv (y_C - y_E)/L_{AB})$ denotes the normalized base width. The excess hole concentrations at the boundaries are,

$$p(y_E) \cong n_i \left[\exp\left(\frac{qV_{EB}}{2kT}\right) - 1\right] \tag{4}$$

$$p(y_C) \cong n_i \left[exp\left(\frac{qV_{CB}}{2kT}\right) - 1\right] \tag{5}$$

where n_i represents the intrinsic concentration of electrons, q denotes the magnitude of electronic charge, and kT/q defines the thermal voltage. In addition, the boundaries y_E and y_C in the base are characterized as

$$y_E = y_{jdp} + \left[\frac{2\varepsilon_S}{qN_{DD}}(\psi_{bd} - V_{EB})\right]^{1/2} (\text{for } V_{EB} < \psi_{bd})$$

$$= y_{jdp} \qquad \text{(for } V_{EB} \geq \psi_{bd}) \qquad (6)$$

$$y_C = y_{epi} - \left[\frac{2\varepsilon_S N_{AS}}{q N_{DD}(N_{AS}+N_{DD})} (\psi_{sub} - V_{CB}) \right]^{1/2}$$
$$\text{(for } V_{CB} < \psi_{sub})$$

$$= y_{epi} \quad \text{for } V_{CB} \geq \psi_{sub}) \qquad (7)$$

Where ε_S denotes the silicon permittivity, N_{DD} and N_{AS} denote the doping concentrations of base (n-drift) and collector (p-substrate), and ψ_{sub} $(= (kT/q)ln(N_{AS}N_{DD}/n_i^2))$ and ψ_{bd} denote the built-in potentials at the C-B and E-B junction.

The BJT base current can be simply characterized as the sum of the back injection component from the base and the recombination component across the base region. For the active mode of the parasitic transistor, the low-level injection is prevalent across the emitter (body) region. Accounting for majority carrier degeneracy and bandgap narrowing [16],

$$I_{BF} = \frac{qA_E}{\tau_{HB}} \int_{y_E}^{y_C} p_{BF}(y)dy + \frac{qA_E n_i^2 y_{jdp}}{N_{AB(eff)}\tau_{nE}} \left[\exp(\frac{qV_{EB}}{kT}) - 1 \right] (8)$$

Where A_E denotes the effective area of E-B junction, $N_{AB(eff)}$ and τ_{nE} denote the effective doping concentration and lifetime of the electron in the emitter and τ_{HB} denotes the lifetime of the highly injected hole at the base. Whereas, in the reverse mode of the parasitic BJT, the high-level injection is prevalent across the collector (substrate) region. Solving another ATE in the collector yields

$$I_{BR} = \frac{qA_C}{\tau_{HB}} \int_{y_E}^{y_C} p_{BR}(y)dy + \frac{qA_C n_i L_{AC}}{\tau_{HC}} \left[\exp(\frac{qV_{CB}}{2kT}) - 1 \right] \quad (9)$$

Where A_C is the effective area of the C-B junction, and L_{AC} and τ_{HC} are the length of ambipolar diffusion and lifetime of highly injected electrons in the collector, respectively.

Now, neglecting carrier recombination in junction SCRs, the model equations characterizing the base transport current can be written as

$$I_{CT} = I_{CF} - I_{CR} \qquad (10)$$

$$I_{CF} = A_{EC}J_{TF} - I_{BF} \qquad (11)$$

$$I_{CR} = A_{EC}J_{TR} - I_{BR} \qquad (12)$$

$$J_{TF} = \frac{1+b_B}{b_B} \left\{ \frac{qn_i^2 y_{jdp}}{N_{AB(eff)}\tau_{nE}} \left[\exp(\frac{qV_{EB}}{kT}) - 1 \right] - qD_A \frac{dp_{BF}}{dy}|_{y=y_E} \right\} \qquad (13)$$

$$J_{TR} = \frac{1+b_B}{b_B} \left\{ \frac{qn_i L_{AC}}{\tau_{HC}} \left[\exp(\frac{qV_{CB}}{2kT}) - 1 \right] - qD_A \frac{dp_{BR}}{dy}|_{y=y_c} \right\} \qquad (14)$$

Where A_{EC} denotes the effective area of BJT cross-section, D_A is the ambipolar diffusivity in the base, and b_B

defines a ratio of electron-mobility to hole-mobility. In Equations (11)-(14), J_{TF} and J_{TR} represent the active-mode emitter current density and reverse-mode collector current density, respectively.

3. Charge-Based Dynamic Model

The dynamic behaviors of the LDMOST are modeled with the time derivative of the regional charges within the device. In the network representing the device model, which is shown in Figure 2, Q_{DI} and Q_{SI} denote the mobile channel charges related to the drain and source node, and Q_{BI} denotes the depletion charge in the non-uniformly doped p-body. Q_{GDOL} and Q_{GSOL} represent the charges stored at the gate overlap capacitances due to the drift region and the lateral source diffusion, respectively.

Q_{JC} and Q_{JE} denote the depletion charges at the C-B and E-B junction of the parasitic BJT, and Q_{DC} and Q_{DE} denote the injection charges at the forward-biased C-B and E-B junction, respectively. These internal charges are expressed as a function of node voltage differences, and the dynamic properties of the device are represented by the transient current.

$$\frac{dQ_i}{dt} = \sum_j \frac{\delta Q_i}{\delta V_j} \frac{dV_j}{dt} \qquad (15)$$

Where Q_i is a regional charge, and V_j is a node voltage difference.

3.1. Expressions for Q_{SI}, Q_{DI} and Q_{BI}

In the non-uniformly doped channel, the p-body doping concentration is simply approximated as a one-dimensional exponential function: $N_{AB}(x) = N_{A0}\exp(-\eta_{ch}x/L_{ch})$, where $\eta_{ch}(= ln(N_{A0}/N_{DD}))$ defines the doping gradient, and N_{A0} denotes the maximum concentration at the source. In the linear region, the relationship between the channel potential V and the mobile channel charge Q_n [14, Equation (2)] yields

$$\int_0^x dQ_n = (C_{ox} + C_D) \int_0^{V(x)} dV \qquad (16)$$

Where C_D is an average of the p-body depletion capacitance, C_{ox} $(= \varepsilon_{ox}/t_{ox})$ represents the thin oxide capacitance and ε_{ox} denotes the oxide permittivity. Then, substituting $V(x) \cong (V_{ch}/L_{ch})x$ into Equation (16), in which V_{ch} is the voltage drop in the channel,

$$Q_n(x) = - \left[C_{ox}(V_{GS} - V_T) + \frac{2C_{D0}\eta_{ch}|\phi_B(0)|}{L_{ch}}x - (C_{ox} + C_{D0})\frac{V_{ch}}{L_{ch}}x \right] \qquad (17)$$

Where,

$$C_{D0} = k_{f3}[q\varepsilon_s N_{A0}/(4|\phi_B(0)|)]^{1/2} \qquad (18)$$

$$|\phi_B(0)| = (kT/q) ln[N_{A0}/n_i] \qquad (19)$$

V_T denotes the channel threshold voltage, and k_{f3} denotes an empirical parameter for depletion capacitance. Following the charge partitioning scheme used in [17],

$$Q_{SI} = W_z \int_0^{L_{ch}} (1 - \frac{x}{L_{ch}}) Q_n(x) dx$$

$$= -\frac{1}{6} W_z L_{ch} [3C_{ox}(V_{GS} - V_T) + 2C_{D0}\eta_{ch}|\phi_B(0)| - (C_{ox} + C_{D0})V_{ch}] \tag{20}$$

$$Q_{DI} = W_z \int_0^{L_{ch}} \frac{x}{L_{ch}} Q_n(x) dx$$

$$= -\frac{1}{6} W_z L_{ch} [3C_{ox}(V_{GS} - V_T) + 4C_{D0}\eta_{ch}|\phi_B(0)| - 2(C_{ox} + C_{D0})V_{ch}] \tag{21}$$

Where W_z is the width of the device. Meanwhile, the body depletion charge can be expressed as,

$$Q_{BI} = -W_z \int_0^{L_{ch}} \left[2q\varepsilon_S N_{AB}(x) \left(2|\phi_B(x)| + \frac{V_{ch}}{L_{ch}}x \right) \right]^{1/2} dx \tag{22}$$

Assuming that $N_{AB}(x)$ and the body Fermi potential $|\phi_B(x)|$ are approximated as $\overline{N_{AB}}$ and $|\overline{\phi_B}|$, respectively,

$$\log(\overline{N_{AB}}) = (\log N_{A0} + \log N_{DD})/2 , \tag{23}$$

$$|\overline{\phi_B}| = [|\phi_B(0)| + |\phi_B(L_{ch})|]/2 , \tag{24}$$

The p-body depletion charge in the linear region is written as,

$$Q_{BI} = -W_z L_{ch} K_{BI} \frac{(V_{ch} + 2|\overline{\phi_B}|)^{3/2} - (2|\overline{\phi_B}|)^{3/2}}{V_{ch}} \tag{25}$$

Where,

$$K_{BI} = \frac{2}{3}\sqrt{2q\varepsilon_S \overline{N_{AB}}} \tag{26}$$

In the region of the channel current saturation, the mobile and depletion charges related to the channel are obtained from Equations (20), (21) and (25) by replacing V_{ch} with the onset voltage for the saturation, Equation (10) [14]:

$$V_{ch(sat)} = \frac{C_{ox}(V_{GS} - V_T) + C_{D0}\eta_{ch}|\phi_B(0)|}{C_{ox} + C_{D0}} \tag{27}$$

In the cutoff region, $Q_{SI} \cong Q_{DI} \cong 0$. If $V_{FBch} < V_{GS} \leq V_T$, where V_{FBch} represents the flatband voltage in the channel, the depletion charge in the p-body can be written as,

$$Q_{BI} = -\frac{3}{2} W_z L_{ch} K_{BI} \sqrt{2|\overline{\phi_B}|} \sqrt{\frac{V_{GS} - V_{FBch}}{V_T - V_{FBch}}} \tag{28}$$

If $V_{GS} \leq V_{FBch}$, the channel is accumulated, thus $Q_{BI} = W_z C_{ox} L_{ch}(V_{FBch} - V_{GS})$.

3.2. Expressions for Q_{GSOL} and Q_{GDOL}

The overlap capacitance between a heavily doped lateral source diffusion and the gate has a fixed value; thus, the gate overlap charge stored at the parasitic capacitance is simply expressed as $Q_{GSOL} = (W_z \Delta L \varepsilon_{ox} V_{GS})/t_{ox}$ where ΔL is defined in Figure 1, meanwhile, the overlap capacitance between a slightly doped non-planar drift region and the gate varies with the applied bias owing to the depletion of mobile carriers.

When $V_{DS} < V_{GS} - V_{FBdr}$ in which V_{FBdr} is an effective flatband voltage at drift region, the gate-to-drain overlap charge is approximated as

$$Q_{GDOL} = -W_z[C_{ox}L_{d1} + \frac{(C_{ox} + C_{fox})L_{d2}}{2} + C_{fox}L_{d3}](V_{DS} - V_{GS} + V_{FBdr}) \tag{29}$$

Where C_{fox} ($= \varepsilon_{ox}/t_{fox}$) represents the thick oxide capacitance. When $V_{DS} \geq V_{GS} - V_{FBdr}$, by using Equations (14)-(16) in [14], the gate-to-drain overlap charge is expressed as,

$$Q_{GDOL} = -q f_{QD} W_z N_{DD} y_{ox}[L_{d1} + \frac{L_{d2}}{t_{fox} - t_{ox}} y_{ox}]$$

(For $V_{DS} \geq V_{GS} - V_{FBdr}$ and $y_{ox} \leq (t_{fox} - t_{ox})/2$)

$$= -q f_{QD} W_z N_{DD}[(L_{d1} + L_{d2}/2)y_{ox} + (L_{d2}/2 + L_{d3})y_{fox}]$$

(For $V_{DS} \geq V_{GS} - V_{FBdr}$ and $y_{ox} > (t_{fox} - t_{ox})/2$) (30)

Where f_{QD} ($0 < f_{QD} \leq 1$) represents a depletion charge partitioning parameter, and y_{fox} and y_{ox} denote the depletion boundary underneath thick and thin oxide, which are defined in Equations (20) and (21) [14].

3.3. Expressions for Q_{JE}, Q_{JC}, Q_{DE} and Q_{DC}

Lastly, the charges associated with the parasitic junction transistor are expressed as follows:

$$Q_{JE} = A_E \sqrt{2q\varepsilon_S \psi_{bd} N_{DD}(1 - \frac{V_{EB}}{\psi_{bd}})} \text{ (for } V_{EB} < \psi_{bd})$$
$$= 0 \qquad \text{(for } V_{EB} \geq \psi_{bd}) \tag{31}$$

$$Q_{JC} = A_C \sqrt{2q\varepsilon_S \psi_{sub} \frac{N_{DD}N_{AS}}{N_{DD} + N_{AS}}(1 - \frac{V_{CB}}{\psi_{sub}})} \text{(for } V_{CB} < \psi_{sub})$$
$$= 0 \qquad \text{(for } V_{CB} \geq \psi_{sub}) \tag{32}$$

$$Q_{DE} = qA_E \int_{y_E}^{yc} p_{BF}(y)dy + \frac{qA_E n_i^2 y_{jdp}}{N_{AB(eff)}} \left[\exp\left(\frac{qV_{EB}}{kT}\right) - 1 \right] \quad (33)$$

$$Q_{DC} = qA_C \int_{y_E}^{yc} p_{BR}(y)dy + qA_C n_i L_{AC} \left[\exp\left(\frac{qV_{CB}}{2kT}\right) - 1 \right] \quad (34)$$

If the parasitic BJT turns on, the excess mobile charges Q_{DE} and Q_{DC} significantly affect the transient characteristics of the device.

3.4. Model Verification: C_{oss} and C_{rss}

With the test samples fabricated for high-voltage ICs, the dynamic model of the LDMOST has been validated in comparison with experiments.

Figure 4 compares two fundamental device capacitances: output capacitance C_{oss} $(\equiv \partial Q_{DT} / \partial V_{DS})$ and reverse transfer capacitance C_{rss} $(\equiv -\partial Q_{GT} / \partial V_{DG})$, in which Q_{DT} $(= Q_{DI} - Q_{GDOL} + Q_{JE} - Q_{DE} + Q_{JC} - Q_{DC})$ denotes the total drain charge, Q_{GT} $(= Q_{GSOL} - Q_{BI} - Q_{SI} - Q_{DI} + Q_{GDOL})$ denotes the total gate charge, and V_{DG} defines the drain-to-gate voltage.

As V_{DS} increases, the magnitude of C_{oss} decreases rapidly. It can be seen that its correspondence is satisfactory over a wide range of drain-to-source bias voltages. The discrepancy in C_{oss} is 3.6 % and 2.7 % at $V_{DS} = 5$ V and 45 V, respectively. Meanwhile, the magnitude of C_{rss} decreases monotonously with the drain-to-source voltage. A good agreement between model and measurement is observed over an entire range of V_{DS}.
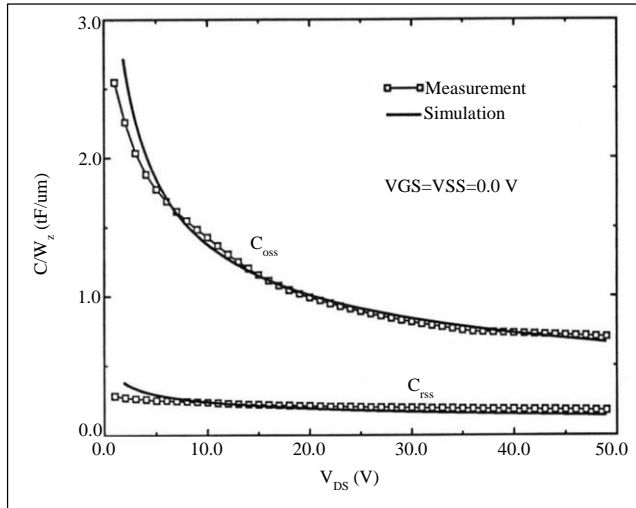

Fig. 4 Simulated and measured device capacitances, V_{SS} defines the substrate-to-source voltage

4. SPICE Simulations and Discussion

To demonstrate the developed LDMOST model, all network elements in Figure 2 have been incorporated directly into the SPICE2G.6 program [18] by appending three new subroutines (LDMOSFET, LDTMOS and LDTBJT) and altering in part the FORTRAN code of eighteen SPICE subroutines in the software. Basically, the subroutine LDMOSFET shown in Figure 5 links the composite model to the node-voltage analysis in the SPICE program.

The internal resistances R_{DR}, R_{BD} and R_{SUB} are treated as conductance elements, and the model calculations are performed mostly in the subroutines LDTBJT and LDTMOS. The derivatives of charges and currents necessary for the Newton-Raphson iteration are calculated via multiple calls of LDTBJT and LDTMOS with perturbations of node voltage differences. The subroutine LDTMOS calculates the drain-source current (I_{DS}), the intrinsic channel charges (Q_{DI}, Q_{SI}, Q_{BI}) and the gate-to-drain overlap charge (Q_{GDOL}), and returns their computed values to the subroutine LDMOSFET.

Whereas the subroutine LDTBJT calculates the parasitic BJT currents (I_{CT}, I_{BR}, I_{BP}) and injection charges (Q_{DC}, Q_{DE}) and returns their computed values to the subroutine LDMOSFET. The other elements (Q_{JC}, Q_{JE}, Q_{GSOL}) are quantified directly in the subroutine LDMOSFET. Accordingly, the three new subroutines in the circuit simulation program calculate the device model equations and link them to the SPICE nodal analysis.

Figure 6 depicts an inductive-resistive load switching circuit using the lateral DMOS transistor, and Figure 7 shows the SPICE-simulated transients for the switching circuit in Figure 6. Note that the element name of the LDMOST device begins with the letter 'Y' in the new version of the SPICE program. The amplitude of the input pulse is 14 V with a rising/falling time of 50 ns. At $V_{DD} = 50$ V, the load resistance with a value of 20 Ω results in a switching current of about 2.5 A. All switching transients are well consistent with the theoretical predictions.

Figure 8 shows the SPICE-simulated gate-drive transients for the switching circuit in Figure 6 with three different values of gate resistance. The gate resistance represented by R_G ranges from 0.2 to 1.0 kΩ. The amplitude of the gate pulse is 14 V with a 50 ns rising/falling time. The simulations properly predict the plateau waveforms occurring at the falling and rising edges of the input signal, which are caused by the reverse transfer capacitance in the double-diffused MOS transistor.

Another simulation result in Figure 9 shows the turn-off transients for the switching circuit in Figure 6 with a small gate resistance of 50 Ω. The load inductance represented by L_L ranges from 50 to 180 nH. The amplitude of the gate input is the same at 14 V, and the rising/falling time of the input voltage is also 50 ns. The simulations in Figure 9 adequately describe the overshoots of voltage and current for a given load inductance [19].
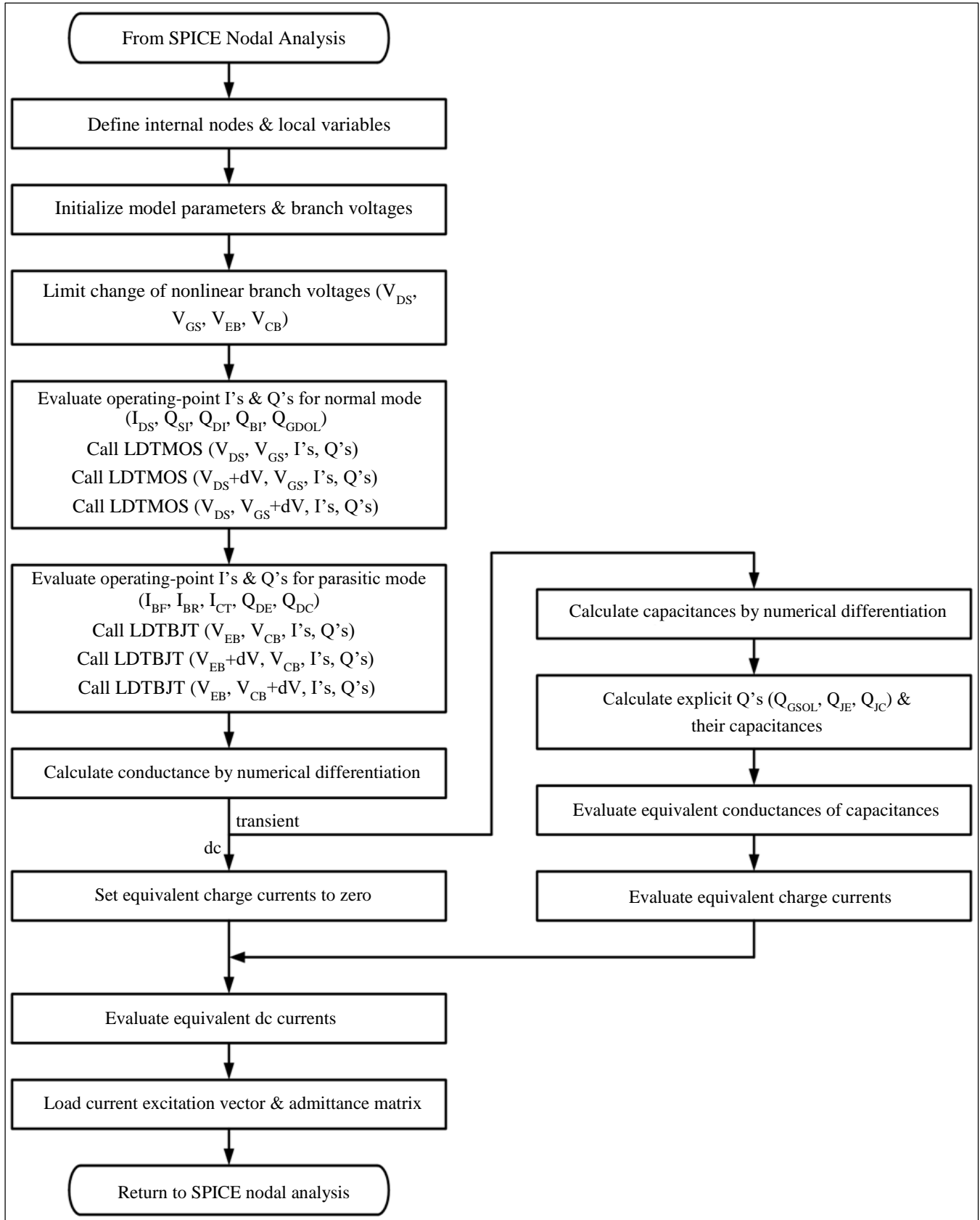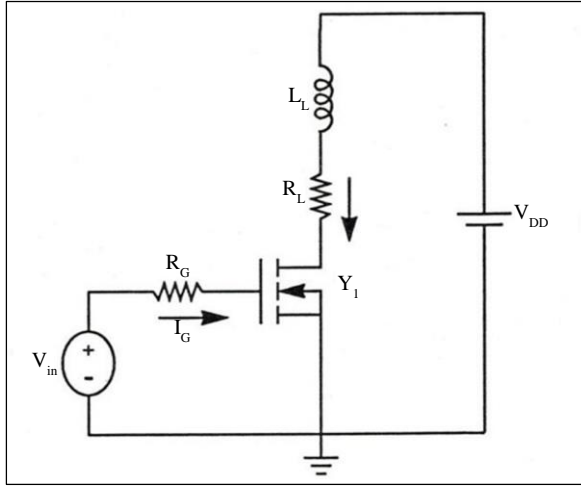
From SPICE Nodal Analysis

↓

Define internal nodes & local variables

↓

Initialize model parameters & branch voltages

↓

Limit change of nonlinear branch voltages (V_{DS}, V_{GS}, V_{EB}, V_{CB})

↓

Evaluate operating-point I's & Q's for normal mode (I_{DS}, Q_{SI}, Q_{DI}, Q_{BI}, Q_{GDOL})
Call LDTMOS (V_{DS}, V_{GS}, I's, Q's)
Call LDTMOS ($V_{DS}+dV$, V_{GS}, I's, Q's)
Call LDTMOS (V_{DS}, $V_{GS}+dV$, I's, Q's)

↓

Evaluate operating-point I's & Q's for parasitic mode (I_{BF}, I_{BR}, I_{CT}, Q_{DE}, Q_{DC})
Call LDTBJT (V_{EB}, V_{CB}, I's, Q's)
Call LDTBJT ($V_{EB}+dV$, V_{CB}, I's, Q's)
Call LDTBJT (V_{EB}, $V_{CB}+dV$, I's, Q's)

↓

Calculate conductance by numerical differentiation

↓ transient / dc

Calculate capacitances by numerical differentiation

↓

Calculate explicit Q's (Q_{GSOL}, Q_{JE}, Q_{JC}) & their capacitances

↓

Evaluate equivalent conductances of capacitances

↓

Evaluate equivalent charge currents

Set equivalent charge currents to zero

↓

Evaluate equivalent dc currents

↓

Load current excitation vector & admittance matrix

↓

Return to SPICE nodal analysis
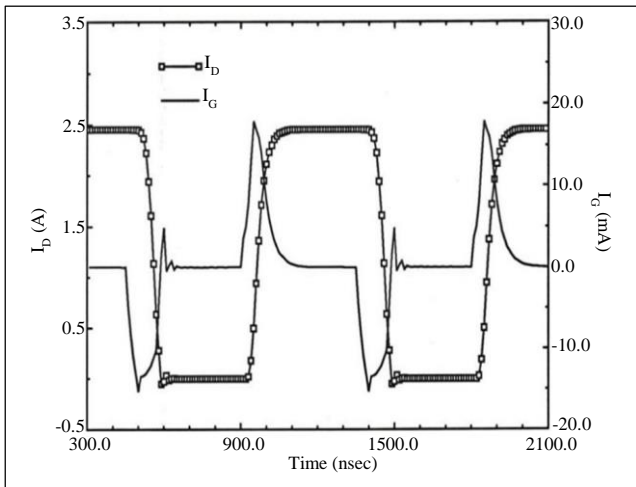
Fig. 5 Flowchart of the subroutine LDMOSFET

Fig. 6 Inductive-resistive load LDMOST switching circuit, Wz of Y₁ measures 5×10⁴ μm
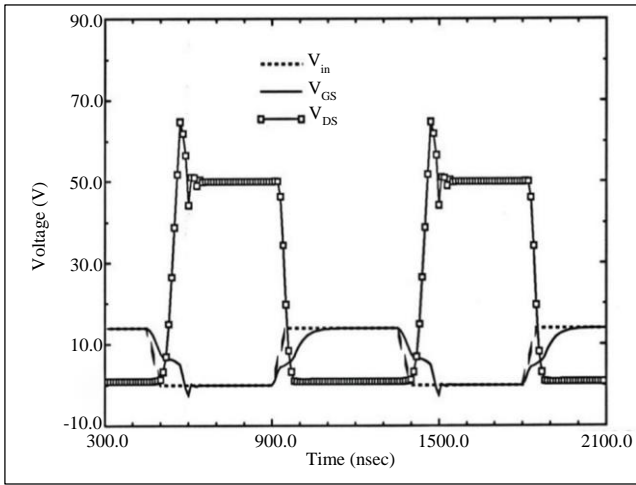
(a)

(b)

Fig. 7 SPICE-simulated transients for the switching circuit in Figure 6 (R_G = 0.5 kΩ, R_L= 20 Ω, L_L = 0.5 μH, V_{DD} = 50 V): (a) Voltage waveforms, and (b) Current waveforms.
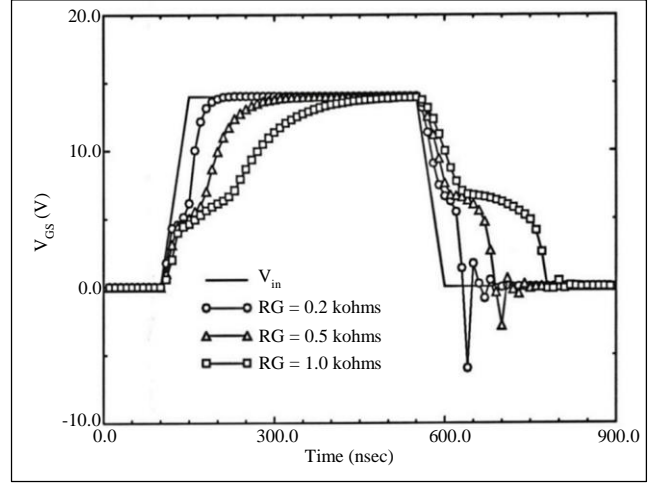
(a)
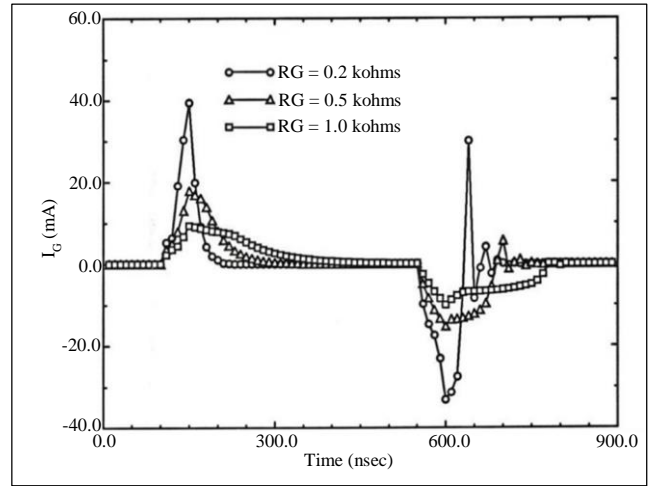
(b)

Fig. 8 SPICE-simulated gate-drive transients for the switching circuit in Figure 6 (R_L= 20 Ω, L_L = 0.5 μH, V_{DD} = 50 V): (a) Gate voltage waveforms, and (b) Gate current waveforms.
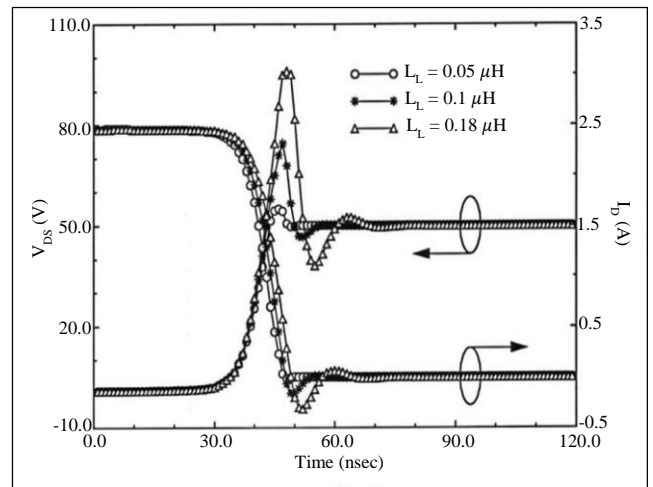
Fig. 9 SPICE-simulated inductive switching-off transients for the switching circuit in Figure 6 (R_G = 50 Ω, R_L = 20 Ω, V_{DD} = 50 V)
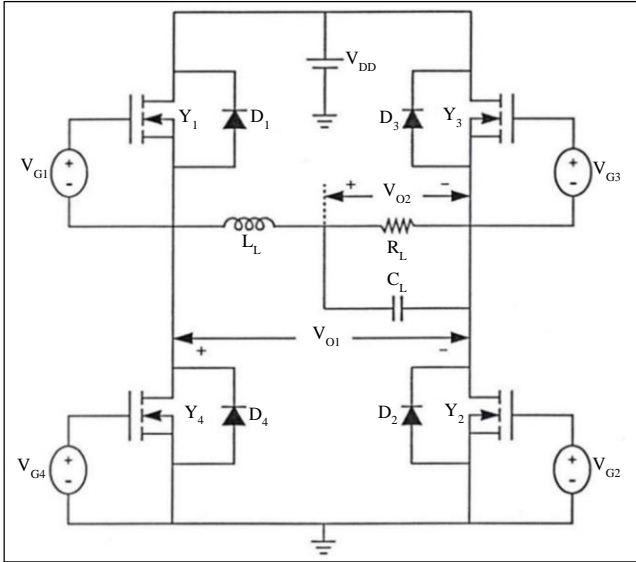
Fig. 10 Full-bridge DC-to-AC converter, V_{DD} = 60 V, R_L = 20 Ω, C_L= 1 nF, L_L = 0.2 μH, and the widths of Y_1, Y_2, Y_3 and Y_4 are all 5×10⁴ μm
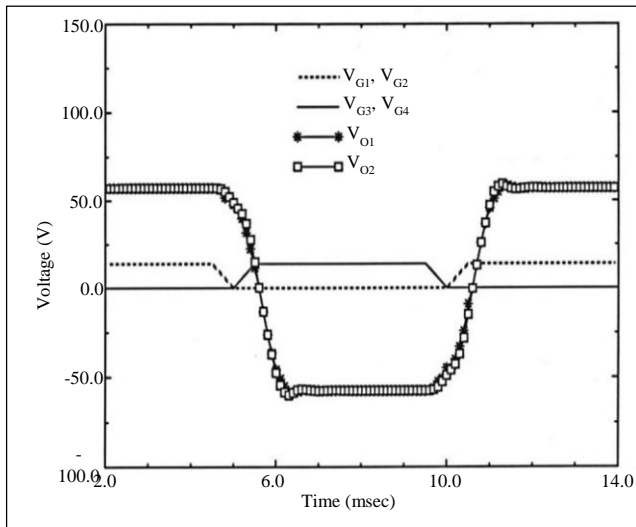

Fig. 11 SPICE-simulated output waveforms for the single-phase DC-to-AC converter in Figure 10

Figure 10 depicts the more complex power circuit, a full-bridge DC-to-AC converter, and Figure 11 shows the SPICE-simulated output waveforms for the conversion in Figure 10. The DC input supply represented by V_{DD} is 60 V, and the amplitude of the alternate gate pulse signals is 14 V with a rising/falling time of 0.5 ms. In the circuit schematic, D_1, D_2, D_3 and D_4 represent the inherent p-n (body-drift and substrate-drift) junction diodes of the LDMOST, which are utilized frequently to clamp the inductive load switch-off current. Note that the transient simulation in Figure 11 reveals the utility of the parasitic components in the LDMOST circuits.

The simulation in Figure 12 shows the reverse-recovery transient for the investigated lateral DMOS transistor. When $t < 0.5\,\mu s$ ($V_{DS} < 0$), in which the parasitic BJT is operating

in saturation, the device stores the injection hole charges in the n-drift region. At $t = 0.5\,\mu s$, a pulse voltage (−5 to +10 V with a 0.6-μs rising time) is supplied to the drain terminal via a 20 Ω resistor to switch the LDMOST to the typical off state. Then, the excess charges in the non-planar drift region begin to diminish by recombination. The SPICE-simulated reverse-recovery current in Figure 12 corresponds well with the theoretical prediction. This feature of the developed model, which cannot be afforded by the behavioral macro models, might be quite useful in the optimal design of smart power ICs.
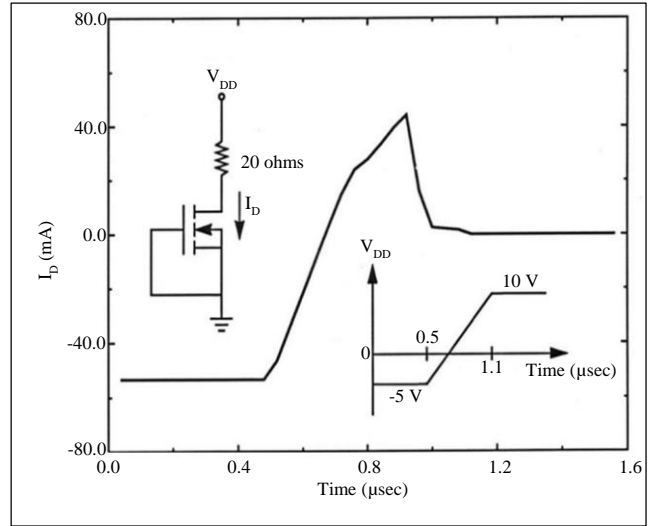

Fig. 12 SPICE-simulated reverse-recovery current of the investigated lateral DMOS transistor. The device width of the LDMOST measures 5×10⁴ μm. V_{DD} changes −5 to +10 V with a 0.6-μs rising time.

5. Conclusion

In this work, a comprehensive lateral DMOS transistor model, including the inherent BJT model and previous static model, was developed and incorporated directly into the SPICE program. The model has been formulated from quasi-static one-dimensional carrier transport equations, which characterize the regional charges and currents within the device. The capacitive charging/discharging currents are calculated from the regional charges.

The model developed herein accounts for the unique features of power MOSFETs like non-uniformly doped channels, reverse-recovery transients and non-planar drift regions. Moreover, the inter-electrode device capacitances obtained from the charge-based dynamic model exhibit a good agreement with those obtained from the device measurements. A range of SPICE simulations for inductive-load switching circuits, practical DC-to-AC converter and parasitic BJT action indicate that this predictive LDMOST model would be quite effective in TCAD of high-voltage power ICs.

Nomenclature

V_{DD} Power supply voltage.
V_{DS} Drain-to-source voltage.
V_{SS} Substrate-to-source voltage.
V_{GS} Gate-to-source voltage.
V_{ch} Voltage drop in channel.
V_{EB} Emitter-to-base voltage.
V_{CB} Collector-to-base voltage.
I_{D} Drain current.
I_{G} Gate current.
I_{SUB} Substrate current.
I_{DS} Drain-source current.

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