SSRG International Journal of Electrical and Electronics Engineering
ISSN: 2348-8379/ https://doi.org/10.14445/23488379/IJEEE-V12I2P109

Volume 12 Issue 2, 74-81, February 2025
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Original Article

High Performance Poly-Si Vertical Trench Power MOSFET Using Double Charge Balance Technique: Design and Simulation

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Received: 08 December 2024 Revised: 07 January 2025 Accepted: 05 February 2025 Published: 22 February 2025

Abstract - *In this work, a new vertical power MOSFET (SJSGTPMOS) structure, using a double charge balanced technique, is proposed and designed for the first time. The double charge balance technique is achieved by splitting the Trench Poly-Si gate and converting the n-drift region into a stack of charge-balanced p/n pillars, which significantly improves the device performance and reduces the total requirement of gate charge as well as Gate-To-Drain Terminal Capacitive (Cgd) coupling. Using 2D-Silvaco ATLAS, the high-performance electrical characteristics output is achieved in our proposed device, compared with the conventional trench MOSFET. The proposed device gives excellent results of 0.94 pC Gate Charge (Qgd), 33.6% improvement in breakdown voltage, 74.1% and 99.29% improvements in two Baliga's Figure of Merits (FOM1 and FOM2), 91.62% in Cgd, at epilayer thickness of 1.2µm, showing the enhancement features of the proposed structure over the existing state-of-the-art, using two perfectly different charge balanced technique, without any impact on the gate control.*

Keywords - *Split gate, Super junction, Charge balance, Trench, Breakdown voltage, Power MOSFET.*

1. Introduction

Power semiconductor devices discover themselves in all innovative system domains, be it mobile phones, with power consumption ranging from a few watts to high-end computers, RF measurements, cars, trains, satellites, etc., which consists of power consumption in watts to Kilo Watt (KW) or Megawatt (MW). Power MOSFET has become a device of prime importance and interest among device researchers. The factors involved in designing the power MOSFET depend on many factors. As a switching device, minimum values of conduction and switching losses are always the prime motive of power device researchers [1, 2].

For optimized output of the power MOSFET, the ON-Resistance (Ron), Breakdown Voltage (BV), and gate-drain charge are the foremost parameters to be analyzed, and their tradeoffs are significant. From a configuration point of view, power MOSFET with vertical trench gate configuration has many advantages over lateral power MOSFET since vertical configuration avoids the accumulation region, thereby reducing the resistance associated with it. Compared with conventional power MOSFETs, which have low voltage handling ability and a large gap between drain and gate, affecting switching performance. Many methods have been explored to address the above issues, like using thicker gate oxide, W-gated trench structure, and step gate oxide to reduce capacitive coupling, increase the ON-Resistance (Ron), Breakdown Voltage (BV), and gate-drain charge, as reported in the literature [3, 4].

Over a few decades, the use of Split poly-gate technology has shown many advantages over conventional trench gate structures. Shielded (Split) gate trench MOSFET is a charge-balanced structure [5] that plays an essential role in achieving low gate charge and low specific ON-resistance by guarding the gate and drain coupling effect to give better FOMs. Additionally, the split gate produces a 2-D charge balance, which aids in a decreased surface electric field, commonly referred to as the RESURF effect [5], which permits a trade-off between Breakdown Voltage (BV) and ON-resistance.

The Split Gate generates an essential Metal Oxide Semiconductor (MOS) capacitor between the trench and the mesa, in addition to depleting the lateral drift area in the blocking state. However, the high electric field problem at the corner of the gate continues to disturb the Ron-BV tradeoffs.

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The Super junction concept in the drift area is another technique that makes use of the "charge balancing" principle. Many pieces of literature have successfully demonstrated the advantage of charge-balanced super junction technology in the device.

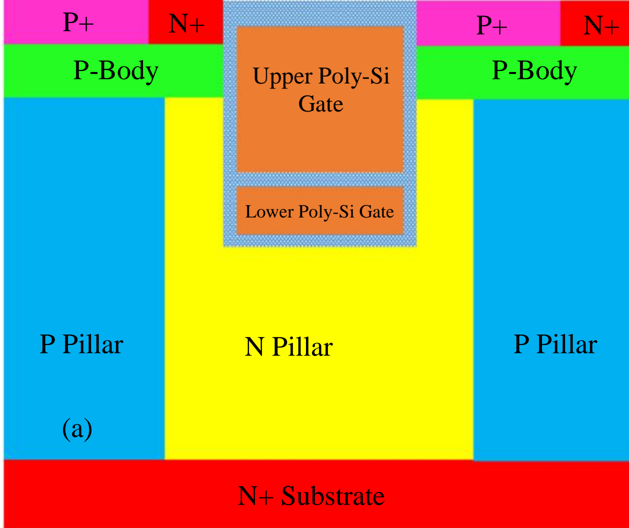

Fig. 1 (a) Cross-sectional view of proposed Super Junction Split Gate Trench Power MOSFET (SJSGTPMOS)

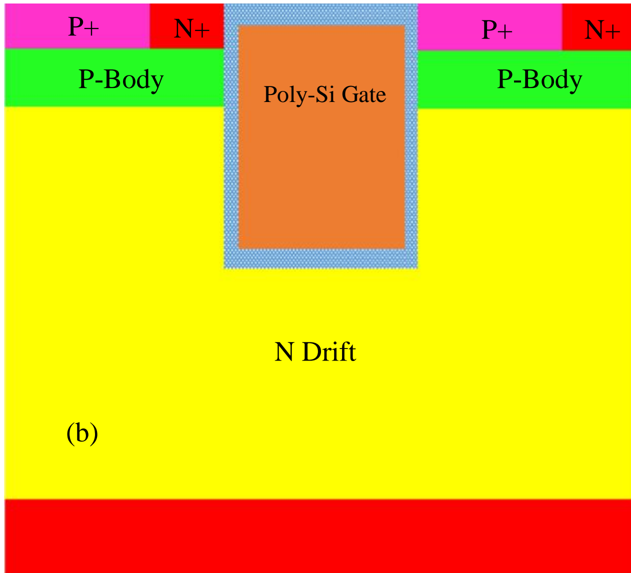

Fig. 1 (b) Cross-sectional view of Conventional Trench Power MOSFET (CTPMOS)

Drift region in improving the specific ON-resistance and device breakdown value. The benefits of a state-of-the-art super junction in the drift area by perfect charge balancing in the device's n/p pillar were demonstrated by Fujihira in his study [6], which introduced the super junction idea and analysis. It breaks the silicon limits and realizes a linear relation between Ron and BV [7]. The literature has described a wide variety of vertical trench gate topologies with super junction drift layers. These structures are capable of withstanding high reverse voltages, but because of their high base resistance, they are unable to significantly lower their particular ON-resistances at the same time as the breakdown voltage. Addressing the above challenges is the need of an hour.

In this work, we have designed and simulated a novel poly-silicon trench power MOSFET with gate and epilayer (drift) engineering to issue the challenges existing in reported power devices. The novelties of our work are presented pointwise. First, the performance of the proposed device under investigation is improved for the first time by employing double charge balance approaches. Furthermore, by dividing the trench gate into two sections, the proposed device's two distinct charge-balancing technologies are accomplished while mitigating the gate-drain coupling impact.

Additionally, the idea of a super junction is applied in the n-drift area by concurrently transforming it into stacks of charge-balanced p/n pillars. The electrical performance of our suggested device has been greatly enhanced by the two charge-balanced methods mentioned above. When compared to the traditional trench power MOSFET (CTPMOS), a thorough simulation examination of the suggested structure (SJSGTPMOS) and its performance reveals a notable improvement in the BV, Ron.sp, Qgd, FOM1 (BV^2/Ron), and FOM2 (Ron. Qgd).

This article has various sections that help fully understand our proposed device's performance. Section 2 describes the device structure and process flow. The simulation outcomes and arguments are shown in Section 3. This paper is completed in Section 4.

2. Proposed Device Structure and Process Flow

2.1. Device Structure's Schematics and its Formation

Figures 1(a) and (b) show the schematic of the proposed Super Junction Poly-Silicon Split Gate Trench Power MOSFET (SJSGTPMOS) and Conventional Trench MOSFET (CTPMOS) [8]. The device constraints used in the design and simulation of the suggested device are displayed in Table 1.

In our proposed work, the split gate is achieved by converting the Trench gate into two (unequal) halves, resulting in an upper gate and a lower gate (near the drain). We have connected the upper gate to the gate terminal next to the channel, whereas the lower gate connects the source terminal (grounded with 0V). The epilayer thickness and doping concentration of the epilayer (drift) region are 1.20µm and 5e16/cm^3, respectively. Since the super junction devices are vulnerable [9] to charge balance in the n/p pillar, the n/p drift pillar area is charged equally to ensure the highest level of charge balancing.

Table 1. Various dimension and doping values of the conventional (CTPMOS) and proposed (SJSGTPMOS) device

Parameters	Conventional Trench MOSFET	SuperJunction Split Gate Trench Power MOSFET
Cell pitch	3µm	3µm
Thickness of Epilayer	1.2µm	1.2µm
Trench width	1µm	1µm
Trench depth	1.2µm	1.2µm
Gate oxide thickness	50nm	50nm
n+ source width	0.334µm	0.334µm
Source Doping	1e19/cm^3	1e19/cm^3
Source depth	0.1µm	0.1µm
n-drift region doping	5e16/cm^3	P pillar=5e16/cm^3 N pillar=5e16/cm^3
n+ source doping	1e19/cm^3	1e19/cm^3
p-body region doping	2e17/cm^3	2e17/cm^3
P+ region doping	1e19/cm^3	1e19/cm^3
N+ Drain doping	1e19/cm^3	1e19/cm^3

Equation (1) links the doping concentration (N) to the width (W) of both n and p-pillars.

$$Wnp \,.\, Nnp = Wpp \,.\, Npp \quad (1)$$

In order to balance the charge in the p/n pillars of the drift area, Equation (1) is guaranteed [10]. A Silvaco ATLAS device simulator is used to do a two-dimensional (2D) simulation examination of the two devices. Among the many benefits of Silvaco ATLAS 2D device simulation software is the ability to model semiconductor devices. Using a straightforward, user-friendly, and adaptable syntax and runtime environment, along with first-rate 2D and 3D visualization capabilities, this physics-based device simulator can model using semiconductor equations. One, two, or three-dimensional simulations of semiconductor devices are possible with ATLAS. The models that are included include the Auger Recombination (AUGER) Model, the Field-Dependent Mobility (FLDMOB), the Concentration-Dependent Mobility (CONMOB), the Impact Ionisation Model (IMPACT SELB), the Concentration-Dependent Lifetime Model (CONSRH), and the Bandgap Narrowing (BGN).

2.1.1. Proposed Device Process Flow

Figure 2 depicts the process flow of the suggested device, known as Super Junction SPLIT Gate Trench Power MOSFET (SJSGTPMOS). First and foremost, lightly doped n-region epitaxial growth is grown initially on a largely n-doped substrate [11, 12], as shown in Figures 2(a), and (b). Next, p/n pillars are formed by selective etching, as illustrated in Figures 2(c), and (d). It was followed by the growth of P-body, P+, and N+ [15], as shown in Figure 2(e). Further, to mark the trenches, a thermal oxide was patterned and trailed by selective etching, as in Figure 2(f) [13, 14, 16, 17]. The development of oxide layers in the super junction-charged balanced drift layer is the next promising and typical phase [15, 18, 19]. The gates are made by first forming an oxide layer on top of the N-super junction device drift layer, as shown in Figure 2(g) [20, 21], and then using LPCVD to create a 50 nm polysilicon layer. Some of the different options for the SJSGTPMOS process flow are shown above. The materials and fabrication processes utilised have no possible negative effects on the environment and are in line with industry norms and literature.

3. Simulation Results and Discussion

3.1. Breakdown Characteristics

Two crucial factors that control power MOSFETs are the breakdown voltage and ON-resistance. The power MOSFET's performance is determined by its tradeoff (Ron-BV) [1]. The ON-resistance is calculated by dividing Vds by Ids from the linear part of the output characteristic curve, and the device's breakdown voltage is measured at zero gate voltage. Figure 3 shows the breakdown characteristics (BV) of conventional (CTPMOS) and the proposed Super Junction Split Gate Trench Power MOSFET (SJSGTPMOS). The graph shows a significant enhancement in the BV achieved in the proposed (SJSGTPMOS) device when implementing the super junction and split gate techniques. Figure 3 indicates that the breakdown voltage has significantly increased to 33.4V, showing the proposed device's larger voltage handling

capacity, indicating a good trade-off between Ron-BV and a significant rise in Baliga's FOM1 of 74.1% when comparing the SJSGTPMOS with the conventional ones.

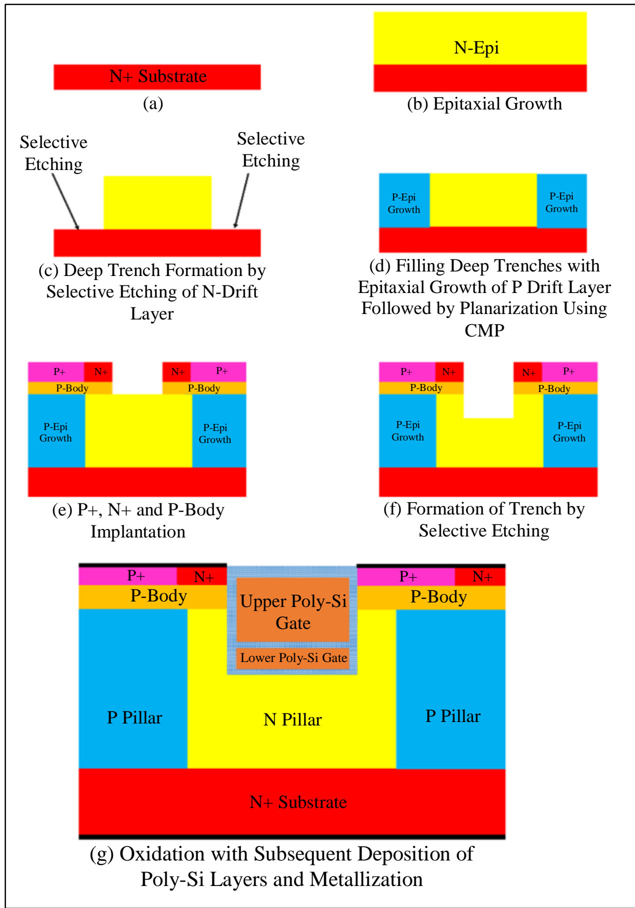

Fig. 2 Suggested procedure for the possible fabrication of the proposed (SJSGTPMOS) device

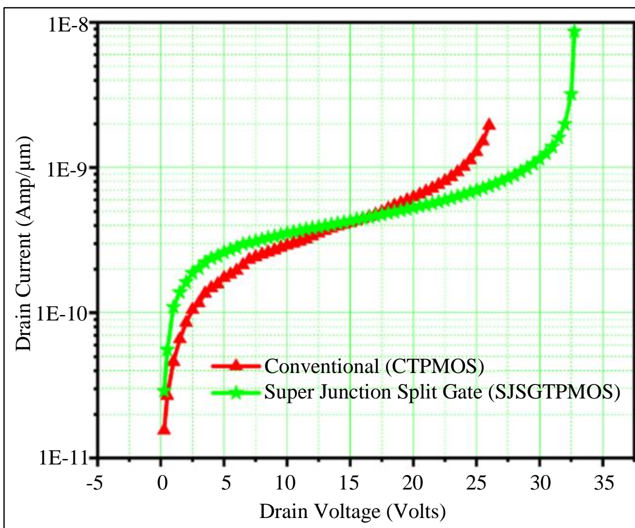

Fig. 3 Breakdown study of proposed (SJSGTPMOS) and the conventional (CTPMOS) devices at Vgs=0V

3.1.1. Gate Charge and Capacitance Analysis

The power device's gate charge has a direct impact on switching loss and speed. Low switching loss and high switching speed are the primary goals; hence, getting a low gate charge value is crucial [21]. Comparing different Poly-Si gate devices to other power devices, a large body of literature has demonstrated the impact on gate charge. Figure 4 below illustrates the circuit [22] that is utilised to provide variation in gate charge. Figure 5 displays the gate voltage vs transient time curve. The gate-to-drain charge (Qgd) is indicated by the plateau (miller) value.

We noticed a smaller simulated value of Qgd in our proposed (SJSGTPMOS) device than in the conventional power MOSFET device. It indicates that the proposed device has a smaller amount of charge Gate-to-Drain Terminals (Qgd) than its counterparts (Figure 5). We have used 10K cells connected in parallel with 10e-6 (Amp) constant current as input for charging the gate. When compared to the standard trench power MOSFET, the proposed SJSGTPMOS device's Gate-to-Drain Terminals (Qgd) is only 25.1 pC, indicating an 81.8% reduction in gate charge, as seen in Table 2. The typical device's gate charge is 138 pC. The output above illustrates the possible impact of using the Split Gate with Super Junction concept in our proposed (SJSGTPMOS) device's drift region.

Furthermore, Table 2 shows the comparative investigation of various performance-determining parameters of the two devices. The table shows that the proposed (SJSGTPMOS) device outperforms the conventional (CTPMOS) devices in terms of Breakdown Voltage (BV) and Qgd. Moreover, the performance of a power MOSFET in terms of the tradeoff between BV, Ron.sp, Qgd, and Cgd is studied, indicating the power device's switching and conduction loss.

The two Baliga's figures of merit, which specify the overall tradeoff between the three parameters, have also been examined. Balliga's figure-of-merits are FOM1 (=BV^2/Ron) and FOM2 (=Ron. Qgd). The high value of FOM1 for a commercial power device suggests a low ON resistance value and a high voltage sustaining breakdown voltage, both of which are desirable. On the other hand, FOM2 ought to show a low gate-to-drain charge (Qgd) and ON-resistance. Comparing our suggested device to the standard (CTPMOS), Table 3 demonstrates a significant enhancement in the extracted figure of merits (FOM1 and FOM2). The full performance situation of our suggested device in Comparison to the Traditional MOSFET (CTPMOS) is shown in Tables 2 and 3, taken together.

The differences between the proposed Super Junction Split Trench Gate Power MOSFET (SJSGTPMOS) and the traditional device as a function of drain-to-source (Vds) voltage are displayed in Figure 6, demonstrating the superiority of the proposed (SJSGTPMOS) device over the

conventional MOSFET. The graph represents the depletion region capacitances related to the p/n vertical pillars of a double charge-balanced proposed device. It is highly subtle when applied to Vds voltages. This phenomenon is more dominantly visible exclusively in its lower range due to the prevailing circumstances, like the availability of larger non-depleted surfaces and the minor depletion region formed across the charge-balanced p/n pillars, resulting in greater output capacitance. The spreading of depletion regions sideways with Vds reduces output capacitances (Cgd and Cds). This phenomenon continues over the entire depletion of the drift region, as presented in Figure 6.

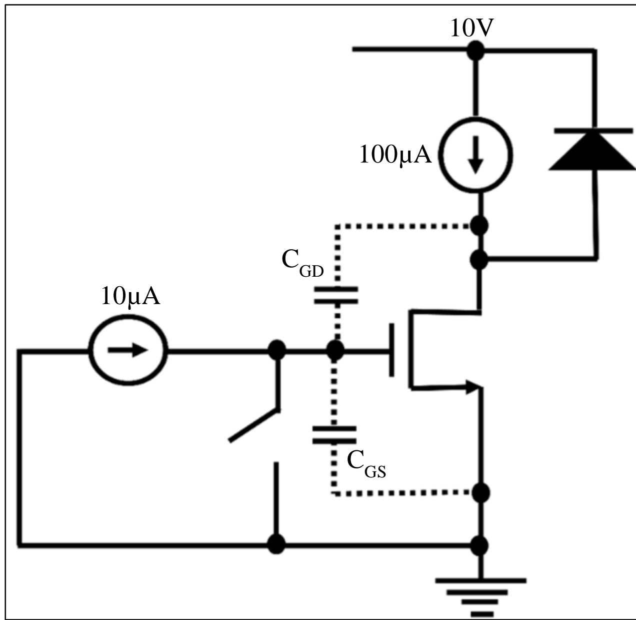

Fig. 4 Mixed-Mode Gate charge simulation circuit used to measure gate to drain charge (Qgd)

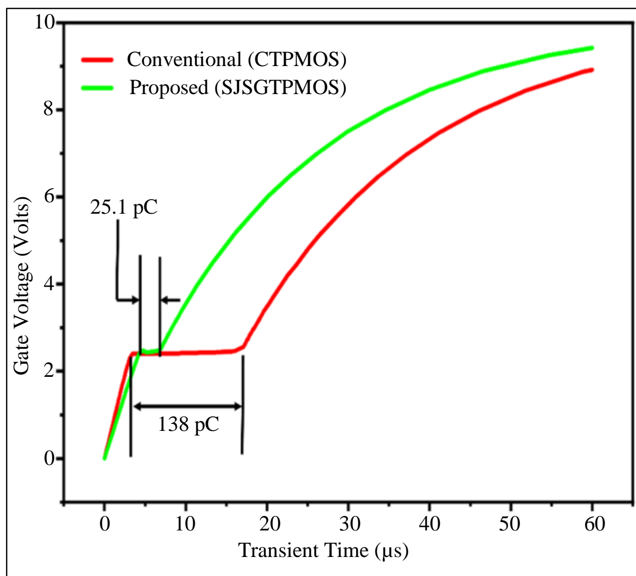

Fig. 5 Transient analysis of the proposed (SJSGTPMOS) and the conventional devices

Table 2. Performance comparison of the two devices

Parameters	CTPMOS	SJSGTPMOS
Drift doping	5e16/cm^3	5e16/cm^3
Ron.sp (mΩ.cm^2)	0.68	0.71
BV (v)	25.0	33.4
Qgd (pC)	138	25.1

As shown in Figure 7, the output capacitances of the suggested (SJSGTPMOS) device exhibit further improvement when compared to the traditional power trench MOSFET. Furthermore, we have shown a significant decrease in the total gate capacitance change of the suggested device when compared to the conventional (CTPMOS) MOSFET, as shown in Figure 8. Our suggested device works better than the standard one and provides great dynamic performance in both Figures 7 and 8.

In Figure 8, we demonstrate a reduced total gate-to-gate capacitance (Cgg) of the proposed SJSGTPMOS device at Vds= 10 V, with Vgs variation. This reduction in Cgg is because of the super junction concepts applied with the additional gate splitting. The suggested device's capacitance value is significantly lower than that of the traditional device, as indicated by the total gate capacitance (Cgg), which fluctuates with Vgs.

Table 3. Figure of merit comparative analysis

Figure of Merit (FOM)	CTPMOS	SJSGTPMOS
FOM1 (MW/cm^2)	0.919	1.6
FOM2 (mΩ.nC)	312.8	59.4

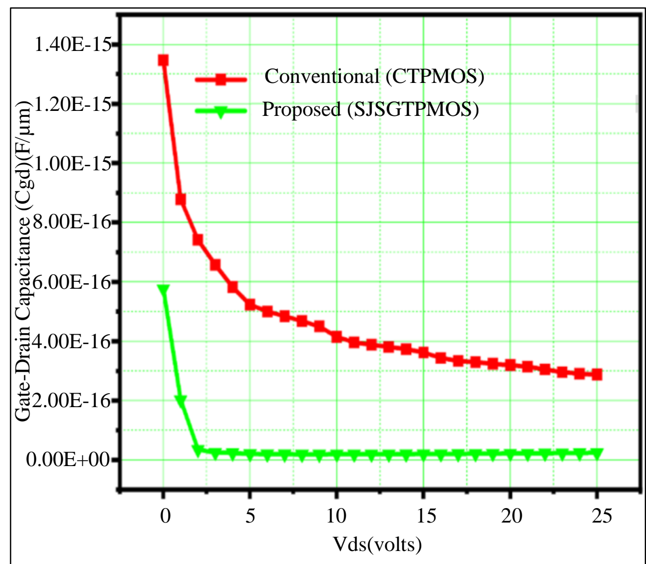

Fig. 6 Gate-to-drain capacitance (Cgd) vs gate voltage variation of the two devices

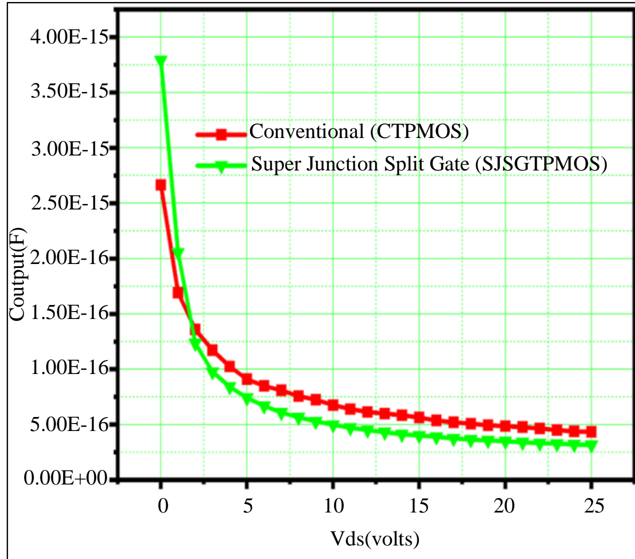

Fig. 7 Variation of the two devices' output capacitance (Coutput) in relation to gate voltage

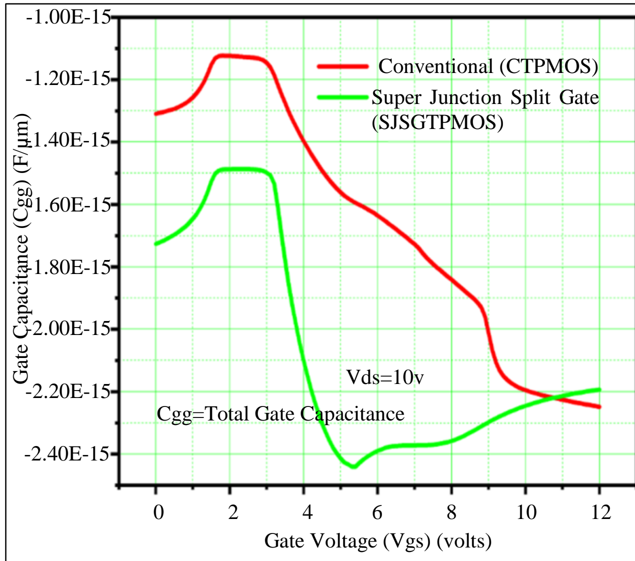

Fig. 8 Total gate capacitance (Cgg) vs gate voltage variation of the two devices

Table 4. Qgd values with upper gate thickness variation in the proposed device (SJSGTPMOS)

Upper Gate Thickness (µm)	1.0	0.7	0.55
Q_{gd} (pC)	25.1	9.9	0.94

3.1.2. Oxide-Gate Thickness Variation and Device Gate Charge Performances

We altered the thickness of the upper gate of SJSGTPMOS, as shown in Table 4. We got the best minimum values in the gate charge (Qgd) at 0.55 µm upper gate thickness, as shown in Figure 9, showing the variation of gate charge with upper gate thickness variation. Since the gate thickness is impacted by the growth in oxide thickness, the graph displays a very low value of gate-drain charge (Qgd). As a result, the gate is now farther from the drain and does not extend much further inside the drift region, which lowers the coupling between the gate and drain and has a major impact on the Qgd. Thus, as Figure 10 illustrates, we also observe a notable decline in FOM2.

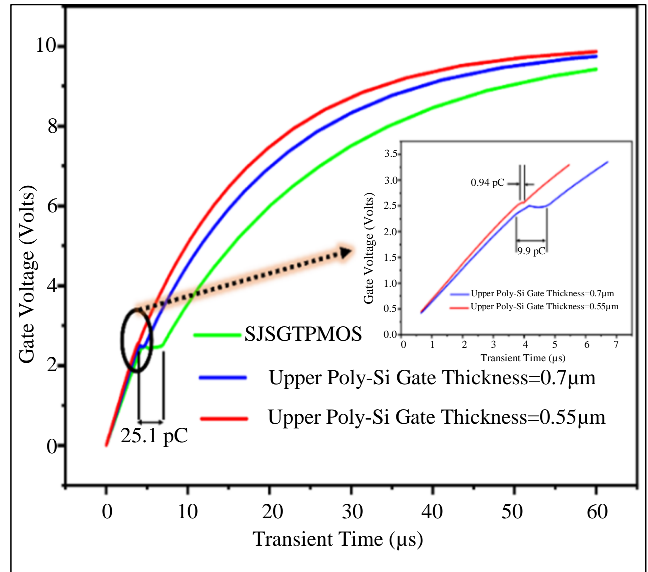

Fig. 9 Gate charge value and curve with variation of gate thickness in SJSGTPMOS

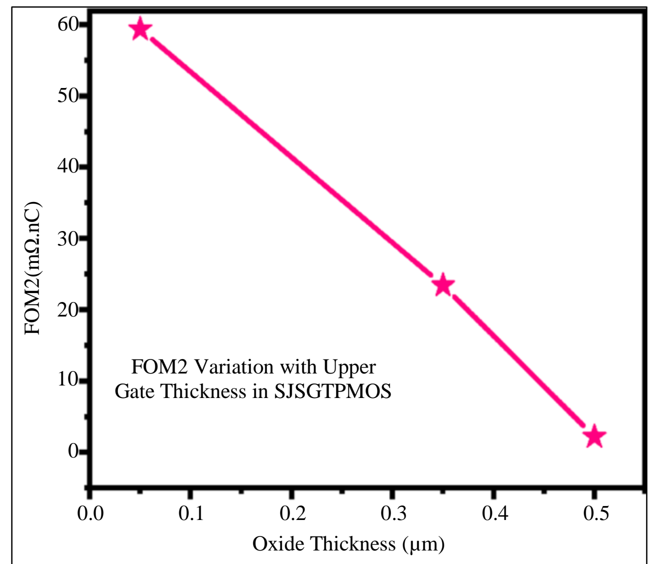

Fig. 10 FOM2 variation of upper gate thickness in SJSGTPMOS

3.1.3. Comparison of SJSGTPMOS with other Various Commercial Low Voltage 25V Power MOSFET and its Variant

The proposed device compares with the commercially available power MOSFET devices at 25V. We have compared this with our proposed device and plotted the same relative

FOM. The relative FOM is attainable in our proposed SJSGTPMOS alongside the FOM reachable in TI's NexFET and NexFET, as shown in Figure 11, indicating a significantly reduced FOM2, which is a significant improvement compared to reported structures.

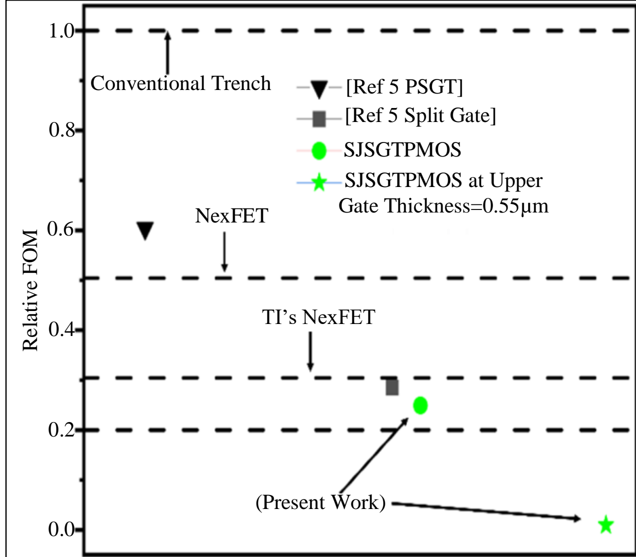

Fig. 11 Relative FOM comparison of the proposed SJSGTPMOS with Conventional Power Trench MOSFET and TI's state-of-the-art NexFET device

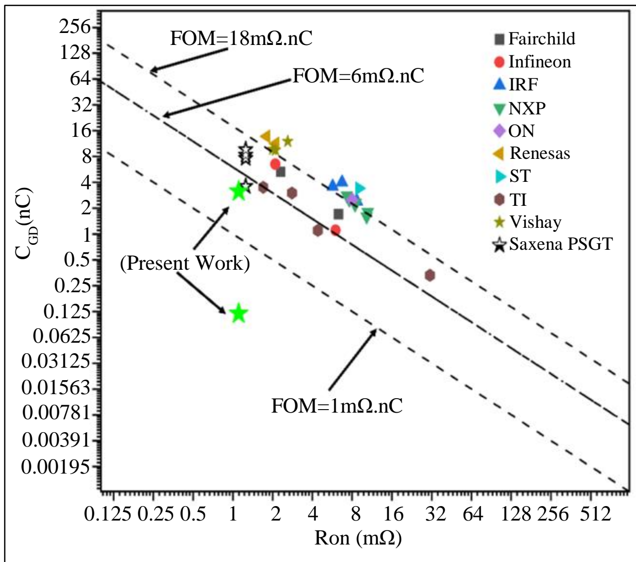

Fig. 12 Commercially available low voltage devices comparison with our proposed SJSGTPMOS (present work)

For better comparison and more profound understanding, the FOM values (for low voltage 25 volts) are plotted in Figure 12 by considering 1.56M cells connected in parallel, resulting in FOM2 as low as 3.138 mΩ.nC and 0.118 mΩ.nC for our proposed SJSGTMOS on varying gate thickness.

4. Conclusion

A new vertical power MOSFET structure using a double charge balanced design technique by combining the unique feature of the RESURF Split Gate with the Super Junction concept proposed in this paper. The split gate 2-D Reduced Surface Electric Field (RESURF) effect and super junction p/n pillar strips technology improves the device performance and lessens the overall requirement of Gate-to-Charge terminals (Qgd) and Gate-to-Drain Capacitive (Cgd) coupling.

A very low simulated value of 0.94 pC Gate-To-Drain Charge (Qgd) is reported in this work, followed by significant improvement in breakdown voltage (33.6%), FOM1 (74.1%), FOM2 (99.29%), Cgd (91.62%) is achieved in the proposed one, showing the enhancement features of the proposed structure over the existing state-of-the-art in terms of performance using two different charge balanced technology.

Based on the aforementioned findings, we can conclude that the double charge method used in vertical trench MOSFETs helps provide a very high switching device while lowering switching and conduction losses. Our proposed device can be employed as a highly rapid switching device with a breakdown voltage range of 0-50 V and a low cell pitch of 3 µm. It may find use in automotive electronics, specifically as power converters in contemporary electric vehicles and as switching devices in electronic control units.

Acknowledgements

All the authors would like to recognize the support from Indira Gandhi Delhi Technical University for Women (IGDTUW), Delhi and Jamia Millia Islamia (JMI), New Delhi.

Ethical Concerns and Data Handling

We guarantee that your results are appropriately represented and that our work is free of plagiarism and research dishonesty.

Author Contribution

Our current suggested structure (device) was conceptualised by Sajad A. Loan and M. Ejaz Aslam Lodhi. Additionally, M. Ejaz Aslam Lodhi designed the gadget and performed the simulation. The result discussion, justification, analysis and manuscript write-up has been done by M. Ejaz Aslam Lodhi, Abdul Quaiyum Ansari and Sajad A. Loan.

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