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Original Article

A Minimum Component Seven-Level Switched-Capacitor Triple Boost Inverter (SL-SCTBI)

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Abstract *- Switched capacitor topologies provide a path towards elevated voltage outputs via the stored energy of capacitors without the need for multiple DC power supplies. The article proposes a new triple boost inverter topology, which is optimized to increase the voltage output while keeping the component count small in order to be applied in renewable energy applications. The Seven-Level SC Triple Boost Inverter (SL-SCTBI) operates with a single DC source with a voltage gain of three times higher than the input with the help of only 8 switches, two diodes and two capacitors. Reduction in its component count and system complexity contributes to higher efficiency and general practicality. A comprehensive comparison study that includes a number of elements, including the number of power electronic devices, gate driver circuits, and capacitors, is described. Since the voltage stabilization occurs at the inverter node, the use of self-balancing capacitors enables circuitry-free stabilization. Comprehensive simulations and laboratory experiments of the SL-SCTBI performance are presented to assess the functionality and effectiveness.*

Keywords *- Minimum component, Self-balancing capacitors, Seven level, Switched-capacitor, Triple boost, Voltage gain.*

1. Introduction

Multilevel Inverters (MLIs) have gained popularity in recent years in the power sector. In [1], a 7-level multilevel inverter that operates through a SIDO converter to produce voltage gain and lower stress on voltages. Although it enhances power quality, there are still two major drawbacks - higher system complexity, increased system cost and possible THD problems in real-world applications. A novel seven-level inverter uses an 8-switch, 4-diode and 4-capacitor modular switched-capacitor circuit to obtain a 4x voltage output and is presented in [2]. The system maintains different switch controls for level generation, and at its highest stress level, it permits up to 4 volts across the switches. The seven-level inverter experiences voltage imbalance between capacitors during states P1 and N1, while its intricate control strategy makes implementation more difficult. With only 9 switches and 2 capacitors, the 7-level inverter system creates multilevel performance, while lowering the parts count as well as eliminating diodes to minimize device expenses in [3]. The control method for capacitor self-balancing requires precise implementation, which becomes difficult when operating under varying load conditions while maintaining low voltage stress across switches. The device provides regenerative functions, but its operational suitability depends on the successful management of load conditions [4]. In [5], the hybrid 7-level inverter uses 7 switches and diodes along with 4 capacitors to achieve a 1.5x voltage gain with reduced voltage stress. However, its practical implementation is challenged by design complexity and the requirement for large capacitors. Despite good efficiency, capacitor losses significantly contribute to the overall power loss. In [6], the seven-level common-ground transformer-less inverter uses 8 switches, 4 diodes, and 3 capacitors, achieving voltage gain with just 33% of the input DC voltage. It maintains capacitor voltage balancing without extra control. However, the high switch count reduces reliability and increases failure points, while high operational frequencies lead to challenges in managing switching losses and efficiency. Through its 8 switches, 1 diode and 2 capacitors configuration, the seven-level triple boost inverter generates three times the input voltage at the output while reducing switching losses with four fundamental frequency operating switches is presented in [7]. The device operates under voltage stress that extends from Vdc to 3Vdc, while the Total Standing Voltage reaches 6.66. A drawback exists because proper voltage management becomes mandatory to prevent capacitor imbalance from occurring. In [8], MLI described uses 9 switches to achieve a 3x gain and a total standing voltage of 6 pu. It efficiently generates seven output levels, but lacks support for additional voltage sources, potentially limiting its application. Further optimization and testing are needed to ensure performance under varying load conditions. A seven-level boosting multilevel inverter reaches a voltage gain of 2 through its 10 switches, 2 capacitors and diodes, while conducting 4 switches at each level, which is designed in [9]. The distribution of switch voltage stress becomes more uniform in

the system, resulting in reduced total switching voltage. The implementation of this inverter faces hurdles because of technical complexities in creating control signals and technical challenges that impact efficient voltage balancing through switched-capacitor technology. In [10], a topology is presented that generates a seven-output voltage system through 6 switches joined with 2 capacitors to achieve voltage boost with decreased DC-link voltage. FCS-MPC presents control complexity and high computational requirements that limit its real-time implementation in the modified inverter. In [11], more devices are used to achieve a peak voltage gain of 6, with dedicated switches for polarity and level generation, maintaining low voltage stress. However, the complex configuration layout and susceptibility to partial shading can impact its efficiency.

In [12], the authors use more devices and components to achieve voltage gain with minimized conduction losses, with only three switches conducting at maximum output voltage. However, it faces challenges from high electromagnetic interference, significant power loss, and limited power capacity, requiring resolution for efficient HFAC deployment. The new seven-level Common Ground (CG) inverter in [13] uses 6 power switches, 2 bidirectional switches, and 2 diodes with 2 switched-capacitor cells and a virtual dc-link capacitor, achieving a 3x voltage gain with 11 conducting switches. However, the circuit requires high capacitor values to generate voltage steps and balancing capacitor voltage becomes important under varying load conditions. In [14], a seven-level common-ground inverter employs 14 switches together with 3 capacitors to reach 3x voltage gain, which boosts its capabilities. The capacitors produce high inrush currents that create design problems for reliability and efficiency, while most switches maintain low voltage stress. The management of these currents needs careful attention to support solar PV applications while maintaining component balance throughout operation, ensuring performance durability. A seven-level doubly grounded photovoltaic inverter uses 9 switches and 3 capacitors, achieving voltage gain to generate seven levels with low voltage stress, is presented in [15]. However, the complexity of managing multiple states and the need for precise control strategies may increase system complexity and cost.

Additionally, the reliance on predictive control requires substantial computational resources, limiting its use in less advanced systems. In [16], an NPC-based switched-capacitor grid-tied inverter is developed to get a 4x boost. It generates 7 voltage levels with 8 conducting switches, minimizing voltage stress on components. However, managing capacitor voltage balance at the input is challenging, and advanced control strategies are needed for optimal performance. A seven-level transformer-less inverter implements 6 unidirectional switches along with 2 bidirectional switches, 4 capacitors and 2 diodes to produce a 1.5x voltage gain is presented in [17]. The system provides lower voltage stress, but its production relies on multiple elements, which could affect production efficiency. Long-term testing of the device under high-power operation conditions needs research to evaluate stability, together with reliability performance. The SC-MLI presented in [18] needs more semiconducting switches to deliver 3 times the voltage gain through a design without magnetic elements. As a voltage level generation mechanism, the inverter uses 10 unidirectional and 2 bidirectional IGBT switches, which maintain the stress at the DC source voltage level. The practical application of the system faces difficulties because of its complex design and its dependent precise control mechanisms, together with possible switching losses. The MLI design presented in [19] produces a 3x voltage boost. The system relies on 4 switches to produce different voltage levels, thus reducing voltage strain. However, the design presents obstacles because of advanced control system difficulties, together with sub-optimal operation across different load kinds. In [20], an inverter with a 1.5x voltage gain. It has seven conducting switches, which reduce conduction losses and limit voltage stress to 1.5Vdc. However, the main limitation is the complexity of control strategies for modulation and managing capacitor charge dynamics.

Through the combination of 10 switches and 2 diodes alongside a single flying capacitor, the proposed inverter system in [21] attains 1.5x voltage gain through its seven voltage levels with minimal conducting switches. Operation complexity increases when the system depends on a flying capacitor to function, even though the maximum blocking voltage stays below input voltage parameters. The operational component voltage stress distribution needs special attention during the system's utilization phase. In [22], an inverter design to achieve a 1.5x voltage boost, with maximum voltage stress at the source voltage and no diodes. It features varying stress levels across the switches for level generation. However, its design may not be suitable for applications requiring very high voltages or rapid dynamic response, and the complex control algorithms may pose challenges in more advanced applications.

In [23], a seven-level switched capacitor design is presented to reach 2Vdc of voltage gain through operation with 6 switches, 1 diode and 3 capacitors. The system protects both the efficiency and voltage distribution across devices. This design presents some disadvantages, including the capability to generate high inrush currents during capacitor switching events and the minimal redundancy available throughout the configuration. In [24], a seven-level inverter design contains 8 switches together with a single diode and 2 capacitors to generate a 3 times voltage gain and reduce component stress. The system needs advanced control programs for its modulation process, yet it encounters problems when adjusting to different load requirements. Skilled management of the self-voltage balancing system becomes essential to stop capacitor voltage imbalance from occurring.

The seven-level transformer-less inverter proposed in [25] uses 12 switches, no diodes, and 3 capacitors to achieve a 1.5x voltage gain, operating in dual modes for both buck and boost functionalities. Furthermore, linking reactive power capability with higher voltage levels may affect system efficiency and increase costs. The design presented in [26] utilize 7 switches and 2 capacitors to get 0 to ±0.5V, ±V and ±1.5V to get a 1.5x voltage gain. The inverter has a low switch count, but the switches may face high voltages during operation. The inherent capacitance balancing becomes less efficient when the inverter is operated at higher frequencies or under varying conditions.

The basic design principle of this inverter reduces its ability to adapt to operational requirements that are different from the initial specifications. The SCMLI circuit in [27] consists of excess devices to get a 3x boost. However, the design may have limitations in scalability and efficiency compared to more complex multilevel inverters, which could affect its use in higher power systems. A 7-level ANPC converter in [28] produces a significant boost. It relies on specific switches for level generation, improving output voltage control. However, the system's complexity adds more components, potentially increasing costs and maintenance needs. Additionally, the implementation of the control strategy may cause time delays, negatively affecting dynamic response speed. A 7-level inverter in [29] uses 8 switches, 2 capacitors, and 2 diodes to achieve a 1.5x voltage gain. Only 4 switches conduct at any time, reducing conduction losses, and the design prevents switch voltage stress from exceeding the input voltage. However, high inrush currents during capacitor charging could limit prolonged use in varied applications, requiring the inclusion of a soft-charging cell to mitigate this issue.

Using three conducting switches simultaneously, the proposed seven-level inverter in [30] functions by combining 6 switches with 2 diodes and 3 capacitors to generate 1.5x voltage gain. The design could encounter high charging current stress despite the resonant cell implementation, but this condition affects the overall efficiency performance under diverse load situations. The topology presented in [31] obtains 3x voltage gain by using 8 switches and 2 diodes with a single capacitor to create up to 7 voltage levels when 4 switches operate in the capacitor charging path. The inverter topology combines soft-charging functions with decreased impulse charging current flow. Voltage balancing components must be implemented for this topology when operating, and scalability for increased voltage levels poses potential difficulties. The greater number of components in traditional systems may reduce reliability metrics compared to the new proposed solution. The SCMLI in [32] has 9 semiconductor switches and 2 capacitors to produce 1.5 times the voltage gain. The design eliminates the necessity of extra diodes to achieve its functionality, which makes it simpler than conventional models. Self-balancing capacitors of the inverter allow efficient level creation with lowered switch voltage stress. The technique needs supplementary floating capacitors that raise both costs and system complexity. The inverter described in [33] requires a single DC source combined with 9 switches with a 3x boost. This design implements capacitor voltage balancing and controls charging current spikes. The design system encounters three main problems: it requires complex control mechanisms, poor scalability capability and its dependency on a single power supply, thus restricting its overall versatility. The design efficiency improves through selective component choices for managing switch-related voltage stresses. The 7L-SCMLI in [34] requires 8 IGBT switches, 1 diode, and 3 capacitors for a 3x voltage gain capability.

The system produces output voltage steps from different switch voltages, causing each switch to handle either a single or double input voltage value. Additional switches increase open switch fault possibilities, but the solution does not address fault detection for other semiconductor-based failures; thus, both issues demand better fault management techniques within this topology. The inverter architecture in [35] produces a 3-times voltage gain with automation of SC voltage balance and reduced conduction losses. Because of its restricted number of switches, the system faces limitations in scalability and flexibility when operating at higher power applications.

The system removes ground leakage current, yet its reliability might be compromised due to variations in load conditions in specific situations. In [36], topology helps to obtain a seven-level output voltage with a 1.5x larger output, but the design has some limitations related to its complexity and the need for additional components that may impact the cost and scalability of the system in practical applications. The inverter presented in [37], 7LBI, operates with 7 power switches and 2 capacitors to operate at 1.5x voltage gain without the need for additional diodes and performs inherent voltage balancing through sensorless methods.

The reduction of devices combined with lowered voltage stress remains subject to challenges regarding state management and high-power requirements. The conducting switches operating stress levels produce certain voltage conditions that require detailed planning to maintain efficiency. The seven-level inverter developed in [38] achieves a voltage gain of 1 through the combination of 10 switches and one capacitor. The basic arrangement of the design helps to minimize the number of devices and control sudden current increases. Operating the design in high-power situations may lead to maximum efficiency limitations and enhanced thermal degradation. Safety measures for components in reactive systems should be established because they help to prevent problems that occur during practical application. In [39], a topology is described to generate a 2VDC voltage gain. The implementation uses fewer

components while offering better protection against capacitor voltage stress to enhance operational dependability. The implementation complexity increases because proper voltage balancing control procedures are necessary. The review of the literature shows that there is a good opportunity in the development of new inverter designs with higher boosting factors.

The paper introduced an inverter circuit that will make use of the Switched Capacitor (SC) technology. This paper presents SL-SCTBI with a Minimum component as shown in Figure 1, with the following key advancements:

- Reduced component count
- Triple voltage boosting capability
- Enhanced DC utilization with continuous input current
- Stable performance under dynamic load or input variations
- Lower voltage ripple across capacitors

This paper starts with an introduction, followed by a description of the SL-SCTBI layout, its working parameters in section 2, and the control mechanisms accordingly. Section 3 is a detailed comparison of the previous Multilevel Inverter (MLI) designs, Section 4 depicts testing results, and Section 5 concludes the study.

2. SL-SCTBI and Functional Modes

2.1. SL-SCTBI Configuration

Figure 1 Illustration of the SL-SCTBI. A single input unit supplies power to 2 floating capacitors; the two capacitors are designated using the terms C1 and C2. C1 and C2 are designed in such a way that they can accept Vs on the input terminal. The SL-SCTBI switches are regulated with two diodes (D1 and D2) and 8 power switches on T1-T4, as well as RU, RL, LU, and LL. The ideal switching sequence would be one that enables the charging of the capacitors with the DC and discharging into the load at a balanced voltage on all the capacitors.

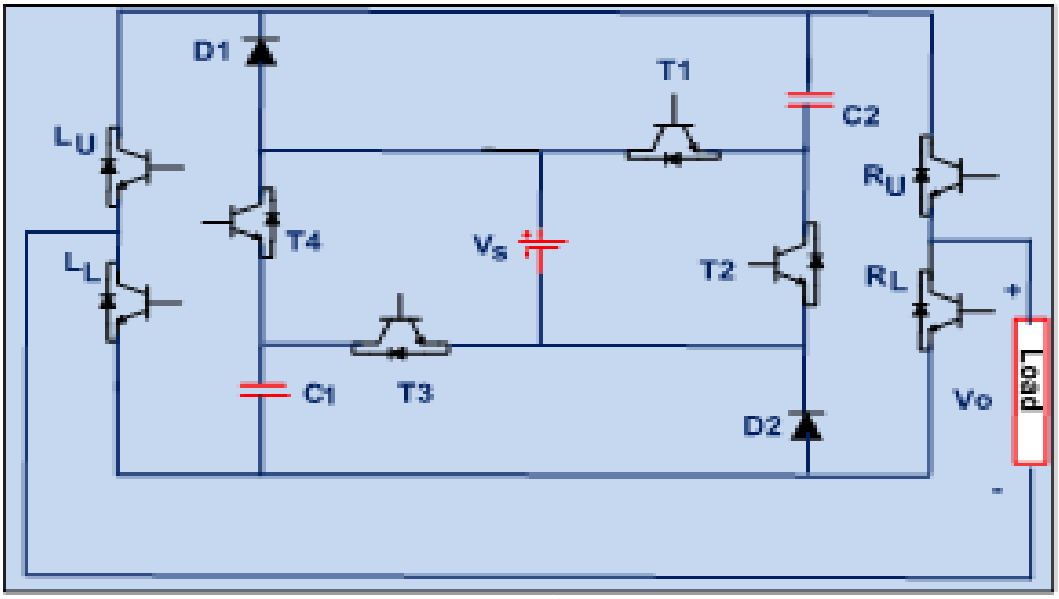

Fig. 1 Topology of SL-SCTBI

Table 1. 7 level switching states

Vdc	T1	T2	T3	T4	R_U	L_L	L_U	R_L	C1	C2
+3Vs	1	0	1	0	1	1	0	0	↓	↓
+2Vs	1	0	0	1	1	1	0	0	↓	↑
+Vdc	0	1	0	1	1	1	0	0	↑	↑
+0	0	1	0	1	1	0	1	0	↑	↑
-0	0	1	0	1	0	1	0	1	↑	↑
- Vs	0	1	0	1	0	0	1	1	↑	↑
-2Vs	1	0	0	1	0	0	1	1	↓	↑
-3Vs	1	0	1	0	0	0	1	1	↓	↓

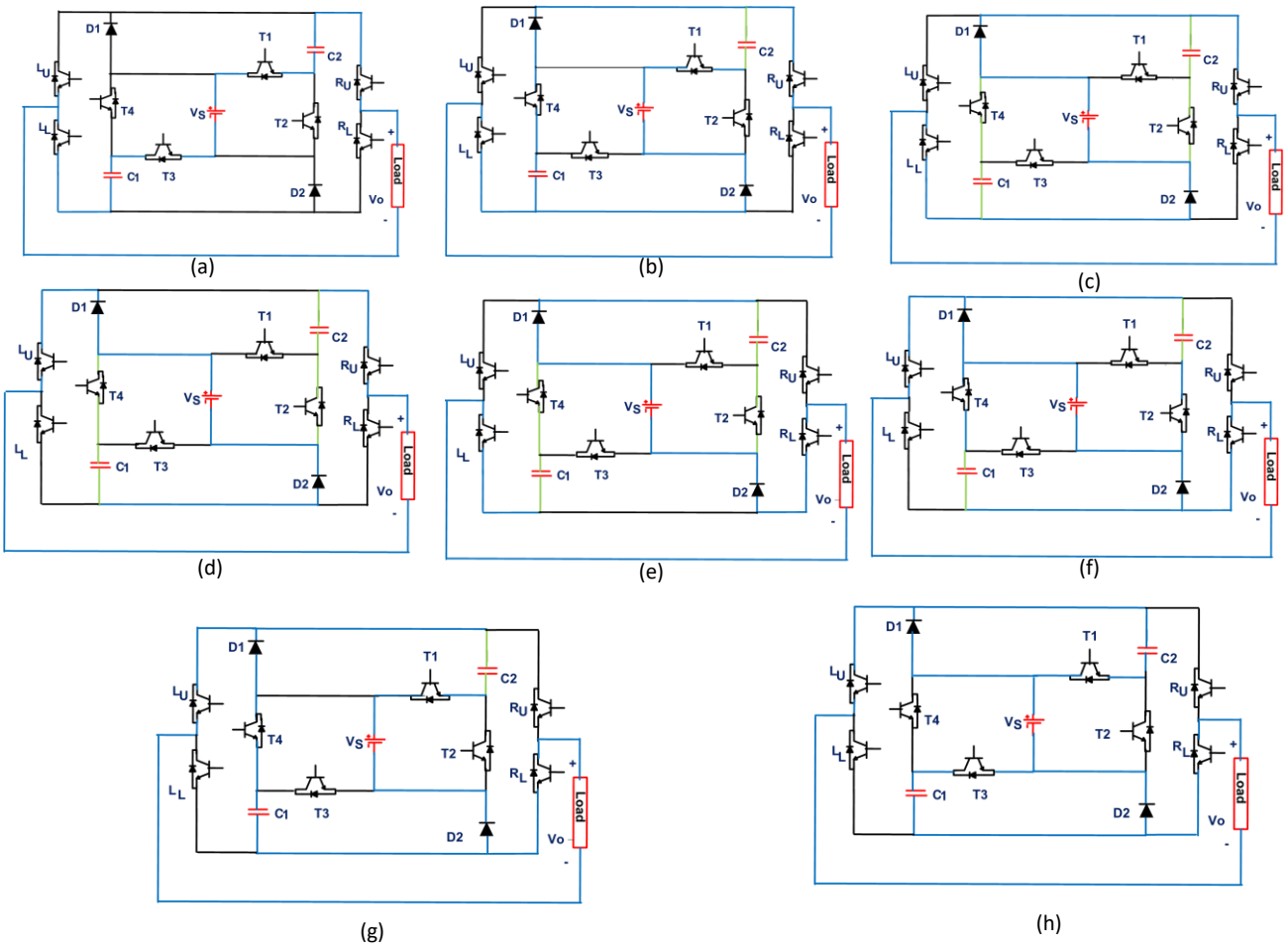

Fig. 2 Operational stages of SL-SCTBI (a) +3Vdc, (b) +2Vdc, (c) +1Vdc, (d) +0, (e) -0, (f) -1Vdc, (g) -2Vdc, and (h) -3Vdc.

SL-SCTBI operates in numerous distinct modes. First, the charge phase begins by switching certain switches and connecting the DC source and floating capacitors. The visualization of the various working modes of the SL-SCTBI is given in Figure 2, in which the flow of current under charging and load conditions is shown. The discussion is initiated using the positive half cycle. In this case, the direction of charging is not changed, but the polarity of the switch is inverted; RU and LL rather than LU and RL become activated. In Mode 1 (+Vs) C1 and C2 are charged to Vs leading to Vs as could be observed in Figure 2. To charge c1, VS flows through diodes D1 charging c1 through T2, and back to VS. Similarly, Vs goes through the T4 to charge C1 through the diodes D2 andback to the Vs to charge the C2. In the load, the current will flow through D1, leading through RU, and the load and the LL through D2 will go back to Vs. The state changes to Mode 2 (+Vs+VC1), capacitor C1 is discharged and capacitor C2 is charged up to +Vs, thus +2Vs is present in the load, as Figure 2 shows. The current paths are as shown below: Vs passes through T4 and charges C2, therefore activating D2 to allow charging of C2 through T4. C1, being the load, is fed to T1 to Vs, then through D2 and ultimately passes out LL and RU. In Mode 3(+Vs+VC1 +VC2), capacitors C1 and C2 are discharged through transistors T1 and T3, which are also connected to the load and +Vs. As a result, C1 and C2 charge the load so that +3V is obtained. The Vs goes through T1, drains C1, then goes through RU to LL, back to C2 through T3, and back to the Vs.

Moreover, capacitors in mode 4 (+0Vs) discharge and hence the load voltage is reduced to +0Vs as shown. The operation modes are reversed, so switches LU and RL are turned on. In mode 5 (-Vs), C1 and C2 are charged to -Vs, and the output obtained is -Vs. The pathway is as follows: To charge C1, the negative of Vs flows through diodes D1 to charge C1 through T2, and back to +Vs. Similarly, to charge S2, the −Vs flows through T4 and charges C1 with the help of diodes D2, and then it finds its way back to Vs. Vs causes Vs to flow through D1, which then returns negative Vs to the load through LU, load, RL and D2. When in mode 6 cases (−Vs−VC1), capacitor C1 discharges and capacitor C2 charges to Vs (see Figure 2), the capacitor voltage reaches

2Vs. The existing circuits are as follows: To charge C2, the current −Vs exists in the direction: T4 minus C2; therefore, D2 is turned on to achieve charging C2 through T4. C1 is discharged to -Vs via T1, then through D2 and finally through LU and RL, under mode 7 (−Vs− VC1− VC2), capacitor C1 and C2 drain via T1 and T3, which are connected to load as well as -Vs Thus, both C1 and C2 are linked with load and discharge giving a load voltage that is a value of -3Vs.

The current will be −Vs will discharge C1 and through LU and RL, C1 will flow through T2 to return to Vs. Switches T1 to T4 are either source voltage stressed with Vs, but the other switches, RU, RL, LU, and LL, receive the greatest voltage stress at 3Vs. The planned SL-SCTBI has a stand voltage of 16 volts. Figure 3 depicts the voltage stress that the components would undergo at every level.

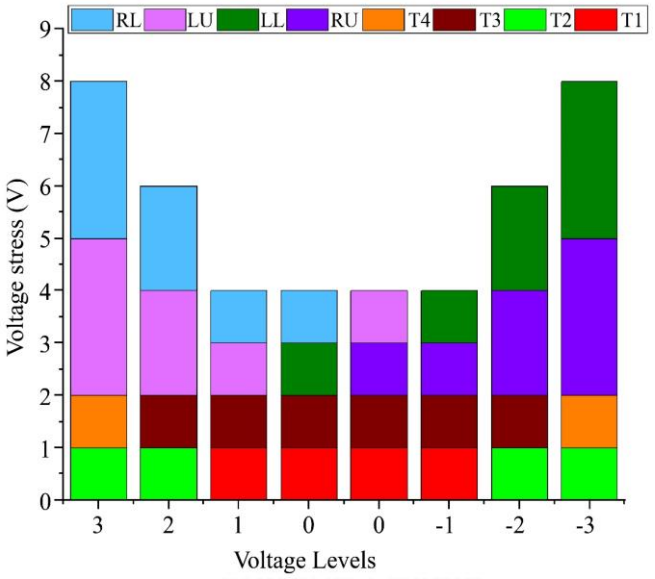

Fig. 3 Stress on the inverter switching device

2.2. Control Methodology

In LSPWM, the M-level inverter method employs (M-1) carriers with the same amplitude, frequency swinging peak to peak. Multilevel Inverters (MLIs) more often use the LS-PDPWM modulation approach since it is less complex, theoretically straightforward, and can be controlled in various ways. This method produces a voltage output using seven different energy levels and six carrier signals.

All these signals are synchronized to maintain the same frequencies. This coordinated array is the so-called title of the Phase Disposition PWM method. The founding pattern is at the zero-reference point as presented in Figure 4(a). The carrier signals are between -3 and 0 and between 0 and +3, and are in phase with the neighbours carrier signals. Switching pulses, appropriate to the switches, are generated with logical circuits. The pulses of the SL-SCTBI arrangement are depicted in Figure 4(b).

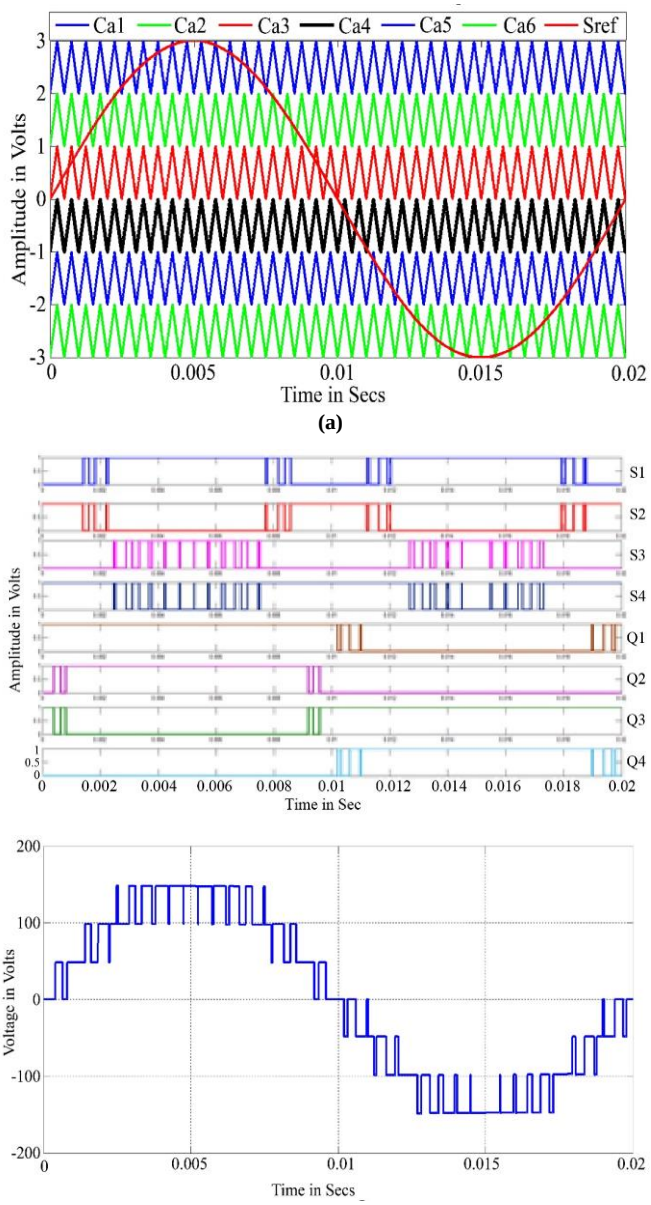

Fig. 4 LS-PDPWM (a) Setup of carriers, and (b) Switching signal.

3. Comparative Assessment of SL-SCTBI Configuration with Recent Literature

The structure proceeded with a detailed comparison of several recent topologies, as shown in Table 2. The evaluation confirmations that most configurations have a relatively high devices, for some of the topologies use up to 17 switches [27], 2 diodes [3], and even 1 capacitor [27] to increase the system complexity and TSV. On the whole, all the topologies can achieve a voltage gain of 3; however, a few of them do it with fewer components. For instance, the proposed Reference 'P' topology is unique and has the best performance of all the metrics. It generates the necessary seven-level output using a single input source, 8 switches, 2 diodes and 2 capacitors.

Table 2. Comparison with the recent configuration

Ref.	Level	Source	Switches	D	C	TSV	Gain
1	7	1	9	2	2	3	3
3	7	1	9	12	2	17	3
6	7	1	8	4	3	6	3
7	7	1	9	1	2	6	3
8	7	1	10	2	2	1	2
9	7	1	6	0	2	2	1
11	7	2	7	2	1	7	3
12	7	1	11	2	3	7	3
13	7	1	14	0	3	3	3
17	7	1	12	2	3	14	3
18	7	1	8	3	3	3	3
22	7	1	10	2	2	8	3
23	7	1	8	1	2	6	3
26	7	1	10	1	2	6	3
27	7	1	16	0	5	3	3
30	7	1	10	0	1	3	3
32	7	1	9	2	2	5	3
33	7	1	8	1	3	10	3
36	7	1	10	0	1	2	3
P	7	1	8	2	2	5.3	3

Additionally, it achieves the low TSV of 5.3, which is among the best in comparison, and maintains a voltage gain of 3. Compared to any other designs, the proposed SL-SCTBI topology shows a much better efficiency and compactness than TSV = 17 [3] and TSV = 14 [17]. The combination of high performance with a low number of components and semiconductor volume yields the proposed inverter as the optimum solution for renewable energy applications due to its compactness.

4. Findings of SL-SCTBI

4.1. Findings through Simulation

Simulations of the SL-SCTBI designs with MATLAB-SIMULINK indicated the efficacy of the technique proposed. The suggested design is assessed for performance and its effectiveness using the LS-PDPWM strategy. This arrangement is optimized to give an output of 7 levels from input 50 V to 150V. The modulation Index of 1 and 2 kHz is used to assess the performance of the SL-SCTBI setup. The effectiveness of both the steady-state and dynamic cases is tested by applying unity modulation measures. The resultant voltage and current values, with a resistive load of 100 ohms, are shown in Figure 5 and 6, along with the respective FFT graphs. Figure 6 shows that the harmonics of the voltage and current were observed at 13.28 % percent. The SL-SCTBI is tested with an RL load of 100 ohms and 250 mH. The voltage and current waveforms in Figure 7 and Figure 8 are shown together with their corresponding spectra. The load voltage showed no change even when there was a significant change in load. Recorded voltage and current harmonics were volt: 13.22 % and current: 0.66 %. The findings reveal effective inductive loading management in the SL-SCTBI design, which makes it suitable for applications involving inductive loading. The resistive-inductive load of 100 ohms and 400 mH was also tested using the SL-SCTBI design. Figure 9 shows harmonic spectra. The steady voltage applied to the load was maintained, although the load varied a lot. The measured current and voltage harmonics were 13.22 % and 0.56 % respectively. Further, the SL-SCTBI is tested with variations in load from resistive to inductive. The voltage and current waveforms are presented in Figures 11 and 12, with plots of the FFT. The total harmonic distortions in the current and voltage readings taken through FFT graphs showed 13.22 % percent and 10.59 % respectively. Figure 13 shows the voltages on the capacitors VC1 and VC2.

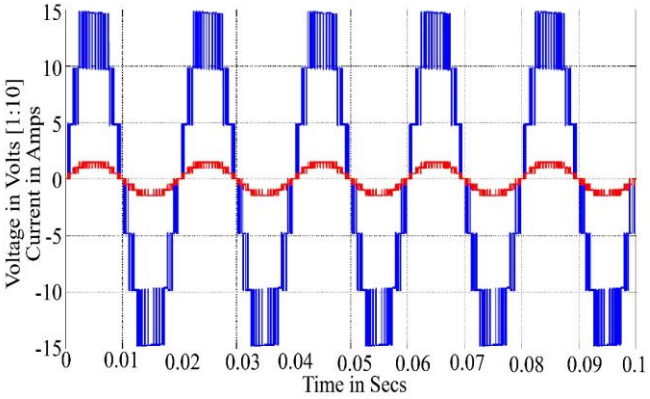

Fig. 5 Voltage and current of a simulated SL-SCTBI circuit under a resistive load

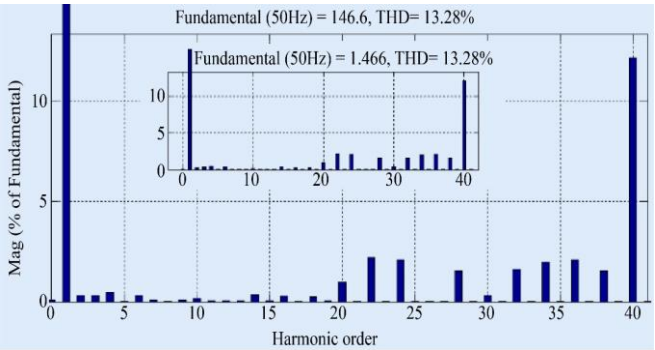

Fig. 6 spectra of voltage and current of SL-SCTBI

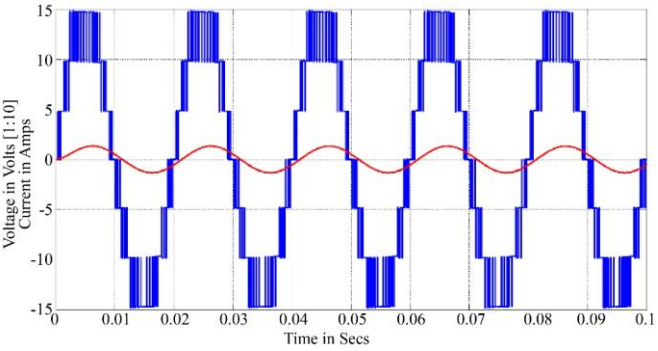

Fig. 7 Voltage and current of a simulated SL-SCTBI circuit under resistive-inductive load conditions (100 ohms-250 mH)

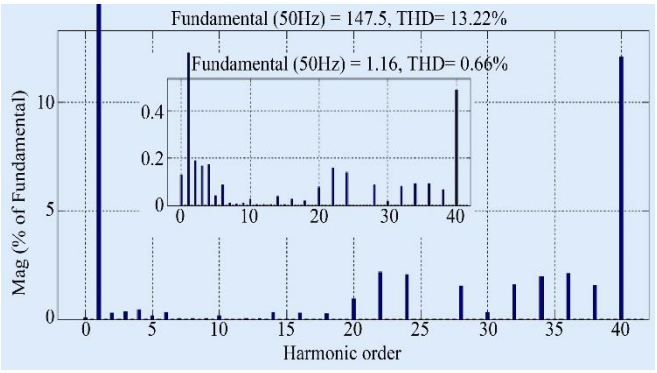

Fig. 8 Harmonic spectra of voltage and current of SL-SCTBI

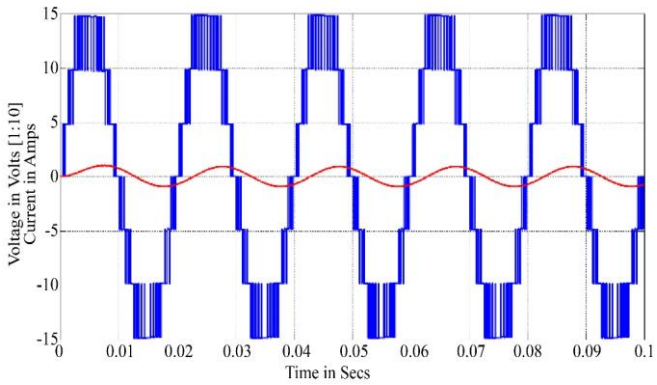

Fig. 9 Voltage and current of a simulated SL-SCTBI circuit under resistive-inductive load conditions (100 ohms-400 mH)

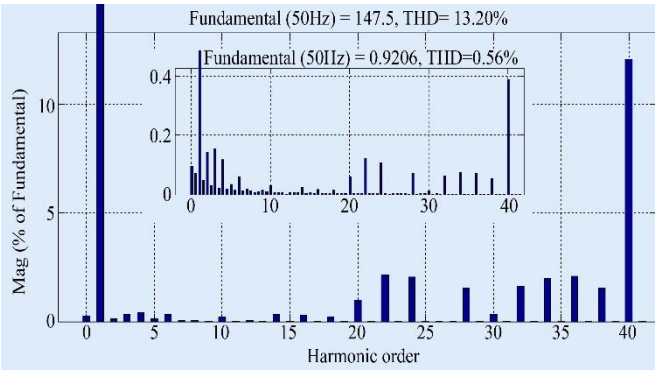

Fig. 10 Harmonic spectra of voltage and current of SL-SCTBI

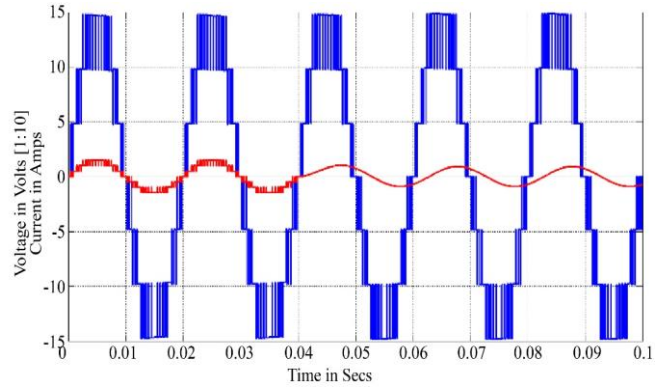

Fig. 11 Voltage and current of a simulated SL-SCTBI circuit R to RL

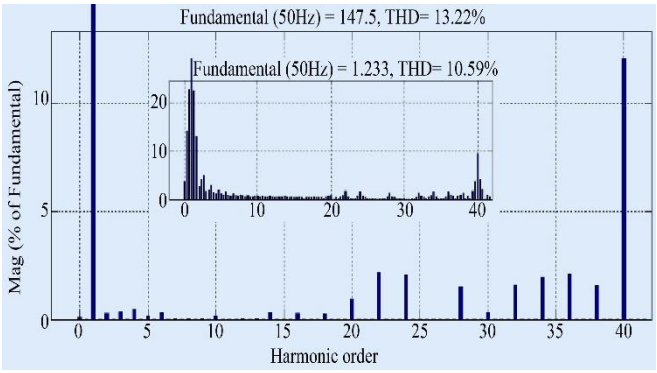

Fig. 12 Harmonic spectra of voltage and current of SL-SCTBI

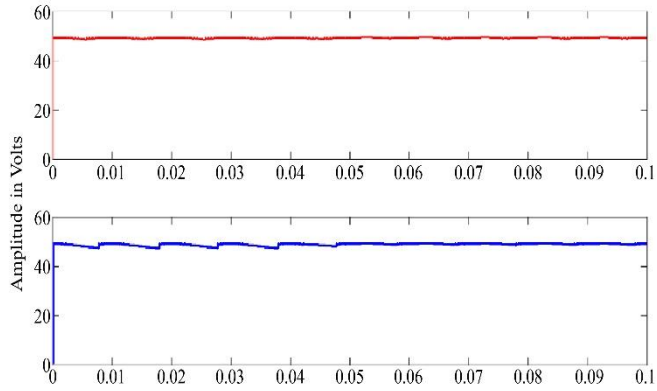

Fig. 13 Capacitor voltage of SL-SCTBI

4.2. Laboratory Testing Results

Test findings prove the practicality and efficiency improvement of the SL-SCTBI layout shown in Figure 14. Each FGA25N120 IGBT is being administered by SL-SCTBI that uses a TLP250 controller, whereas IGBT gate control signals are generated with a Spartan-3 FPGA. Figure 15 shows the spectral plots, and Figure 16 gives the results of the testing methods that compared the voltage and current effects of a resistive load (100 ohms).

The voltage and the current distortion are 15.58 %. Waveforms of voltage and current and harmonic spectra are depicted in the Figure 17 and 18, respectively, with an RL load measured current and voltage harmonics of 15.50 % and 1.10 %, respectively. The SL-SCTBI design is also performed using a resistive-inductive load of 100 ohms and 400 mH.—Figures 19 and 20 show voltage and current waveforms as well as the associated spectra. Load voltage was kept constant even when there was a significant variation in load. The harmonics of voltage and current measured were 15.50 and 1.02, respectively.

Also, the voltage and the current outputs during the change between a 100-ohm resistive load and a 100-ohm-400-mH inductive-resistor load are shown in Figures 21 and 22, respectively, along with FFT plots. The voltage and the current distortion were 15.50 and 13.10 percent, respectively.

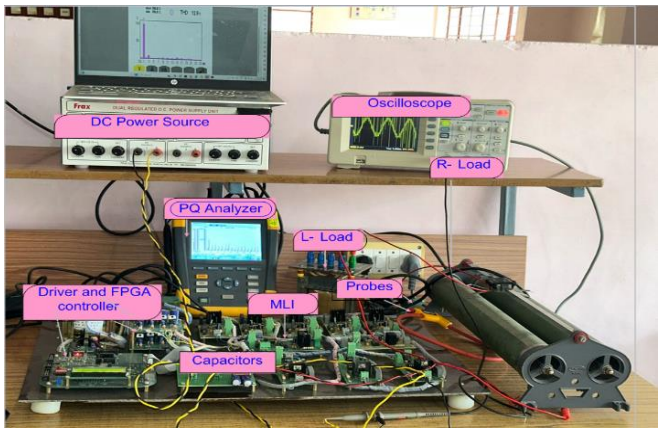

Fig. 14 Laboratory set up of SL-SCTBI

Table 3. Specifications

Components	Model
IGBT	FGA25N120
Control unit	FPGA
Input	V = 50V
Load	R - 100Ω, L - 250 mH

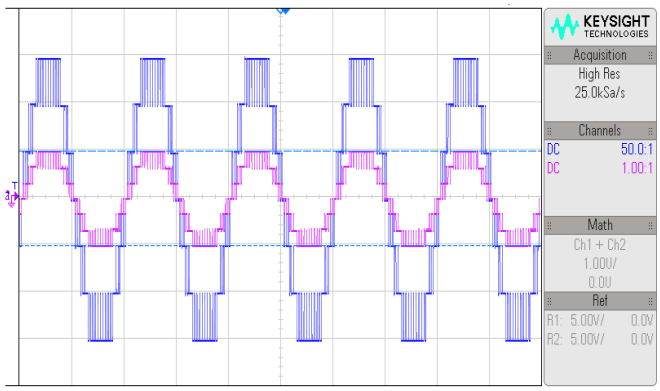

Fig. 15 Experimental data describing the voltage and current performance of the SL-SCTBI circuit when loaded with a resistive load

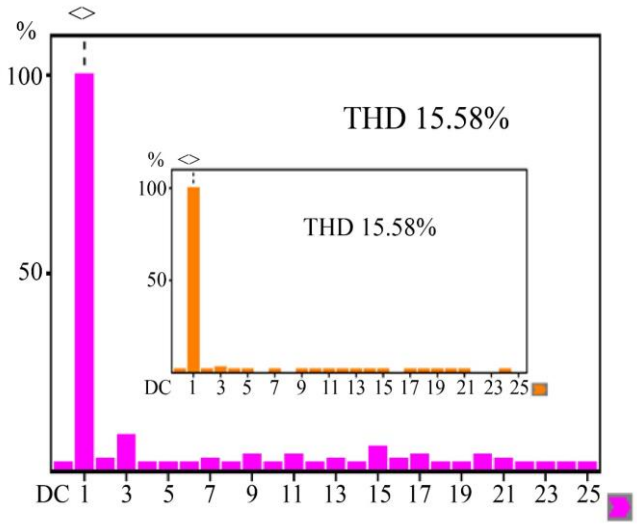

Fig. 16 SL-SCTBI harmonic spectra voltage and current

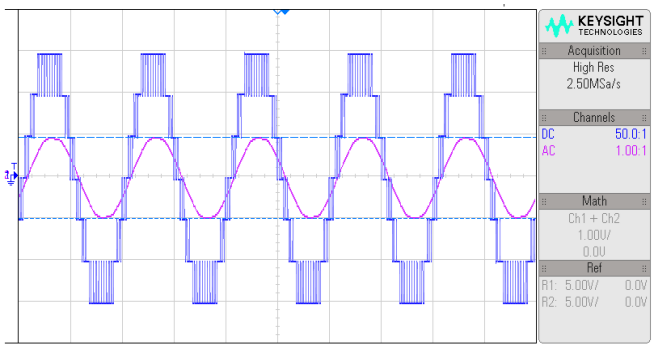

Fig. 17 Experimental data relating voltage and current of the SL-SCTBI ircuit to a resistive-inductive load condition (100 ohms-250 mH)

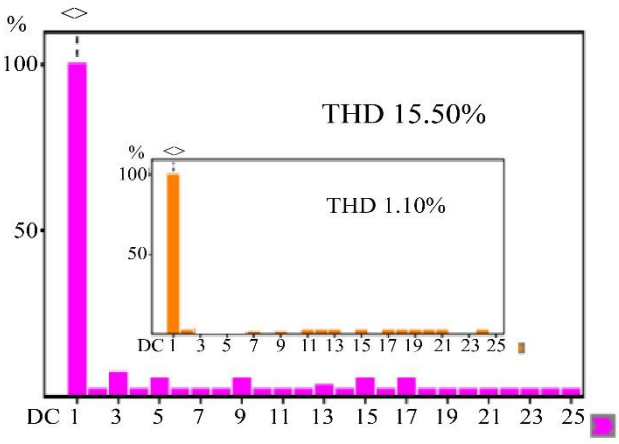

Fig. 18 SL-SCTBI harmonic spectra voltage and current

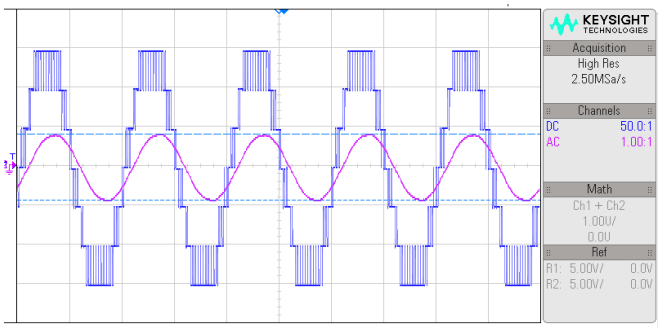

Fig. 19 Experimental data relating voltage and current of the SL-SCTBI circuit to a resistive-inductive load condition (100 ohms-400 mH)

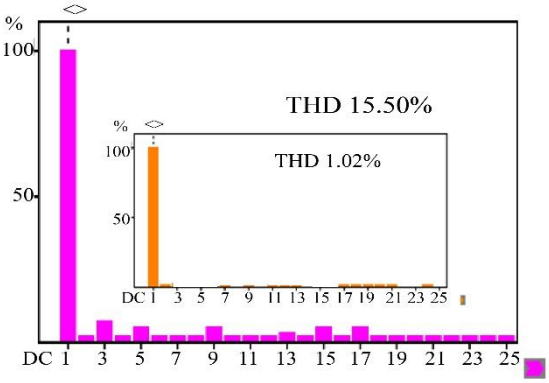

Fig. 20 SL-SCTBI harmonic spectra voltage and current

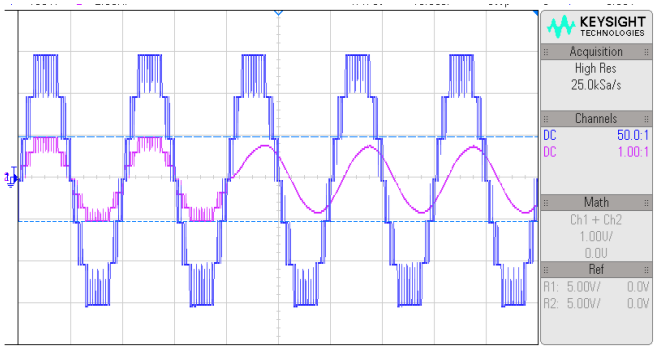

Fig. 21 Experimental data relating voltage and current of the SL-SCTBI circuit from R to RL

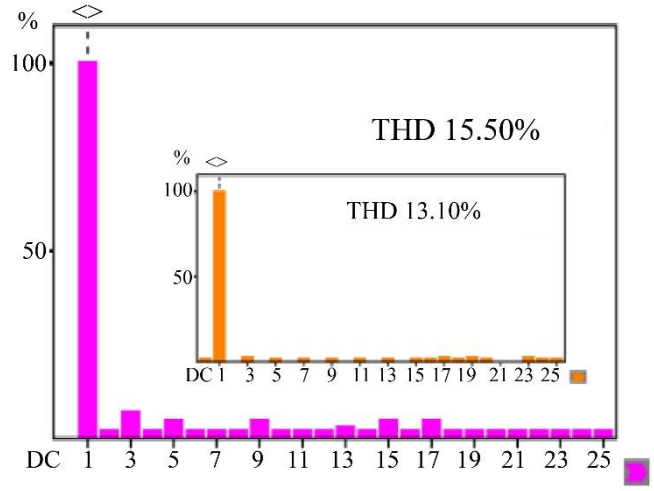

Fig. 22 SL-SCTBI harmonic spectra voltage and current

5. Conclusion

The Level Switched Capacitor Triple Boost Inverter (SL-SCTBI) can be said to represent a significant advancement in inverter technology. Here, it is shown that the SL-SCTBI can deliver voltage gain up to three times the input while generating seven distinct voltage levels with only eight switches, two diodes, and two capacitors. Numerous benefits are associated with this design. This reduces the overall system architecture, reduces manufacturing costs, and simplifies installation and maintenance. This design also addresses the voltage stability problem conventionally faced by traditional inverters by using self-balancing capacitors, which also improves operational reliability. As a result, the system does not require overly complex control mechanisms and represents higher efficiency in adapting to the changing load conditions.

In comparison to the currently available multilevel inverter designs, the SL-SCTBI is found to be superior to other existing designs. This study discusses the operational principles of the inverter, which shows the inverter's ability to handle the voltage stress of its components well and thus enhance reliability and the longevity of the inverter. Theoretically, it provides the benefit and lab tests and simulations corroborate these benefits. The results show that while the SL-SCTBI is well suited to existing applications, the design also has substantial potential to be extended for new inverter designs. Its capability to operate on a single DC power source that is simple to operate makes it a strong player in the renewable energy sector. Finally, the SL-SCTBI is a viable voltage-boosting solution for power electronics to not only increase energy conversion efficiency but also cut down costs and improve the reliability of energy conversion systems in the new energy realms. Future research could continue this line of work and explore the other optimizations, along with the integration of advanced control strategies to really exploit performance under all operational conditions.

Author Contribution

Author 1 contributed to the implementation and drafting of the article, and Author 2 contributed to the methodology and drafting of the article.

Reference

[1] Amal Mohan, and P. Jayaprakash, "An Improved Seven Level Multilevel Inverter for Grid Connected SPV Application," *2021 International Conference on Communication, Control and Information Sciences (ICCISc)*, Idukki, India, pp. 1-6, 2021. [CrossRef] [Google Scholar] [Publisher Link]

[2] Liangzong He et al., "Capacitor-Voltage Self-Balance Seven-Level Inverter with Unequal Amplitude Carrier-Based APODPWM," *IEEE Transactions on Power Electronics*, vol. 36, no. 12, pp. 14002-14013, 2021. [CrossRef] [Google Scholar] [Publisher Link]

[3] Aryorad Khodaparast et al., "Circuit Configuration and Modulation of a Seven-Level Switched-Capacitor Inverter," *IEEE Transactions on Power Electronics*, vol. 36, no. 6, pp. 7087-7096, 2021. [CrossRef] [Google Scholar] [Publisher Link]

[4] Yuanmao Ye et al., "Comparative Analysis of Hybrid NPP and NPC Seven-Level Inverter with Switched-Capacitor," *IEEE Access*, vol. 9, pp. 85852-85863, 2021. [CrossRef] [Google Scholar] [Publisher Link]

[5] Felipe Bovolini Grigoletto et al., "Step-Up Seven-Level Common-Ground Transformerless Inverter," *2021 14th IEEE International Conference on Industry Applications (INDUSCON)*, São Paulo, Brazil, pp. 716-722, 2021. [CrossRef] [Google Scholar] [Publisher Link]

[6] Pulavarthi Satya Venkata Kishore et al., "A New Reduced Switch Seven-Level Triple Boost Switched Capacitor Based Inverter," *IEEE Access*, vol. 10, pp. 73931-73944, 2022. [CrossRef] [Google Scholar] [Publisher Link]

[7] Md. Fazla Elahi, and Md. Aminul Islam, "A Triple Boost Self-Balanced Switch Capacitor Converter Based Multilevel Inverter," *2022 12th International Conference on Electrical and Computer Engineering (ICECE)*, Dhaka, Bangladesh, pp. 473-476, 2022. [CrossRef] [Google Scholar] [Publisher Link]

[8] Swati Halakarti, and Chandrasekhara Seregara, "Design and Simulation of Single Phase Seven-Level Boosting Multilevel Inverter with Self-Balancing Switched-Capacitor," *2022 IEEE North Karnataka Subsection Flagship International Conference (NKCon)*, Vijaypur, India, pp. 1-7, 2022. [CrossRef] [Google Scholar] [Publisher Link]

[9] Parth Patel et al., "Predictive Control of Seven Level Multi-Level Inverter Based Single Phase Shunt Active Filter," *2022 IEEE Industry Applications Society Annual Meeting (IAS)*, Detroit, MI, USA, pp. 1-6, 2022. [CrossRef] [Google Scholar] [Publisher Link]

[10] Narender Reddy Kedika et al., "Single-Phase Seven-Level Inverter with Multilevel Boost Converter for Solar Photovoltaic Systems," *2022 Second International Conference on Power, Control and Computing Technologies (ICPC2T)*, Raipur, India, pp. 1-6, 2022. [CrossRef] [Google Scholar] [Publisher Link]

[11] Patriot Sher Dash, and Shyama Prasad Das, "Switched-Capacitor Multi-Input Seven-Level Inverter for HFAC Applications," *2022 IEEE 2nd International Conference on Sustainable Energy and Future Electric Transportation (SeFeT)*, Hyderabad, India, pp. 1-5, 2022. [CrossRef] [Google Scholar] [Publisher Link]

[12] Ankur Srivastava, and Jeevanand Seshadrinath, "A Single-Phase Seven-Level Triple Boost Inverter for Grid-Connected Transformerless PV Applications," *IEEE Transactions on Industrial Electronics*, vol. 70, no. 9, pp. 9004-9015, 2023. [CrossRef] [Google Scholar] [Publisher Link]

[13] Mohammad Ali et al., "A Common-Ground Seven-Level Boosting Inverter (CG7LI) for Solar-PV Application," *2023 IEEE International Conference on Energy Technologies for Future Grids (ETFG)*, Wollongong, Australia, pp. 1-5, 2023. [CrossRef] [Google Scholar] [Publisher Link]

[14] Mokhtar Aly et al., "A Doubly Grounded Boost Seven Level PV Inverter Topology with Model Predictive Controller," *2023 IEEE 8th Southern Power Electronics Conference and 17th Brazilian Power Electronics Conference (SPEC/COBEP)*, Florianopolis, Brazil, pp. 1-6, 2023. [CrossRef] [Google Scholar] [Publisher Link]

[15] Milad Ghavipanjeh Marangalu et al., "A New High Step-Up NPC-Based Switched-Capacitor Seven-Level Grid-Tied Inverter for PV Applications," *2023 IEEE 64th International Scientific Conference on Power and Electrical Engineering of Riga Technical University (RTUCON)*, Riga, Latvia, pp. 1-6, 2023. [CrossRef] [Google Scholar] [Publisher Link]

[16] Naser Vosoughi Kurdkandi et al., "A New Seven-Level Transformer-Less Grid-Tied Inverter with Leakage Current Limitation and Voltage Boosting Feature," *IEEE Journal of Emerging and Selected Topics in Industrial Electronics*, vol. 4, no. 1, pp. 228-241, 2023. [CrossRef] [Google Scholar] [Publisher Link]

[17] Injila Sajid et al., "A Novel Seven-Level Switched Capacitor Multilevel Inverter Topology with Common Ground Configuration," *2023 International Conference on Power, Instrumentation, Energy and Control (PIECON)*, Aligarh, India, pp. 1-6, 2023. [CrossRef] [Google Scholar] [Publisher Link]

[18] Dai-Van Vo et al., "A Novel Single-Phase Seven-Level Boost Inverter with Simplified Control," *2023 IEEE International Conference on Energy Technologies for Future Grids (ETFG)*, Wollongong, Australia, pp. 1-6, 2023. [CrossRef] [Google Scholar] [Publisher Link]

[19] Swapan Kumar Baksi, and Ranjan Kumar Behera, "A Reduced Switch Count Seven-Level Boost ANPC Based Grid Following Inverter Topology with Photovoltaic Integration," *IEEE Transactions on Industry Applications*, vol. 59, no. 4, pp. 4238-4251, 2023. [CrossRef] [Google Scholar] [Publisher Link]

[20] Ronnan de Brito Cardoso et al., "A Seven-Level Inverter with Natural Balance and Boosting Capability," *2021 IEEE Energy Conversion Congress and Exposition (ECCE)*, Vancouver, BC, Canada, pp. 2495-2500, 2021. [CrossRef] [Google Scholar] [Publisher Link]

[21] Ronnan De B. Cardoso, Edison Roberto C. Da Silva, and Leonardo R. Limongi, "A Seven-Level Inverter with Reduced Component and DC-Link Voltage," *2023 IEEE Energy Conversion Congress and Exposition (ECCE)*, Nashville, TN, USA, pp. 3577-3583, 2023. [CrossRef] [Google Scholar] [Publisher Link]

[22] Pankaj Kumar Yadav, Hari Priya Vemuganti, and Monalisa Biswal, "A Seven-Level Switched Capacitor-Based RSC-MLI Topology with Suppressed Inrush Currents for Grid-Connected Applications," *2023 5th International Conference on Power, Control & Embedded Systems (ICPCES)*, Allahabad, India, pp. 1-6, 2023. [CrossRef] [Google Scholar] [Publisher Link]

[23] Lakshmi Prasanna, and T.R. Jyothsna, "A Switched Capacitor Seven-Level Inverter with Self Voltage Balancing Ability," *2023 IEEE International Conference on Power Electronics, Smart Grid, and Renewable Energy (PESGRE)*, Trivandrum, India, pp. 1-6, 2023. [CrossRef] [Google Scholar] [Publisher Link]

[24] Jaber Fallah Ardashir et al., "Dual Mode Seven-Level Transformer Less Grid-Tied Inverter with Common Ground Concept," *2023 IEEE Kansas Power and Energy Conference (KPEC)*, Manhattan, KS, USA, pp. 1-5, 2023. [CrossRef] [Google Scholar] [Publisher Link]

[25] G.G. Rajasekhar et al., "Seven Level Switched Capacitor Multilevel Boost Inverter for Renewable Energy Sources," *2023 International Conference on Advances in Electronics, Communication, Computing and Intelligent Information Systems (ICAECIS)*, Bangalore, India, pp. 643-646, 2023. [CrossRef] [Google Scholar] [Publisher Link]

[26] Ahmad Rafey Moonis et al., "Seven Level Single Source Switched-Capacitor Multilevel Inverter implemented with NLC and Level Shift PWM Technique," *2023 International Conference on Computer, Electronics & Electrical Engineering & their Applications (IC2E3)*, Srinagar Garhwal, India, pp. 1-6, 2023. [CrossRef] [Google Scholar] [Publisher Link]

[27] Sabari L. Uma Maheswari et al., "Space vector Pulse Width Modulation with 7 Level ANPC Converters for Capacitor Voltage Balancing," *2023 3rd International Conference on Innovative Practices in Technology and Management (ICIPTM)*, Uttar Pradesh, India, pp. 1-6, 2023. [CrossRef] [Google Scholar] [Publisher Link]

[28] Kaibalya Prasad Panda, Sumant Kumar Dalai, and Gayadhar Panda, "Step-up Switched-Capacitor Common-Grounded Seven-Level Inverter for Transformer Less PV System," *2023 IEEE International Conference on Power Electronics, Smart Grid and Renewable Energy (PESGRE)*, pp. 1-6, 2023. [CrossRef] [Google Scholar] [Publisher Link]

[29] Kaibalya Prasad Panda, Sumant Kumar Dalai, and Gayadhar Panda, "Switched-Capacitor Boost Common-Ground Six-Switch Seven-Level Inverter with Simplified Control," *2023 IEEE 3rd International Conference on Sustainable Energy and Future Electric Transportation (SEFET)*, Bhubaneswar, India, pp. 1-6, 2023. [CrossRef] [Google Scholar] [Publisher Link]

[30] Sangeeta Kumari, N. Sandeep, and Arun Kumar Verma, "T-Type Seven-Level Inverter with Triple Voltage-Boosting Gain," *IEEE Journal of Emerging and Selected Topics in Industrial Electronics*, vol. 4, no. 3, pp. 899-906, 2023. [CrossRef] [Google Scholar] [Publisher Link]

[31] V.S.K. Prasadarao, Sankar Peddapati and Balram Kumar, "A Voltage-Boosting Seven-Level Switched Capacitor Multilevel Inverter with Reduced Device Count," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 12, no. 1, pp. 743-753, 2024. [CrossRef] [Google Scholar] [Publisher Link]

[32] Milad Ghavipanjeh Marangalu et al., "A New High Step-Up SC-Based Grid-Tied Inverter with Limited Charging Spike for RES Applications," *IEEE Open Journal of Power Electronics*, vol. 5, pp. 295-310, 2024. [CrossRef] [Google Scholar] [Publisher Link]

[33] Vikram Singh, Anamika Yadav, and Shubhrata Gupta, "Effective Switch Fault Detection and Classification in Seven-Level Switched Capacitor Multilevel Inverter by Using Variable Mode Decomposition," *2024 4th Asian Conference on Innovation in Technology (ASIANCON)*, Pimari Chinchwad, India, pp. 1-6, 2024. [CrossRef] [Google Scholar] [Publisher Link]

[34] Anil Jakhar, N. Sandeep, and Arun Kumar Verma, "Seven-Level Common-Ground-Type Inverter with Reduced Voltage Stress," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 12, no. 2, pp. 2108-2115, 2024. [CrossRef] [Google Scholar] [Publisher Link]

[35] Atif Iqbal et al., "Single-Phase Dual Ground 7L Inverter Topology with Reduced Component Count and Stress," *2024 IEEE 4th International Conference on Sustainable Energy and Future Electric Transportation (SEFET)*, Hyderabad, India, pp. 1-6, 2024. [CrossRef] [Google Scholar] [Publisher Link]

[36] Weijie Lin et al., "Switched-capacitor Based Seven-level Boost Inverter with a Reduced Number of Devices," *CSEE Journal of Power and Energy Systems*, vol. 10, no. 1, pp. 381-391, 2024. [CrossRef] [Google Scholar] [Publisher Link]

[37] Sangeeta Kumari, and N. Sandeep, "Switched-Capacitor-Based Seven-Level Inverter with Reduced Component Count and Current Stress," *IEEE Journal of Emerging and Selected Topics in Industrial Electronics*, vol. 5, no. 1, pp. 2-7, 2024. [CrossRef] [Google Scholar] [Publisher Link]

[38] Javad Ebrahimi et al., "A Single-Phase Seven-Level Nested Switched-Capacitor Converter with Enhancing Lifetime and Reducing Size of Flying Capacitors," *IEEE Transactions on Power Electronics*, vol. 40, no. 7, pp. 9234-9248, 2025. [CrossRef] [Google Scholar] [Publisher Link]

[39] Mingzhe Wu et al., "Topology and Control of Seven-Level Tree-Type Active Neutral-Point-Clamped Converters," *IEEE Transactions on Industrial Electronics*, vol. 72, no. 4, pp. 3257-3268, 2025. [CrossRef] [Google Scholar] [Publisher Link]