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Original Article

A New Transformer-Less Quasi-Switched Converter with Continuous Load Current for Electric Vehicle Applications Using Robust Controller Approach

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Abstract *- This article introduces a transformer-less modified quasi-switched non-isolated converter designed for electric vehicle charging applications. The primary feature of this quasi-arrangement is its ability to maintain continuous load current with low-order ripples and better voltage regulation while operating within a nominal duty cycle range. In existing configurations, many voltage multiplier cells or converters are employed to attain higher efficiency, but this leads to increased switching and conduction losses. To overcome these issues, the proposed topology uses fewer components, which improves efficiency by approximately 96.2% and results in a reduction in losses. The converter is controlled with a robust Model Predictive Control (MPC), which results in better output response, a peak overshoot at 0.3%, and faster settling times. Additionally, the operating principle, theoretical, and steady-state analysis, and comparisons to existing topologies are included. A 200W hardware prototype will be designed, built, and tested to evaluate the system's performance and validate the experimental results.*

Keywords *- Battery, Electric vehicle, Model predictive control, Non-isolated, PV system.*

1. Introduction

In recent years, the sustainable development and utilization of various renewable energy sources, such as wind, PV modules, and fuel cells, have received broad global attention to promote a green, sustainable environment and reduce fossil fuel consumption. Recent breakthroughs and research developments in DC-DC converters using renewable sources aim to achieve high power density, improved efficiency, and better voltage conversion ratios.

Researchers mainly focus on high-gain DC-DC converter topologies, such as non-isolated and isolated, unidirectional and bidirectional, single-stage or multi-stage power converters, utilizing advanced controllers to maximize power extraction from renewable energy systems. Among these, multiport converter topologies are generally preferred in series-connected PV systems to harness sufficient power when integrated with various renewables, as outlined in the literature [1-3]. This study [4] employs a coupled inductor and voltage-doubler rectifier circuit to achieve higher gain without requiring an extreme duty cycle range. A new ultra-voltage gain converter using a single switch providing fewer ripples in output voltage and current is approached, making it suitable for high-power applications [5]. This converter attains superior step-up or step-down capability under steady-state conditions, where the duty cycle is either higher or lower than 50% [6]. Here, a voltage-doubler circuit integrated with a quadratic boost converter is introduced for LED driver applications by increasing the duty ratio of the single switch [7]. Due to the advantages of continuous input current, non-inverted output voltage, and improved efficiency, a Voltage Multiplier (VM) cascaded boost structure is employed [8]. An arrangement to reduce the number of passive components and achieve higher gain is presented by analyzing the converter's performance under steady-state conditions [9]. By combining a two-inductor boost structure with multiple VM cells, a hybrid transformer-less structure is developed [10]. This study proposes a non-isolated single-switch converter for renewable energy conversion, providing significantly higher gain with better efficiency [11]. But, bi-directional power flow utilizes either non-isolated or isolated converters to reduce ripples, modify voltage conversion ratios, and improve efficiency, resulting in increased control complexity [12]. Therefore, interleaving techniques and synchronous rectification methods are employed to eliminate current ripples at the battery side and enhance efficiency [13]. Figure 1 shows a schematic diagram for single-stage power conversion in DC-DC converters. But, in most cases, the quadratic type is recommended for a wide voltage conversion ratio and reduced stresses across the power switch [14].

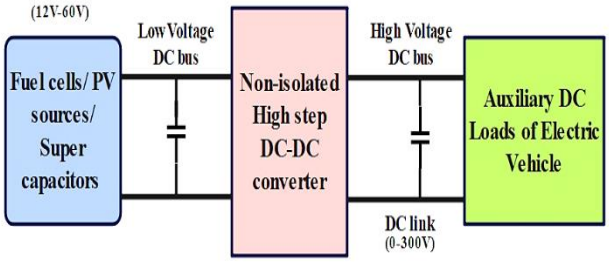


Fig. 1 Schematic representation of single-stage power conversion

By using a simple PWM method and a split-capacitor structure, extended ZVS can be obtained in converters [15]. This study suggests a quadratic converter employing two switched VM cells to achieve continuous source current and wide voltage gain [16]. A CI-combined VM circuit is investigated in [17] to mitigate higher voltage stress and improve gains. To accomplish soft-switching conditions, an isolated transformer with a reduced turns ratio is employed in the proposed converter [18]. Coupled inductors with two switched capacitors are proposed for achieving a high voltage conversion ratio, but are not able to suppress voltage spikes across the power switch [19, 20]. Based on the literature reviewed, the topologies mentioned above utilize transformers or voltage multiplier cells, which increase component count, power loss, complexity, and system cost. This article offers a revolutionary non-isolated quasi-switched converter with a single power switch at low cost to overcome the limitations of previous topologies regarding component count, power loss, steady-state responsiveness, and peak overshoot.

The essential aspects of the proposed system, represented in Figure 2, are as follows,

- Reduced ripple at the load side to ensure continuous load current.
- Improved power density and efficiency.
- Transformer-less structure simplifies control operation at low cost.
- The suggested MPC control improves dynamic response, reduces peak overshoot, and enables faster settling time.

This article is divided into the sections below. Section II discusses the operating principles and modes of operation. Section III addresses stress analysis and component selection. Section IV discusses the proposed converter control scheme and its performance comparison. Section V displays the results of MATLAB simulations. Section VI represents the experimental results. The article concludes with Section VII.

2. Operating Principle and Modes of the Proposed Configuration

This section describes the converter operating under CCM circumstances. Figure 2 depicts the proposed topology, which includes a single power switch (Q), three diodes (D_1, D_2, and Do), two inductors (L_1 *and* L_2), three capacitors (C_1, C_2, and C_3), a PV source, and a battery load. The converter has two modes, as shown in Figures 3 and 4. Figure 5 illustrates the system's key waveform during CCM.

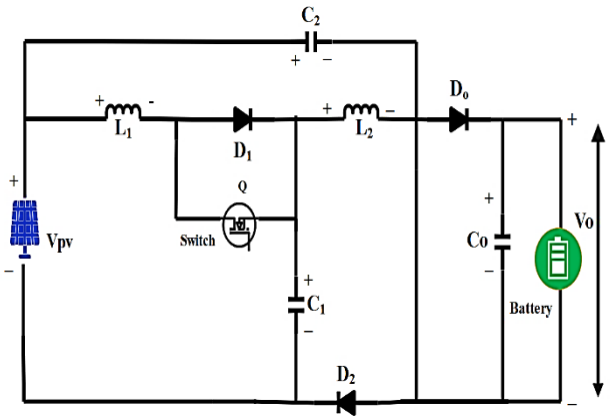


Fig. 2 Structure of the proposed system

2.1. Modes of Operation

2.1.1. Mode 1: Switch (Q) On (T_o<DT_s<T_1)

When the power switch Q is turned ON during the time interval (T_0-T_1), D_o is forward biased, and diodes D_1 and D_2 remain in reverse blocking mode. Figure 3 illustrates the mode 1 operation.

The input PV source supplies the current to inductor L_1. The capacitor C_1 charges at the same time via the PV source. Here, the source (V_{PV} or V_S) is parallel with the switch Q. The inductor L_2 charges using the V_{PV} and V_Q combination.

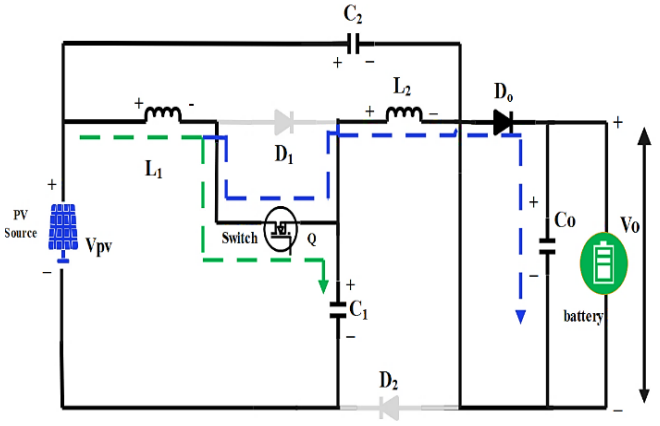


Fig. 3 Mode 1 operation

The voltages across inductors and capacitors can be described using Kirchhoff's Voltage Law (KVL). Hence,

$$V_{Co} = V_o, V_{L1} = V_{PV} = V_Q \quad (1)$$

$$V_{L2} = V_{C2} = \frac{V_{PV}}{1-D} + V_o \quad (2)$$

2.1.2. Mode 2: Switch (Q) Off (T_1<DT_s<T_2)

During this stage, Q is turned off (T_1-T_2), and the inductors L_1 and L_2 discharge their stored energy to the load side through capacitors. L_1 charges C_1, and L_2 discharges to C_2. Finally, the output capacitor delivers its total energy to the load. The mode 2 operation is depicted in Figure 4. In the operating key waveform, D represents the duty cycle, and T is the total switching period.

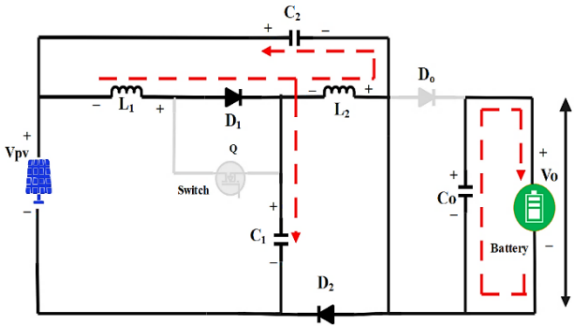


Fig. 4 Mode 2 operation

Using KVL, the expression for the voltages of the semiconductor elements is represented as,

$$V_{L1} = V_{C1} = \frac{DV_{PV}}{1-D} \tag{3}$$

$$V_{L2} = \frac{2V_{PV}}{1-D} - V_o \tag{4}$$

$$V_{C2} = \frac{V_{PV}}{1-D} \tag{5}$$

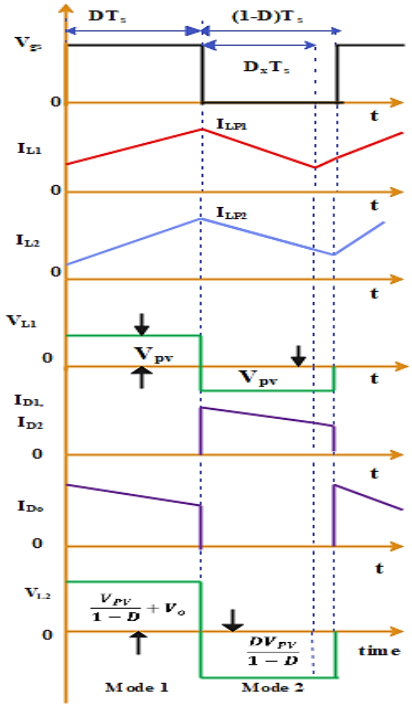


Fig. 5 Operating keywaveform

To examine the steady-state circumstances, apply the inductor volt-sec balance principle during one complete cycle, T_s. The average voltage across L is expressed as,

$$\int_0^{DTs} V_L dt + \int_{(1-D)Ts}^{Ts} V_L dt = 0$$

$$\left(\frac{V_{PV}}{(1-D)} + V_o\right) D + \left(\left(\frac{2V_{PV}D}{(1-D)}\right) - V_o\right)(1-D) = 0 \tag{6}$$

$$\frac{V_{PV}}{(1-D)} D + V_o D + \left(\frac{2V_{PV}D}{(1-D)}\right) - V_o - \frac{2V_{PV}D}{(1-D)} + V_o D = 0 \tag{7}$$

$$\frac{V_{PV}}{(1-D)} D + 2V_o D - V_o = 0 \tag{8}$$

$$\frac{DV_{PV}}{(1-D)} = V_o(1+2D) \tag{9}$$

As a result, the converter gain may be calculated as the ratio of steady-state output voltage to input voltage.,

$$\frac{V_o}{V_{in}} = \frac{D}{(1+2D)(1-D)} \tag{10}$$

3. Stress Analysis and Design Guidelines

3.1. Stress Analysis

3.1.1. Voltage Stress on the Switch and Diodes

In the Off state, the voltage stress across the power switch V_Q and the voltage stress on diodes D_1, D_2, and D_o can be expressed as,

$$\begin{cases} V_Q = V_{Switch} = V_{C1} = V_{C2} = \frac{DV_{pv}}{(1+2D)(1-D)} \\ V_{Co} = \frac{(1-D)V_{pv}}{(1+2D)(1-D)} \end{cases} \tag{11}$$

$$\begin{cases} V_{D1} = V_{D2} = \frac{V_{pv}}{(1+2D)(1-D)} \\ V_{Do} = \frac{(1-D)V_{pv}}{(1+2D)(1-D)} \end{cases}$$

3.1.2. Current Stress on the Switch and Diodes

In mode 1, the diode D_o remains forward-biased while D_1 and D_2 remain in reverse. So, the present stress during the On state is expressed as:

$$i_{s1} = i_{L1} = i_{L2} = \frac{DI_o}{(1+2D)(1-D)} \tag{12}$$

Hence, the average current on the diodes is,

$$\begin{cases} I_{D1} = \frac{I_o}{(1+2D)(1-D)} \\ I_{D2} = DI_o \\ I_{Do} = I_o \end{cases}$$

3.2. Design Guidelines

3.2.1. Inductor Selection

By utilizing the volt-sec balancing concept, during the On state, the inductances are designed by calculating the current ripple as 20% at 50 kHz, provided by the following equation,

$$\begin{cases} L_1 = L_2 = \frac{V_S D}{\Delta i_L f_s} \\ \Delta i_L = \Delta i_{L1} = \Delta i_{L2} = \frac{DV_S}{f_S L} \end{cases}$$

The variables f_s, ΔiL, D, and V_s represent the switching frequency, ripple in inductor current, duty cycle, and input voltage, respectively.

3.2.2. Capacitor Selection

Using the charge-sec balance principle, capacitance values are calculated using a 10% capacitor voltage ripple (ΔVc).

$$\begin{cases} \Delta V_{c1} = \frac{DI_o}{f_S C_1 (1-D)}, \quad I_o = \frac{V_o}{R_L} \\ \Delta V_{c2} = \frac{D^2 I_o}{(1-D) f_S C_1} \\ \Delta V_{co} = \frac{V_S . D^2}{8(1-D) f_S^2 C_o L_2} \end{cases}$$

3.2.3. Selection of Power Switch

Switch voltage is an important metric in estimating the efficiency and cost of a high-gain converter. The switching voltage is less than the load voltage but equal to the capacitor voltage.

$$V_Q = \frac{V_S}{1-D} \tag{3}$$

4. Control Algorithm and Performance Comparison Investigations with Existing Configurations

4.1. Control Strategy

Figure 6 depicts a robust, optimized, advanced control strategy, the Model Predictive Controller (MPC), incorporated in the proposed configuration to predict the system's future behavior by achieving better output response, reduced peak overshoot, and fast settling time over a predetermined time horizon. A control signal is generated between the reference signal and the output voltage at each sampling point. The duty cycle is calculated by predicting the future outputs for y(K+1) for K=1 to N at each moment.

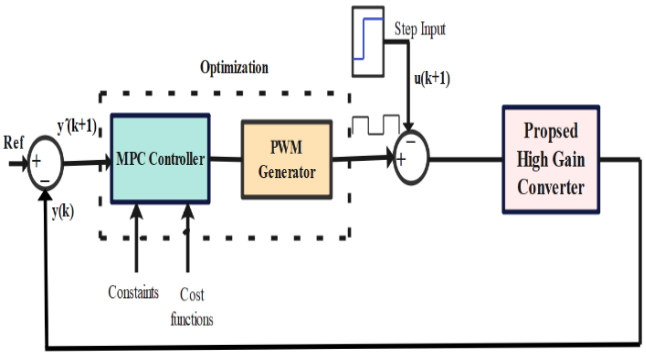


Fig. 6 Proposed control algorithm

The goal of MPC is to make the prediction time longer than the sampling period and assess the transient features to reduce the system's dynamic response. The controller is constructed with two states, one input, and a control horizon of 2. The controller optimizes the system to minimize the steady-state error using a ten-step projected horizon. The controller is optimized by setting the cost functions and restrictions, and applying initial conditions to generate input and output responses. The controller computes the step response for a linear time-varying system, as shown in Figure 7. In dynamic and closed-loop systems, the voltage-to-duty cycle range transfer function is expressed by the following equation,

$$G_{Vd}(s) = K \frac{a_2 s^2 + a_1 s^1 + a_o}{b_2 s^2 + b_1 s^1 + b_o} \tag{14}$$

Figures 8 and 9 show the generation of input and output responses against the internal response, as well as switching pulse generation at a duty range of 0.7.

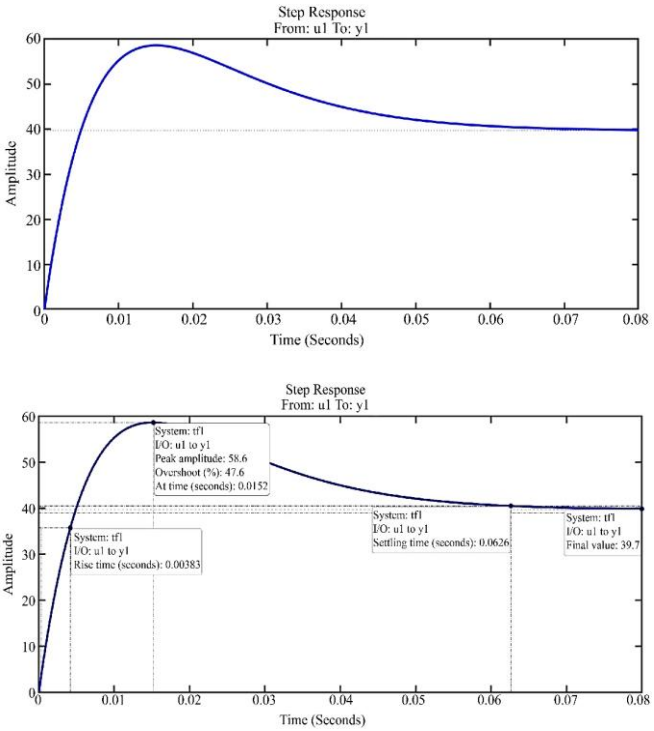
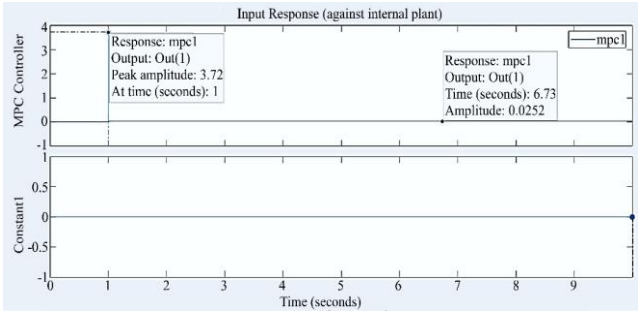


Fig. 7 Controller step response



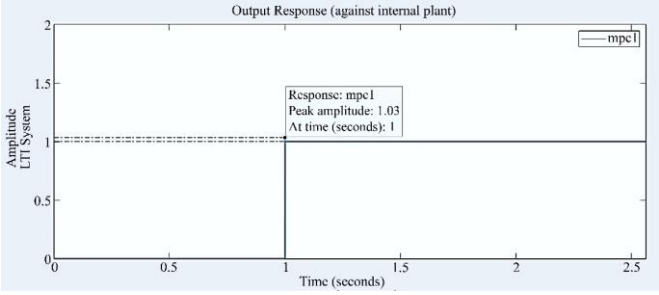


Fig. 8 Generated input and output responses of the controller

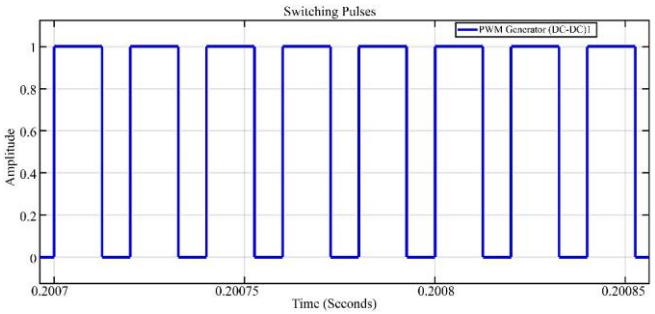


Fig. 9 Switching pulse generation at 0.7 duty range

4.2. Performance Comparison

Several topologies use switched inductor (SL) approaches to enhance voltage conversion ratio, high power density, and efficiency in existing topologies, including cascaded VM cells and hybrid switched capacitor (SC). Compared with existing topologies referenced in [12, 13, 15], the proposed architecture employs a single power switch and fewer power components to improve efficiency. Table 1 Presents the simulation parameters and specifications of the PV module, and Figure 10 depicts the PV system's performance curves. Table 2 compares the proposed configuration with recently reported topologies. Among various structures, the proposed topology achieved a peak efficiency of approximately 96.2% and improved voltage regulation with reduced losses.

Table 1. Simulation parameters and specifications of the solar PV array

Parameters	Values
Input Voltage (PV Port- V_{in})	20 V
Output Load Voltage	52 V
Duty Cycle	0.5~0.6
Switching Frequency	50 kHz
Inductors (L_1,L_2)	5.25mH
Capacitors(C_1,C_2,C_o)	175µF,1000 µF
Load Resistance	1kΩ
Parameters	**Specifications**
Maximum Peak Voltage (V_{mp})	30V
Maximum Peak Current (I_{mp})	7.7A
Maximum Power (P_{max})	220W
Short Circuit Current (I_{sc})	8.3A
Open Circuit Voltage (V_{oc})	38V

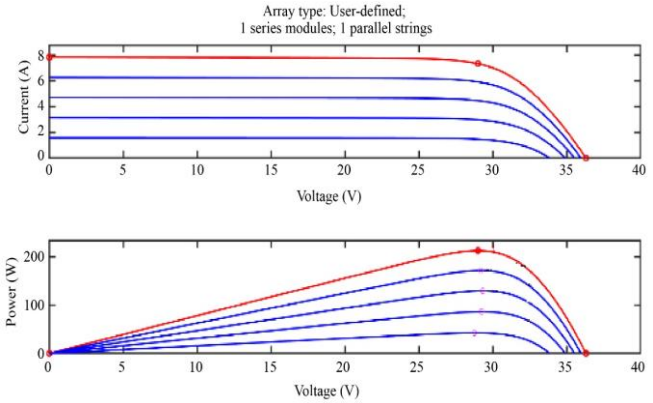


Fig. 10 VI & PV curves of the solar PV array at various irradiances

5. Simulation Results and Calculation of Power Loss Analysis

5.1. Simulation Results of the Proposed System

The proposed QS-SL converter's simulation results are executed using the MATLAB Simulink Toolbox.

The system delivers output power at 50W with ripple-free continuous load current, as illustrated in Figures 11 and 12.

Due to the constant or variable load, the output voltage is constantly kept at roughly 19.8V, with a decreased overshoot at a 0.7 duty range.

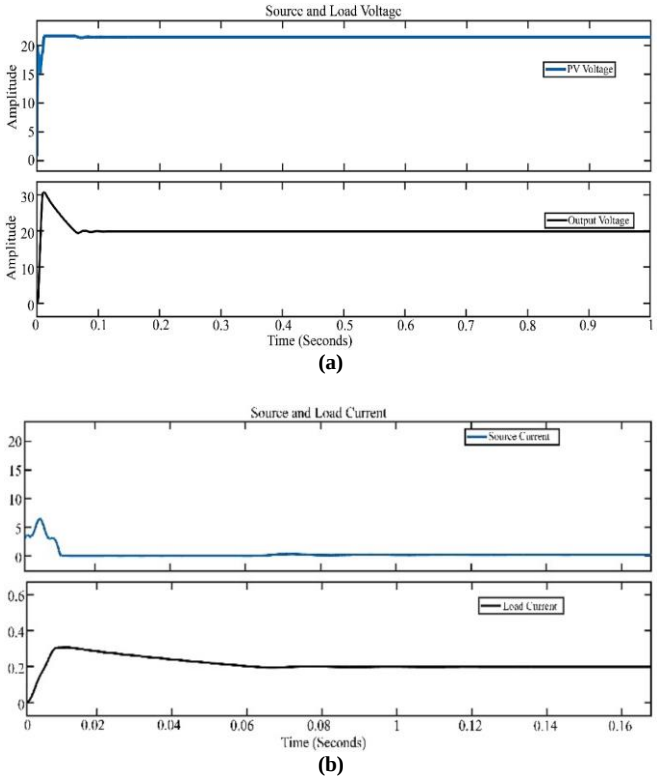


Fig. 11 Simulation results, (a) Source and load voltage, and (b) Source and load current.

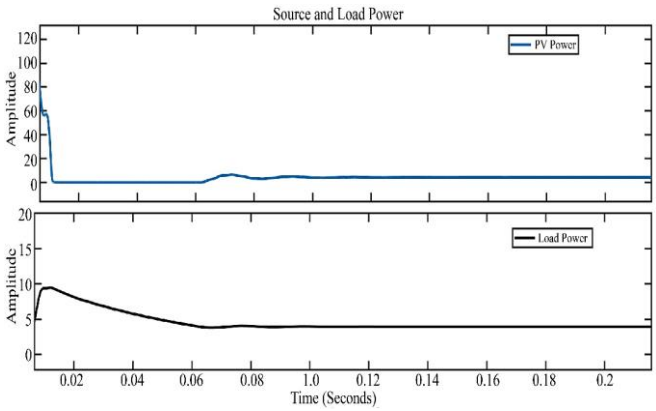


Fig. 12 Simulation result of source and load power

5.2. Power Loss Calculation

The proposed converter power loss can be calculated to estimate the efficiency. During the switch 'Q' On period, both switching and conduction losses are expressed by the following equation:

$$\begin{cases} P_{Q(cond)} = I_{Q(rms)}^2 r_s \\ P_{Q(switch)} = \frac{P_Q T_{(On+Off)} f_s}{2} \\ P_{Q(Total)} = P_{Q(cond)} + P_{Q(switch)} \end{cases}$$

The diode power loss is calculated by the following expression,

$$\begin{cases} P_{D(r_d)} = [I_{D1(rms)}^2 + I_{D2(rms)}^2 + I_{Do(rms)}^2] r_d \\ P_{D(V_f)} = [I_{D1(avg)}^2 + I_{D2(avg)}^2 + I_{Do(avg)}^2] v_f \\ P_{D(Total)} = P_{D(r_d)} + P_{D(V_f)} \end{cases}$$

Also, the capacitors and inductor losses are expressed as,

$$P_L = I_{Lrms)}^2 r_L$$

$$P_{C(Total)} = I_{C(Total(rms))}^2 r_C$$

Therefore, the total power loss can be calculated as,

$$P_{(Total-loss)} = P_{Q(Total)} + P_{D(Total)} + P_L + P_{C(Total)}$$

Finally, the system efficiency can be evaluated by,

$$\eta\% = \frac{P_{out}}{P_{out} + P_{Loss(Total)}}\% = 96.2\%$$

6. Experimental Study

To verify the simulation studies and steady-state analysis, a hardware prototype of 200W was designed and built in the laboratory for the proposed topology, as shown in Figure 13. The power switch used is MOSFET IRF630 (V_{DS}=600V, $R_{DS(on)}$=0.40Ω), and the diodes are IN4007. The MOSFET switch is driven by a TLP250 driver circuit. Figure 14. depicts the measured experimental results of the proposed converter where V_{PV}=25V and D=0.5, respectively. The waveforms of the inductor currents (I_{L1} and I_{L2}) and the output voltage V_o are also represented. It is observed that the input current remains in continuous conduction during the switch 'Q' On position. The measured output voltage, V_o, is observed at 50V, which is slightly less than the calculated value. The experimental parameters are presented in Table 3. The measured capacitor voltages and currents are shown in the Figures. 15 and 16. It can be observed that the voltages increase to 30V and 50V, respectively. Similarly, during the switch-on position, D_1 and D_2 remain reverse-blocking, so the voltage stresses across the diodes are lower than the output voltage. The observed waveforms are depicted in Figure 17. During the OFF position, the measured switching voltage stress is significantly lower than the previous voltage ratings, resulting in reduced loss and cost for the converter. The theoretical and experimental output gain of the proposed configuration is plotted and compared in Figure 18. It can be noted that the practical values are consistently lower than the theoretical values due to the absence of parasitic components. The experimental measured efficiency of the proposed system in CCM mode for the various power ranges is plotted in Figure 19. It is proven that, due to the variation in input voltages, the efficiency can be observed at a maximum of 96.2% with reduced conduction loss at a 0.5 duty cycle. The detailed power loss analysis has been depicted in Figure 20 under the rated operating conditions.

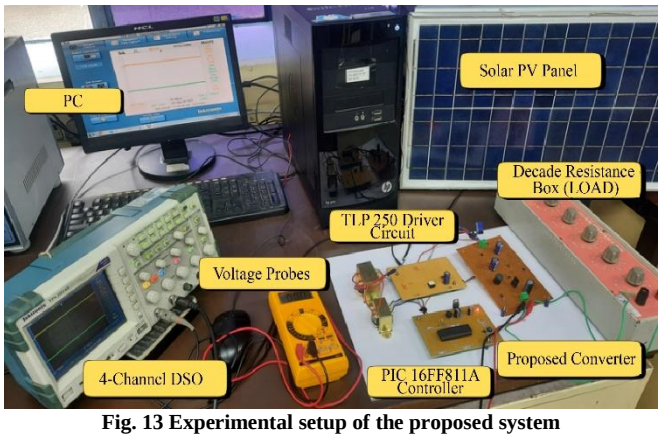


Fig. 13 Experimental setup of the proposed system

Table 2. Performance comparison with existing configurations

Topologies	Switch	D	C	L	Switching Frequency	Voltage Gain ($\frac{V_o}{V_{in}}$)	Input Current	Efficiency (%)	Output Power
Ref [5]	1	4	3	2	100kHz	$\frac{2-D}{(1-D)^2}$	Pulsating	91.2%	500W

Ref [6]	1	2	2	3	50kHz	$(\frac{D}{D_1})^2$	Non-pulsating	95.9%	100W
Ref [7]	1	5	4	2	40kHz	$\frac{1+n}{(1-D)^2}$	Pulsating	92%	200W
Ref [9]	2	4	3	2	50kHz	$\frac{3-D}{1-3D}$	Pulsating	93.2%	200W
Ref [11]	3	2	1	2	50kHz	$\frac{1+D_1}{1-D_1-D_2}$	Non-pulsating	93.6%	200W
Ref [14]	1	3	3	2	60kHz	$\frac{3+D}{2(1-D)}$	Pulsating	92.2%	250W
Proposed Topology	**1**	**3**	**3**	**2**	**50kHz**	$\frac{D}{(1+2D)(1-D)}$	**Non-pulsating**	**96.2%**	**200W**

Table 3. Experimental parameters

Components	Parameter Values
PV Panel	Loom solar, 40V, 3.5 A
Output Power (P_{max})	200 W
Input Voltage (V_{in})	20 V
Output Voltage (V_{out})	50 V
Switching Frequency (f_{sw})	50 kHz
Power MOSFET (Q) Switch	IRF630
Driver Board	TLP250
Microcontroller	PIC 16FF811A IC
Diodes (D_1, D_2, and D_o)	IN4007
Inductor (L)	8mH
Capacitors (C_1 and C_2)	150 µF, 64 V,1000 µF
Output capacitor (C_o)	1000 µF
Battery	12.6V,1.5A
Load resistor	1 kΩ, 10 kΩ,

The dynamic response performance analysis can also be performed under variations in input voltage and step load changes, respectively. The experimental waveform demonstrates that the output voltage remains stable due to the step load change, shown in Figures 21 and 22.

However, the dynamic analysis also proves for variation in input voltage from 25V to 35V, maintaining the regulated output voltage at 50V. Therefore, the proposed topology shows better performance in both theoretical and experimental results.

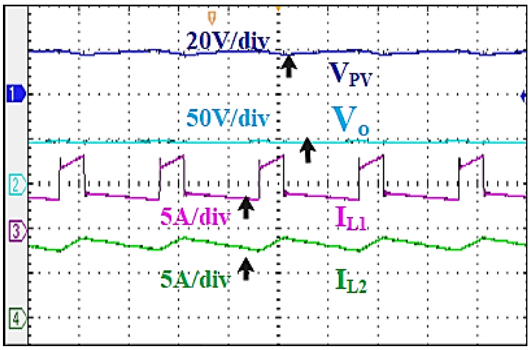


Fig. 14 Simulation result of input, output voltages and inductor currents

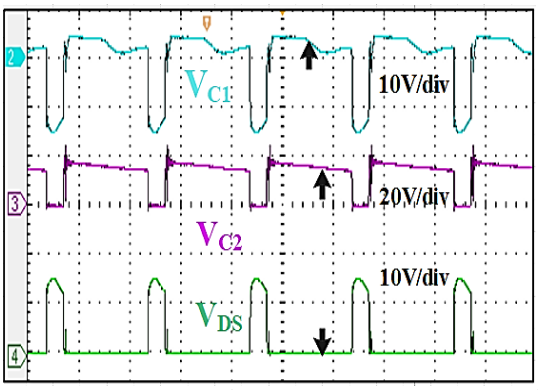


Fig. 15 Simulation result of capacitor voltages and V_{DS} waveform

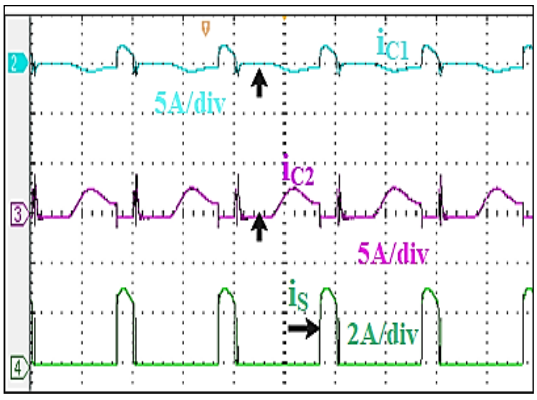


Fig. 16 Simulation waveform of capacitor currents and i_S

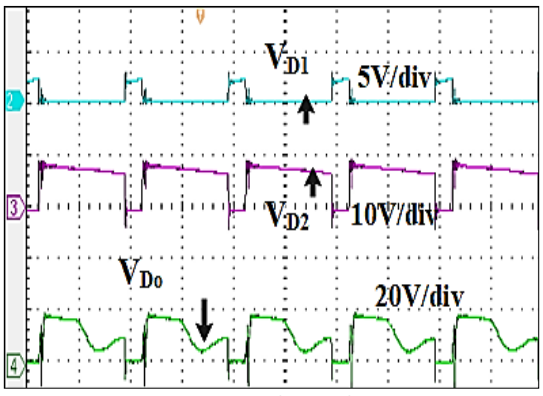


Fig. 17 Measured waveforms of V_{D1}, V_{D2} and V_{Do}

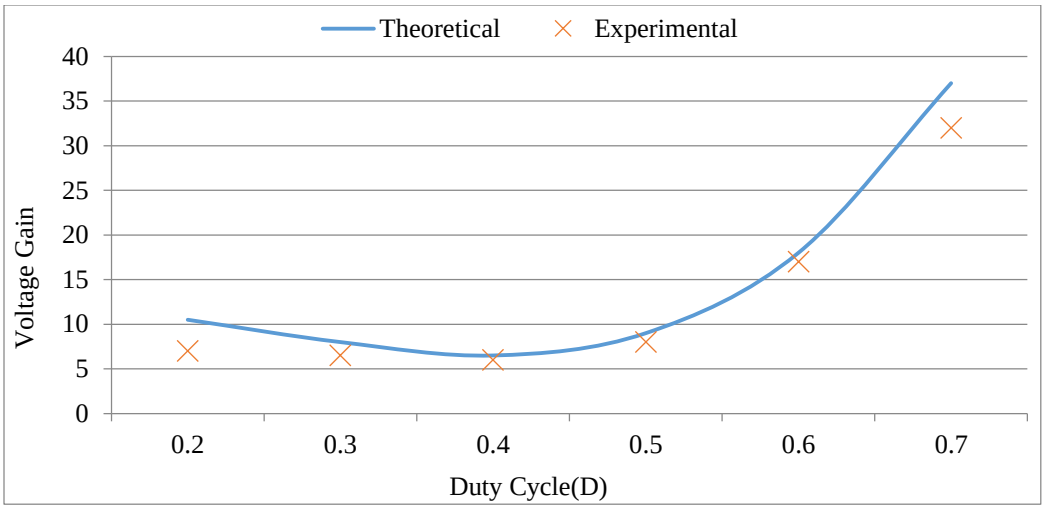


Fig. 18 Theoretical and experimental comparison

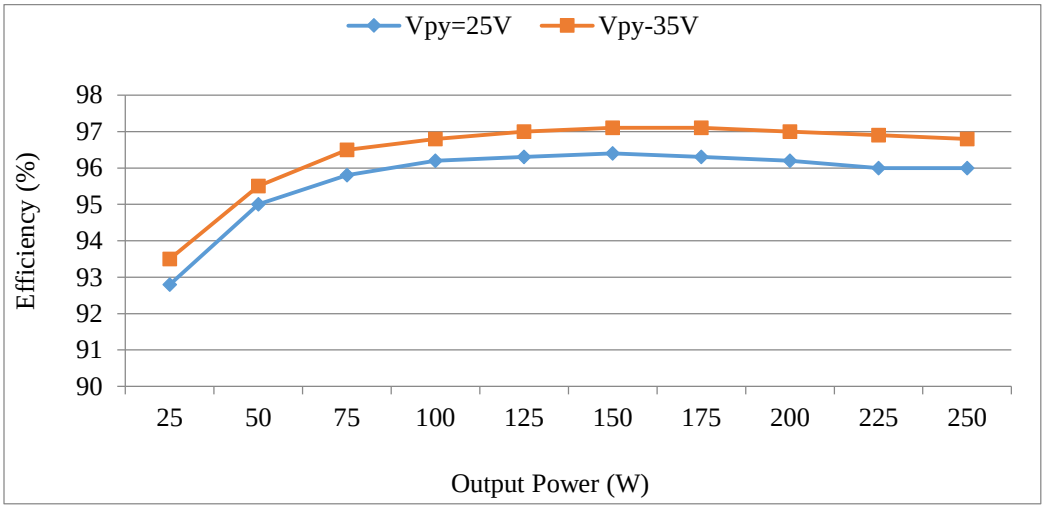


Fig. 19 Performance curve of the proposed system

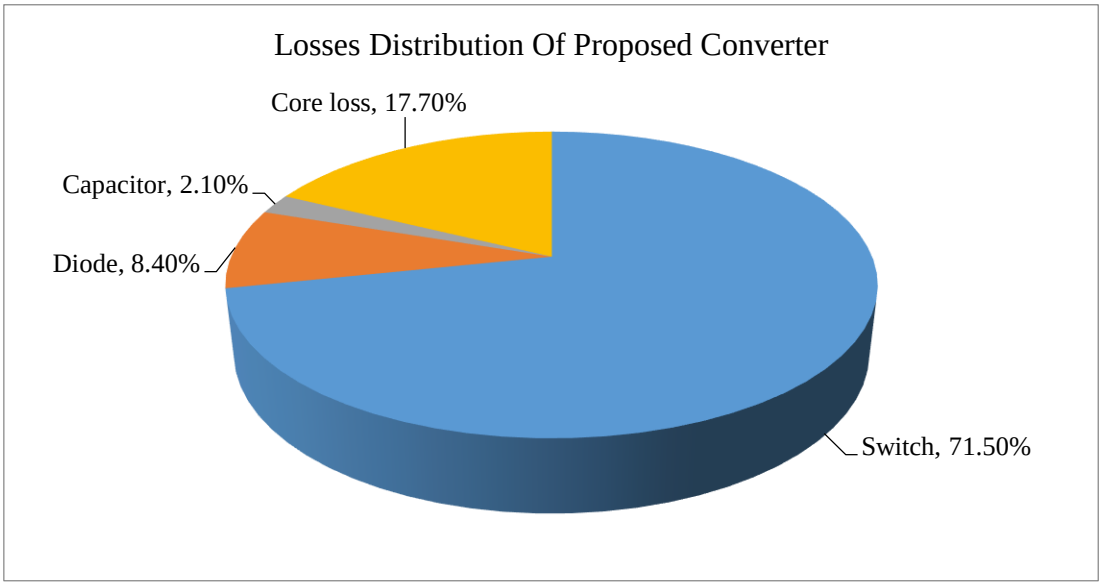


Fig. 20 Power loss distributions

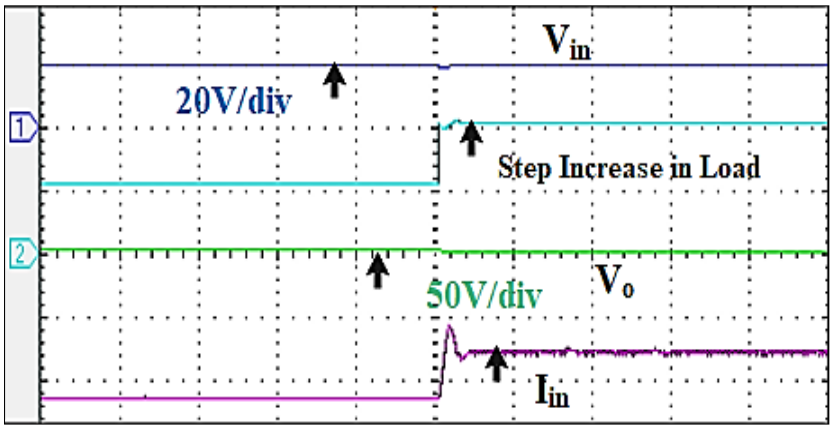


Fig. 21 Dynamic response of step load increase

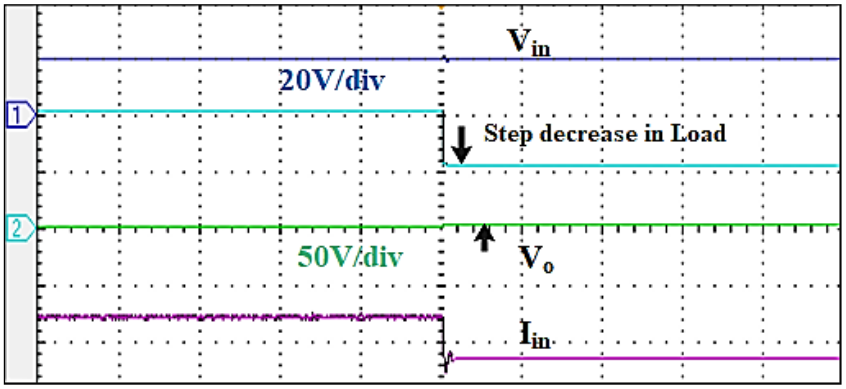


Fig. 22 Dynamic response of step load decrease

7. Conclusion

This article presented a transformer-less modified structure of a Quasi Switched-Single Inductor (QS-SL) configuration. Model Predictive Control (MPC) is used to provide ripple-free continuous load current, maintain a regulated output voltage at reduced 0.3% overshoot, and achieve a rapid settling time. Under the dynamic load conditions, the converter consistently maintains a regulated load voltage at 50V with an efficiency of 96.2% at 0.6-0.7 duty range. This implies that the proposed topology is suitable for auxiliary loads in electric vehicles.

The simulation findings were executed using MATLAB software, and a 200W experimental prototype was built and tested, and the results were obtained.

7.1. Future Scope

The proposed work can manage power flow from a single port to the DC load. While addressing this limitation, the converter is further extended as a multiport DC-DC converter powered with dual sources for electric vehicle charging systems and DC microgrids.

References

[1] R. Venugopal et al., "Review on Unidirectional Non-Isolated High-Gain DC-DC Converters for EV Sustainable DC Fast Charging Applications," *IEEE Access*, vol. 11, pp. 78299-78338, 2023. [CrossRef] [Google Scholar] [Publisher Link]

[2] Hadi Tarzamni et al., "Non-Isolated High Step-Up DC-DC Converters: Comparative Review and Metrics Applicability," *IEEE Transactions on Power Electronics*, vol. 39, no. 1, pp. 582-625, 2024. [CrossRef] [Google Scholar] [Publisher Link]

[3] Ankit Kumar Singh et al., "High Voltage Gain Bidirectional DC-DC Converters for Supercapacitor Assisted Electric Vehicles: A Review," *CPSS Transactions on Power Electronics and Applications*, vol. 7, no. 4, pp. 386-398, 2022. [CrossRef] [Google Scholar] [Publisher Link]

[4] Sara Hasanpour, "New Structure of Single-Switch Ultra-High-Gain DC/DC Converter for Renewable Energy Applications," *IEEE Transactions on Power Electronics*, vol. 37, no. 10, pp. 12715-12728, 2022. [CrossRef] [Google Scholar] [Publisher Link]

[5] Gangavarapu Guru Kumar et al., "Switched Capacitor-Inductor Network Based Ultra-Gain DC-DC Converter Using Single Switch," *IEEE Transactions on Industrial Electronics*, vol. 67, no. 12, pp. 10274-10283, 2020. [CrossRef] [Google Scholar] [Publisher Link]

[6] Hossein Gholizadeh, Saman A. Gorji, and Dezso Sera, "A Quadratic Buck-Boost Converter With Continuous Input and Output Currents," *IEEE Access*, vol. 11, pp. 22376-22393, 2023. [CrossRef] [Google Scholar] [Publisher Link]

[7] Yijie Wang et al., "A Single Switch Quadratic Boost High Step Up DC-DC Converter," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 6, pp. 4387-4397, 2019. [CrossRef] [Google Scholar] [Publisher Link]

[8] Vemparala Seshagiri Rao, and Kumaravel Sundaramoorthy, "Performance Analysis of Voltage Multiplier Coupled Cascaded Boost Converter With Solar PV Integration for DC Microgrid Application," *IEEE Transactions on Industry Applications*, vol. 59, no. 1, pp. 1013-1023, 2023. [CrossRef] [Google Scholar] [Publisher Link]

[9] Danyang Bao et al., "Switched Inductor Double Switch High Gain DC-DC Converter for Renewable Applications," *IEEE Access*, vol. 9, pp. 14259-14270, 2021. [CrossRef] [Google Scholar] [Publisher Link]

[10] Antonio Manuel Santos Spencer Andrade et al, "Hybrid High Voltage Gain Transformerless DC–DC Converter," *IEEE Transactions on Industrial Electronics*, vol. 69, no. 3, pp. 2470-2479, 2022. [CrossRef] [Google Scholar] [Publisher Link]

[11] Mohammad Farsijani et al., "Design and Implementation of a Single Switch High Gain Boost Topology: Structure, Ripple Control and ZCS," *IEEE Access*, vol. 11, pp. 2092-2104, 2023. [CrossRef] [Google Scholar] [Publisher Link]

[12] Amir Hossein Khanbabaie et al., "A Bidirectional Isolated DC-DC Converter with Low Voltage Stresses for Energy Storage Systems Integration," *IET Power Electron*, vol. 17, no. 3, pp. 1621-1711, 2024. [CrossRef] [Google Scholar] [Publisher Link]

[13] Zhixing Yan et al., "Ripple-Free Bidirectional DC-DC Converter with Wide ZVS Range for Battery Charging/Discharging System," *IEEE Transactions on Industrial Electronics*, vol. 70, no. 10, pp. 9992-10002, 2023. [CrossRef] [Google Scholar] [Publisher Link]

[14] Septimiu Lica, Dan Lascu, and Evelyn-Astrid Lovasz, "A New Step-Up-Down Quadratic DC-DC Converter with a Single Active Switch," *Journal of Computational and Applied Mathematics*, vol. 436, 2024. [CrossRef] [Google Scholar] [Publisher Link]

[15] Van-Cuong Bui et al., "A Novel Isolated DC-DC Converter for High Step-Down Applications," *IEEE Access*, vol. 11, pp. 81545-81562, 2023. [CrossRef] [Google Scholar] [Publisher Link]

[16] S.V.K. Naresh, Sankar Peddapati, and Mamdouh L. Alghaythi. "Anon-Isolated High Quadratic Step-Up Converter for Fuel Cell Electric Vehicle Applications," *International Journal of Circuit Theory and Applications*, vol. 58, no. 8, pp. 3841-3864, 2023. [CrossRef] [Google Scholar] [Publisher Link]

[17] Sara Hasanpour, and Sze Sing Lee, "New Step-Up DC/DC Converter with Ripple-Free Input Current," *IEEE Transactions on Power Electronics*, vol. 39, no. 2, pp. 2811-2821, 2024. [CrossRef] [Google Scholar] [Publisher Link]

[18] Guosheng Tian et al., "Isolated High Step-Up Soft-Switching Quasi-Z-Source DC-DC Converter," *IEEE Access*, vol. 12, pp. 49927-49936, 2024. [CrossRef] [Google Scholar] [Publisher Link]

[19] Xuefeng Hu et al., "A Single-Switch Coupled Inductor-based DC-DC Converter with High Gain and Low Voltage Stress," *IEEE Transactions on Power Electronics*, pp. 1-13, 2025. [CrossRef] [Google Scholar] [Publisher Link]

[20] Jie Ding et al., "A Single-Switch High Step-Up DC-DC Converter based on Three-Winding Coupled Inductor and Pump Capacitor Unit," *IEEE Transactions on Power Electronics*, vol. 37, no. 3, pp. 3053-3061, 2022. [CrossRef] [Google Scholar] [Publisher Link]