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Original Article

A High-Gain Multi-Input DC-DC Converter and Modified Fifteen-Level Inverter for PV-Based Grid and EV Charging Applications

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Abstract *- Efficiency of renewable energy conversion systems is gaining momentum with the trend toward compact power conversion architectures, which provide interfacing between low-voltage photovoltaic sources and medium-voltage Alternating Current (AC) systems while maintaining satisfactory quality. Conventional multilevel inverter topologies like Neutral-Point-Clamped (NPC), Flying Capacitor (FC), and Cascaded H-Bridge (CHB) abnormalities lead to huge devices, switching losses, and system complexity. For the first time, this article presents an integrated power conversion structure in which a high-gain single-input multi-output Direct Current (DC)-DC converter is combined with a reduced-switch fifteen-level DC–AC multilevel inverter to overcome these limitations. The system defined in this work produces many regulated DC voltage levels from one Photo Voltaic (PV) source and implements these asymmetrical voltages to synthesise a stepped multilevel AC through higher-voltage utilisation and decreased components required. In such a study, a sinusoidal pulse-width modulation control strategy is adopted to ensure stable driving operation and synthetic voltage in various loads. Simulation results indicate that the configuration achieves an output Root Mean Square (RMS) voltage of 230 V and a peak voltage of 325 V with enhanced harmonic performance, with a Total Harmonic Distortion (THD) for current and voltage at 3.9% and 2.8%, respectively. Moreover, the reduced active switches and absence of clamping diodes lower switching and conduction loss to 68 W and 54 W, respectively, leading to a total power dissipation of 122 W and a maximum efficiency of 96.4%. Therefore, the proposed architecture provides a compact and efficient solution for grid-connected photovoltaic systems, electric vehicle charging infrastructure, and distributed renewable energy applications that require high-quality power conversion.*

Keywords *- DC-DC Converter, Electric Vehicle Charging Infrastructure, Multilevel Inverter, Power Quality Improvement, Renewable Energy Systems, SDG 7-Affordable and Clean Energy, SDG 11-Sustainable Cities and Communities, Sinusoidal PWM control.*

1. Introduction

The rapid global shift towards renewable energy systems, electric mobility, and smart grids has significantly increased the demand for efficient, compact, and scalable power conversion architectures that can connect low-voltage renewable sources to medium- to high-voltage AC systems. Specifically, PV-based distributed generating systems have inherent limitations such as the low output voltage level, partial power generation, and environmental sensitivity, requiring high-gain DC-DC converters and advanced DC-AC inverter blocks [1-4]. Traditional boost converters, commonly used despite certain practical limitations such as severe duty-cycle operation, large current ripple in the inductor currents, and high stress on switches, have efficiency decreases at higher step-up ratios. To resolve these issues, various modified DC-DC conversion topologies such as cascaded boost converters, coupled-inductor-based converters, switched-capacitor configurations, quadratic converters, and hybrid topologies have been examined. The conventional two-level inverter is limited due to high switching and filter losses, poor harmonics performance, and large filters required; hence, it is not appropriate for high grid-quality applications. For this reason, NPC, FC , and CHB are the highlighted multilevel inverter topologies. Nevertheless, NPC inverters entail too many clamping diodes, and capacitor voltage equalisation remains difficult to achieve in flying capacitor inverters due to their integral number of capacitors and complex balancing approaches. CHBs are modular and versatile but require multiple isolated DC power sources, raising the cost and complexity of the system operation. Because of these

limitations, much research has focused on reduced switch multilevel inverter topologies that can create higher voltage levels with a smaller number of power devices and reduce the total standing voltage so that high efficiency can be achieved [5-7]. Recent developments have aimed to incorporate DC-DC boosting stages with multilevel inverter blocks directly, removing bulky isolation transformers and shrinking the system size while improving the conversion efficiency. Single-input multiple-output DC-DC converters have attracted increasing interest for their capacity to provide various regulated voltage levels from a single renewable source and thereby efficiently feed asymmetrical multilevel inverter topologies.

Nevertheless, many open issues remain in the conventional configurations that result in high switching losses because of the higher device number, unbalanced power sharing among inverter module stages, susceptibility to modulation index changes, and lower adaptation to nonlinear and variable loads. Considers that some of the systems claimed only address either voltage upgrade or harmonic mitigation without providing an integrated solution maximising power density, device usage, and quality, as well as dynamic stability for all those issues. The missing links are observed in the system-level design approach, including duty-cycle control, voltage gain profile, overall inverter modulation method, and loss model configuration [8-11].

Moreover, there has not been much focus on performance comparison between level-1 and level-m multilevel inverter topologies operating under the same power rating, which is important to prove practical dominance. Another key issue is to guarantee stable operation under rapid load changes and grid disturbances, because some of the current systems show transient oscillations, higher harmonic content, or control instability when a sudden change occurs. Therefore, among recent research trends is the development of more compact and higher-gain systems for power conversion that apply reduced-switch topology to good DC-DC converters, combined with advanced multilevel inverters employing simpler control techniques such as sinusoidal pulse-width modulation. Such are the previously microinverter-based grid-connected PV system introduced in [12] and the low-efficiency DC-AC-DC conversion systems reviewed in [13].

These systems are aiming at low THD, high efficiency, small total power loss, and improved voltage utilisation, as well as a low component count. The connectivity of these plants to real-time applications is becoming more and more relevant, such as in grid-connected photovoltaic plants, electric vehicle charging stations, battery energy storage systems, and smart microgrids. In EV charging infrastructure, high-efficiency conversion is important to step up low-voltage DC sources to grid-level AC with minimum losses [14-17]. In microgrid applications, harmonically superior multilevel converters allow smaller filters to be used and provide better quality of power as well as grid conformity. It is also the case that more compact transformers offer fewer solutions in terms of residential and commercial photovoltaic installations, which offer a number of positive features such as reduced cost per installed watt, higher power density, and improved system reliability. These application-oriented constraints highlight the requirement for compact, efficient, modular, and tolerant power conversion systems. Accordingly, the current trend of research focuses on designing integrated power conversion architectures to address voltage boosting, harmonic cancellation, loss minimisation, and dynamic performance concurrently with leading-edge technologies for renewable energy power electronics to develop safe, high-performance real-time applications [18-20]. The following targets are considered for the modified system.

- To develop a high-gain single-input multi-output DC–DC converter capable of efficiently boosting low-voltage photovoltaic input to multiple regulated DC voltage levels using optimized duty-cycle control, thereby enabling flexible and reliable power distribution for multilevel inverter operation.
- To design a reduced-switch fifteen-level DC–AC multilevel inverter topology that minimizes the number of active power devices, gate drivers, and passive components while achieving lower total standing voltage and enhanced voltage utilization.
- To implement an effective sinusoidal PWM-based control strategy that ensures stable inverter operation across a wide modulation index range, enabling precise voltage regulation, reduced harmonic distortion, and improved dynamic response under varying load conditions.
- To perform a comprehensive performance evaluation and comparative analysis focusing on voltage THD, current THD, switching loss, conduction loss, total power loss, and efficiency, establishing the superiority of the proposed system over conventional multilevel inverter configurations.

2. Modified DC-DC and DC-AC Converter Topologies and Operating Principles

The power conversion structure is the new one, including a single-input multi-output high-gain DC-DC converter in series with fifteen levels of reduced-switch DC-AC multilevel inverter, as shown in Figure 1, in which the PV source, control blocks, and grid-connected interface are clearly distinguished. The DC-DC converter topology shown in Figure 2 employs an inductor-based boost topology along with a controlled switching diode-capacitor network system to regulate the voltage for three DC outputs generated from a low PV input voltage. The design and performance parameters of the system are illustrated in Table 1. The converter also works in Continuous Conduction Mode (CCM), and the voltage gain is decided by the duty-cycle relationship as listed in Table 2,

whereby stepped-up voltages can be achieved at three levels of 46 V, 92 V, and 184 V with a 23 V PV input. The determination of component values, such as inductance, capacitance, etc., which are listed out in Table 3, is done following a procedure while keeping the current ripple and output voltage ripple low, while Table 1 gives an overall operating condition of the PV system and switching frequency. These controlled DC outputs are used as asymmetrical input sources for the fifteen-level inverter topology shown in Figure 3, which is proposed for higher voltage gain with a minimum number of active switches. It operates through the switching mode sequence at different output voltage levels. The operating modes for positive half-line voltages are shown in Figures 4 through 9, which show stepped outputs of 322 V, 276 V, 230 V, 180 V, 138 V, and 92 V by proper selection of DC source levels and controlled switch conduction paths. In Figures 10 through 17, asymmetrical negative voltage levels to -322 V can be achieved through the reversing of current paths in complementary switching states, ensuring production of a full-cycle AC waveform. When the DC sources and switching devices contribute to each voltage level in a sequential manner, a relationship between the DC-link voltage, switching logic, and output waveform shape is emphasised by all the figures. Operational investigation indicates that the proposed inverter keeps each voltage cell balanced and requires no extra clamping diodes and flying capacitors, which leads to a low number of components because of this characteristic. In addition, by using both the DC–DC converter and DC–AC inverter together and coordinating their operation properly, combined with level generation methods that rapidly switch between adjacent voltage levels, it can efficiently increase the output voltage of the cells generated based on a stacking structure while generating precise levels in such a way that harmonic distortion and switching loss become as low as possible.

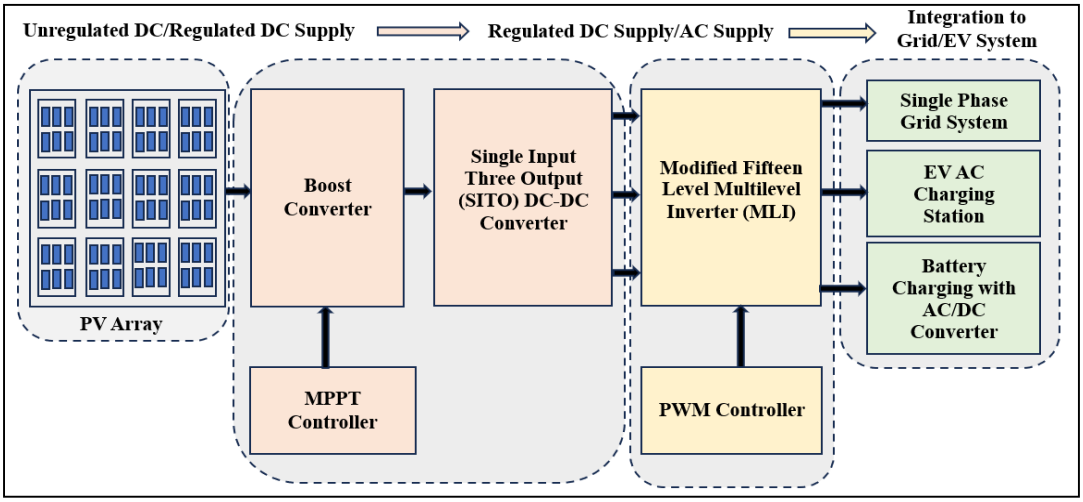

Fig. 1 Block diagram of the proposed multi-input DC - DC converter with grid integration

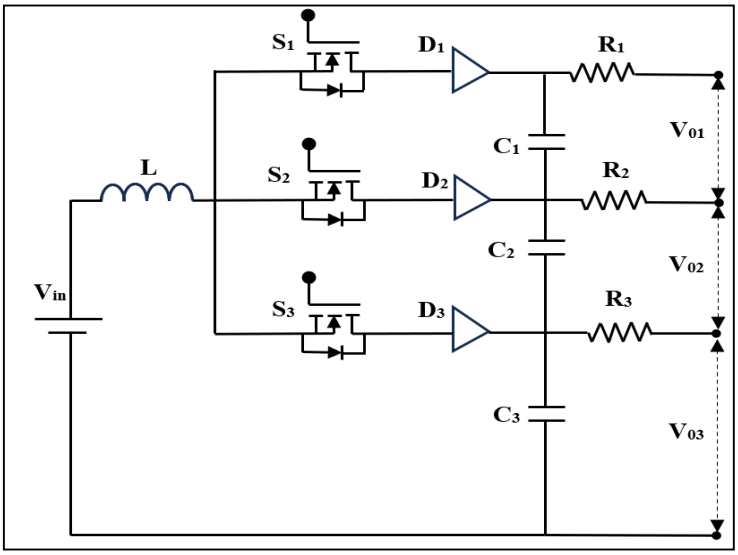

Fig. 2 Circuit topology of the high-gain DC-DC converter

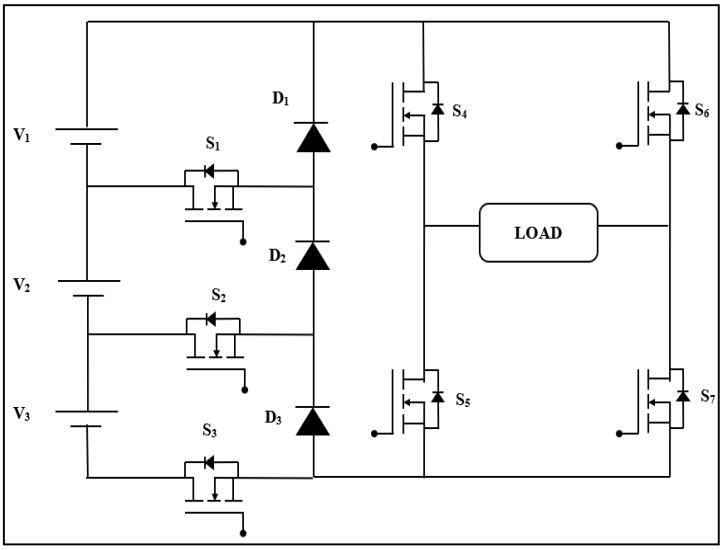

Fig. 3 Circuit configuration of the fifteen-level DC-AC inverter

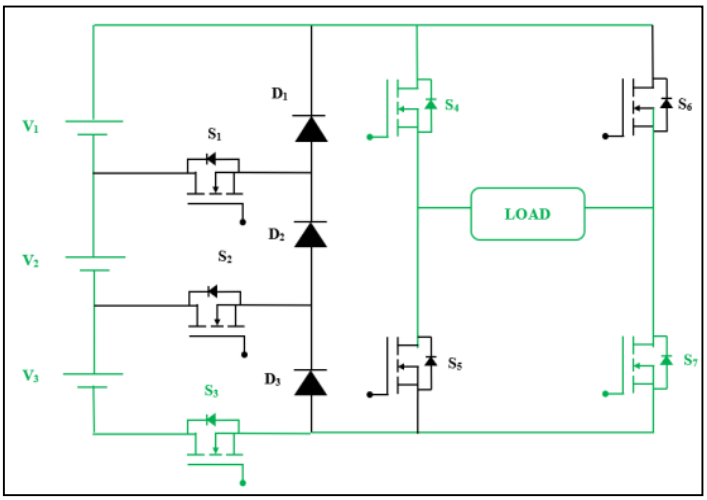

Fig. 4 Operating mode of the proposed inverter at output voltage of 322 V

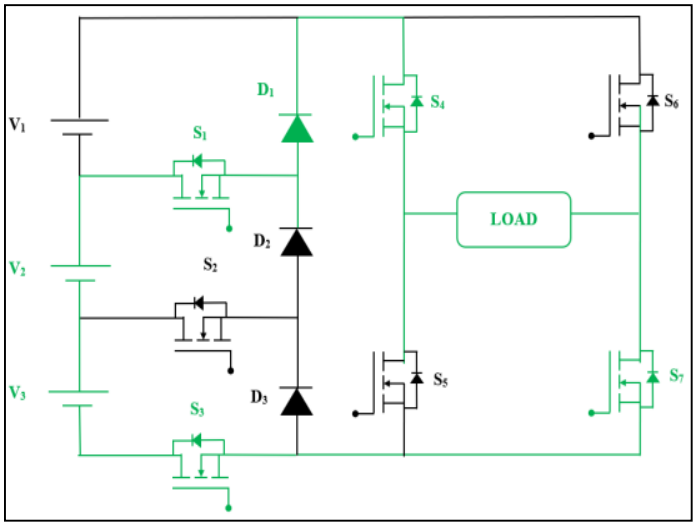

Fig. 5 Operating mode of the proposed inverter at output voltage of 276 V

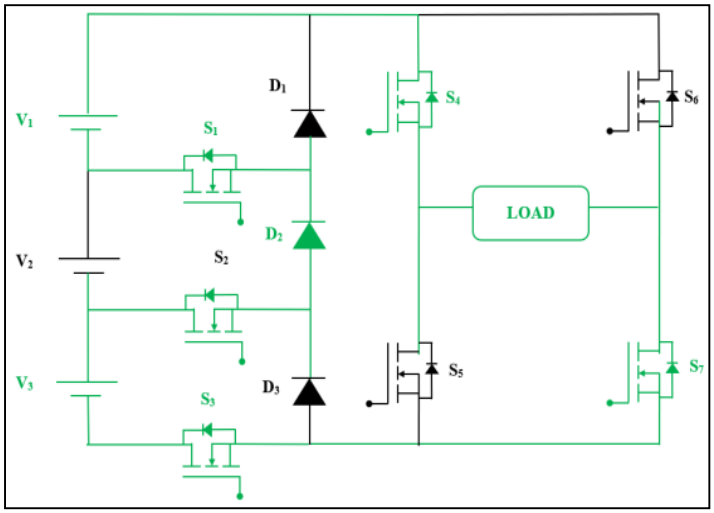

Fig. 6 Operating mode of the proposed inverter at an output voltage of 230 V

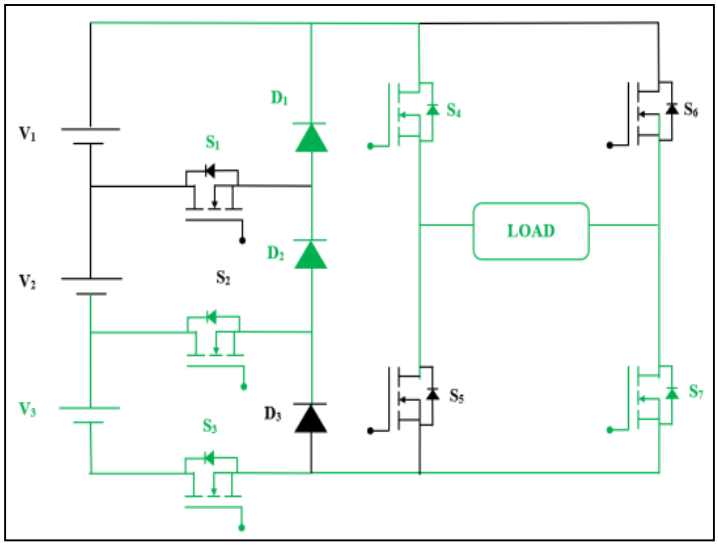

Fig. 7 Operating mode of the proposed inverter at output voltage of 180 V

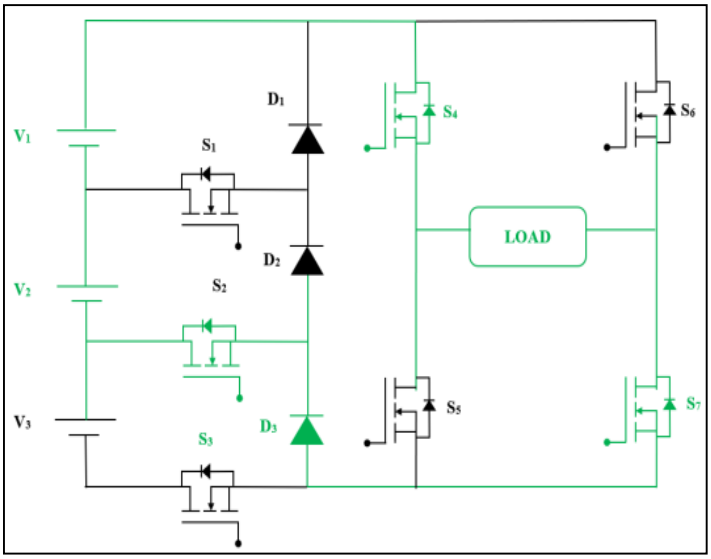

Fig. 8 Operating mode of the proposed inverter at output voltage of 138 V

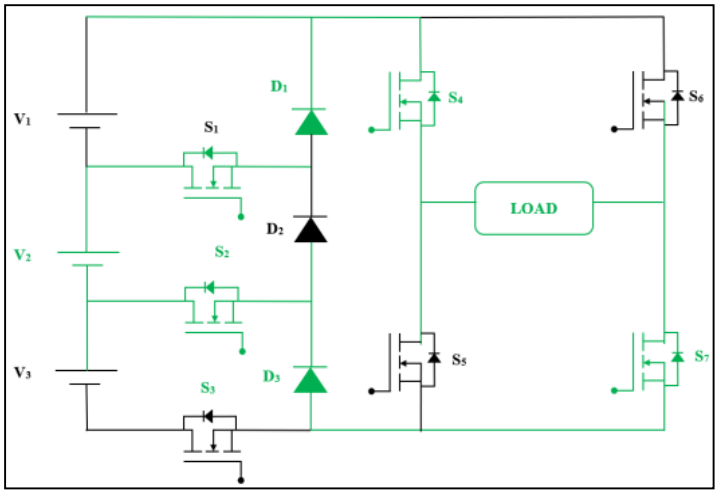

Fig. 9 Operating mode of the proposed inverter at output voltage of 92 V

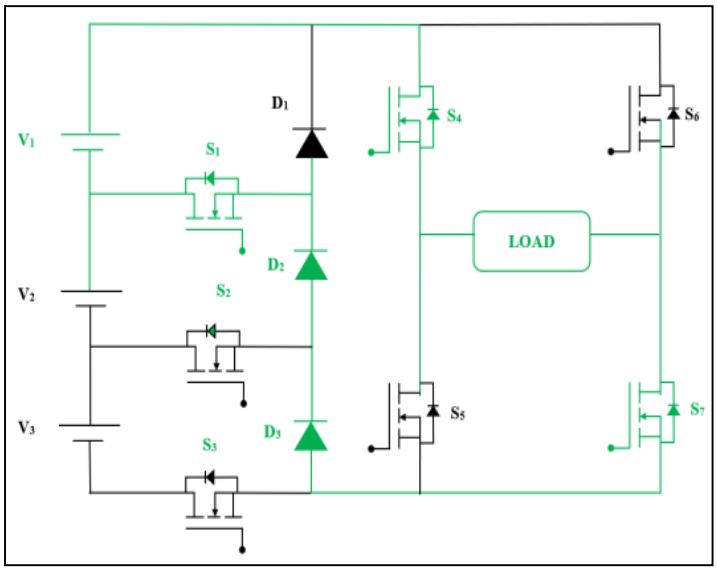

Fig. 10 Operating mode of the proposed inverter at an output voltage of 46 V

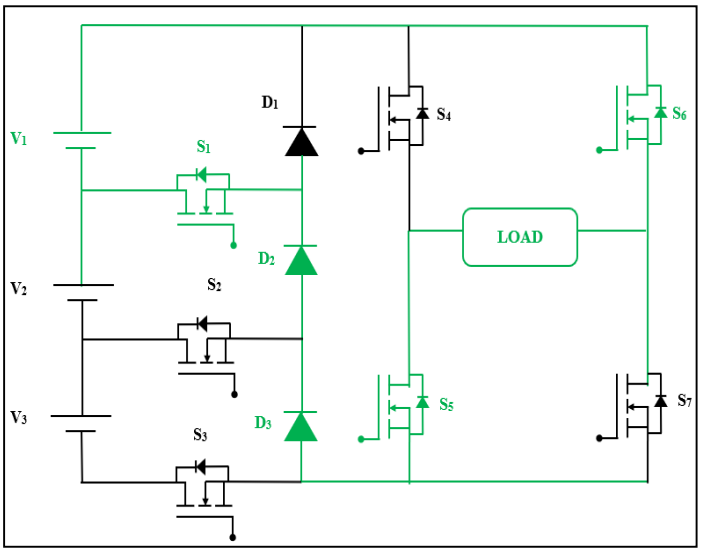

Fig. 11 Operating mode of the proposed inverter at output voltage of -46 V

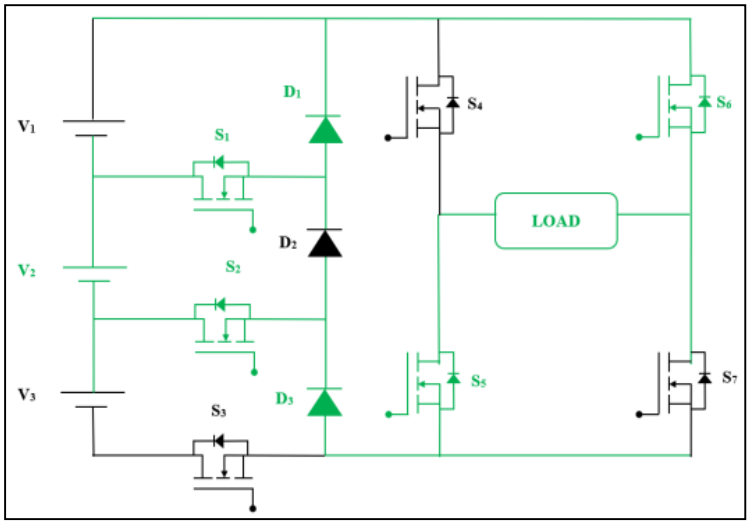

Fig. 12 Operating mode of the proposed inverter at output voltage of -96 V

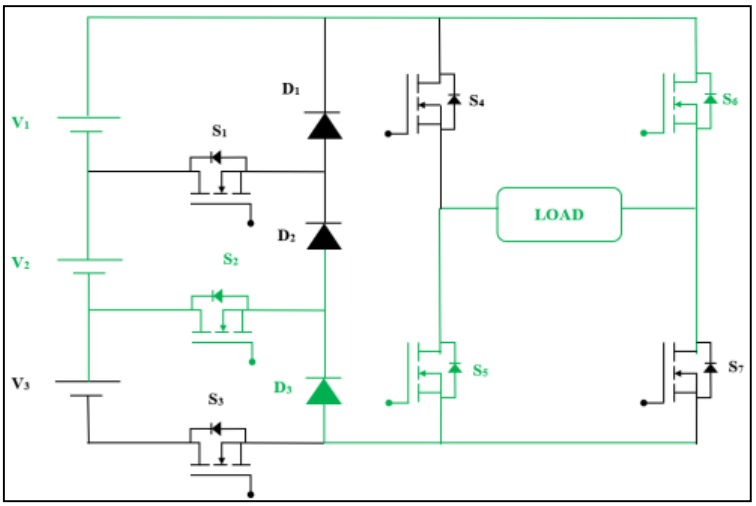

Fig. 13 Operating mode of the proposed inverter at output voltage of -138 V

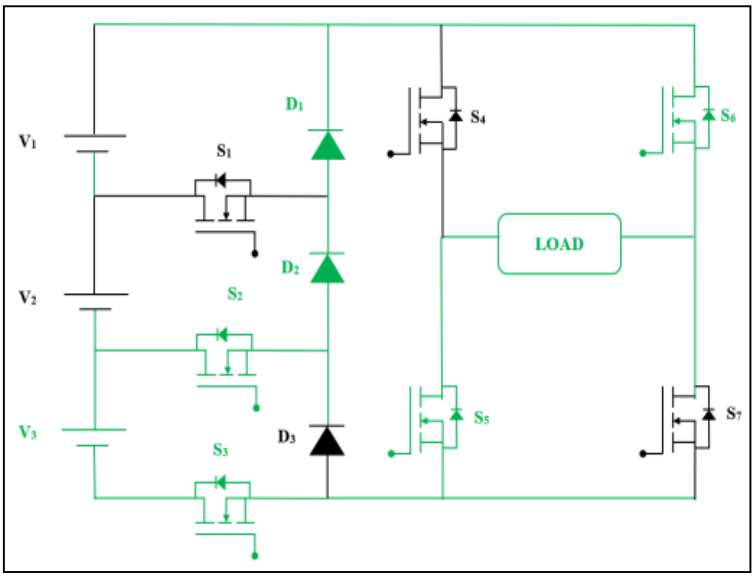

Fig. 14 Operating mode of the proposed inverter at output voltage of -180 V

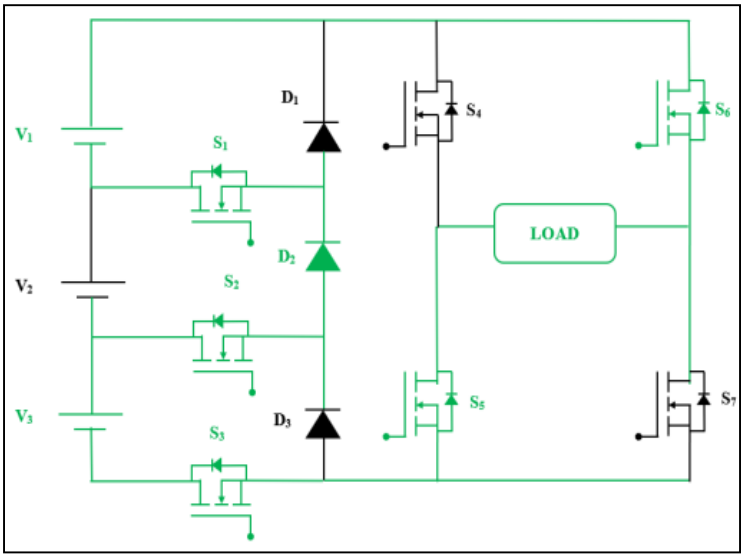

Fig. 15 Operating mode of the proposed inverter at output voltage of -230 V

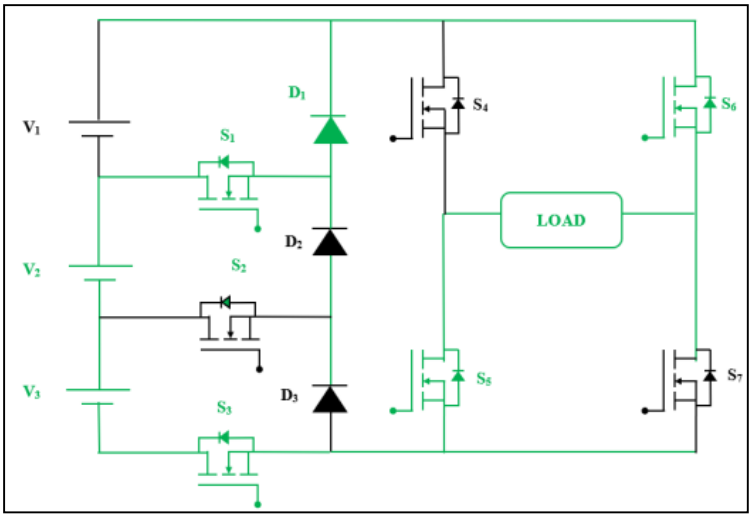

Fig. 16 Operating mode of the proposed inverter at output voltage of -276 V

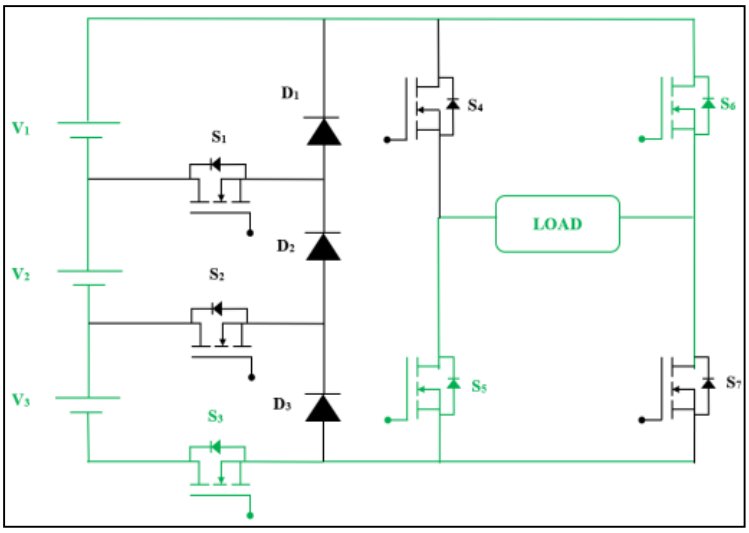

Fig. 17 Operating mode of the proposed inverter at output voltage of -322 V

Table 1. Design and performance parameters of the PV system

S.No.	Particulars	Design Values
1	PV operating voltage	23 V
2	Switching frequency (fs)	20 kHz
3	Switching period ($T_s = 1/f_s$)	50 µs
4	Output voltages (V_o)	46 V, 92 V, 184 V
5	Power per output (P_o)	200 W (each output, for sizing)
6	Input current estimate ($I_{in} = P_o/V_{in}$)	(200/23 = 8.70) A
7	Inductor ripple fraction (CCM) ($\Delta I_L = r_I I_{in}$)	1.74 A
8	Output voltage ripple target ($\Delta V_o = r_V V_o$)	0.02
9	PV panel Standard Test Conditions (STC) $\left((V_{oc}, I_{sc}, V_{mp}, I_{mp}, P_{mp})\right)$	28 V, 9.2 A, 23 V, 8.7 A, 200 W

Table 2. Voltage gains and duty-cycle relationship of the DC–DC boost converter

S.No.	Boost Voltage Relation	V_{PV} (V)	Vo (V)	Duty Cycle (D)
1	$V_o = \frac{V_{in}}{1-D}$	23	46	0.50
2			92	0.75
3			184	0.875

Table 3. Inductor and capacitor design parameters of the DC–DC converter

S.No.	Output Voltage (V)	Duty Cycle (D)	Inductor Design	$L_{Designed}$ (mH)	Capacitor Design	$C_{Designed}$ (µF)
1	46	0.50	$L = \frac{V_{in}D}{\Delta I_L f_s}$	0.33	$C = \frac{I_o D}{\Delta V_o f_s}$	118
2	92	0.75		0.50		44
3	184	0.875		0.58		12.9

3. Results and Discussion

The simulation result in terms of the performance of the designed power conversion system is well-detailed with some numerical evaluations in Table 4 and explicitly compared with benchmarked results given in Table 5, whereas dynamic and frequency response assignments are reflected by Figures 18 to 30. The DC–DC converter function under different DC cycles is early confirmed by using the output voltage waveforms in Figure 18, delivering the regulated DC voltage of 46 V, 92 V, and 184 V from the PV input of 23 V for duty cycles of 0.5, 0.75 and 0.875, respectively, indicating verification with the theoretical relation for voltage gain.

The corresponding pulse generation signals shown in Figure 19 work in stable switching mode at an unmodulated 20 kHz switching frequency, with constant pulse width and negligible output for uniform energy transfer and minimal current ripple. Figure 20 illustrates the use of a level-rotating sinusoidal reference in conjunction with a multi-carrier PWM structure to synthesise a fifteen-level accurately stepped output voltage waveform. The output voltage waveform under the resistive load of Figure 21 is a trapezoidal one, similar to the response of a resistive load with diminished voltage. Figure 22 exhibits a linear and sinusoidal voltage-current relationship at large efficiencies, demonstrating that the conversion between voltage and current is well transferred with almost perfect undistortion. The output current waveform in Figure 23 presents an absolutely smooth phase shift versus the voltage form and indicates that in the case of a reactive load, the inverter operates ideally with no oscillation or instability. Harmonics' behaviour is thoroughly investigated based on frequency-domain results; the voltage THD spectra shown in Figure 24 show a high peak of the fundamental and nearly suppressed higher-order harmonics, whereas the current THD spectrum in Figure 25 reduces to 2.8% more, verifying the effect of multilevel voltage synthesis on harmonics, which are much better than those obtained in traditional multilevel topology configurations, are consistent with the theoretical equations and performance indicators shown in Table 4. The dynamic response of the inverter for load change from resistive to resistive–inductive is shown in Figure 26 and shows the excellent dynamic stability and control robustness because of its small overshoot of voltage output and current output. The spectral properties of the modified fifteen-level inverter are further highlighted by the power spectrum in Figure 27 and the power spectral density diagram shown in Figure 28, which show drastic suppression of low- and mid-frequency harmonic components that would

result in lower electromagnetic interference and enhanced power quality. The RMS spectrum shown in Figure 29 indicates a uniform voltage distribution over changing frequencies, which demonstrates the uniform output voltage regulation. In Figure 30, it has been systematically investigated the impact of modulation index on inverter characteristics, where the rise in modulation index from 0.5 to 1.0 has caused an increase in the value of output voltage magnitude proportionately and a reduction in the values of both voltage and current THD for waveform quality, respectively, and is mentioned as well as a good correlation with depth of modulation to waveform quality. The comparative performance analysis in Table 5 provides additional evidence regarding the improved performance characteristics of the proposed fifteen-level inverter structure compared with conventional two-level, NPC, FC, and CHB topologies.The overall standing voltage is less than 644 V, much lower than the value as high as 1300 V in a cascaded H-bridge modular design, directly leading to low device stress and improved reliability. The loss analysis is conducted, from which the switching and conduction losses of the proposed structure are found to be 68 W and 54 W, respectively, with a total power loss of 122 W, significantly lower than that of conventional designs. Therefore, the inverter attains 96.4% maximum efficiency, which is higher than PWM-based NPC, FC, and CHB inverters.

Table 4. Performance evaluation parameters of the DC–AC inverter

S.No.	Parameters	Expressions	Justification
1	Output RMS voltage	$V_{\text{rms}} = \sqrt{\frac{1}{T}\int_0^T v_o^2\,(t)\,dt}$	$v_o(t)$: inverter output voltage, T: fundamental period
2	Fundamental RMS of output	$V_{1,\text{rms}} = \frac{V_{1,\text{pk}}}{\sqrt{2}}$	$V_{1,\text{pk}}$: peak of the fundamental component from Fast Fourier Transform (FFT)
3	Voltage THD	$\text{THD}_v(\%) = 100\sqrt{\frac{\sum_{n=2}^{\infty} V_{n,\text{rms}}^2}{V_{1,\text{rms}}^2}}$	$V_{n,\text{rms}}$: RMS of n$^{\text{th}}$ harmonic voltage
4	Current THD	$\text{THD}_i(\%) = 100\sqrt{\frac{\sum_{n=2}^{\infty} I_{n,\text{rms}}^2}{I_{1,\text{rms}}^2}}$	$I_{n,\text{rms}}$: RMS of n$^{\text{th}}$ harmonic current
5	Total harmonic distortion factor	$\text{DF} = \frac{1}{\sqrt{1+\left(\frac{\text{THD}}{100}\right)^2}}$	Often used to relate THD to the waveform.
6	Per-switch switching loss	$P_{\text{sw},k} = f_s\left(E_{\text{on},k} + E_{\text{off},k}\right)$	f_s: switching frequency; $E_{\text{on}}, E_{\text{off}}$: energy per event
7	Switching energy	$E_{\text{on/off}} = \frac{1}{2}V_{\text{sw}}I_{\text{sw}}t_{\text{on/off}}$	$V_{\text{sw}}, I_{\text{sw}}$: switch voltage/current at transition; $t_{\text{on/off}}$: transition time
8	Per-switch conduction loss	$P_{\text{cond},k} = \frac{1}{T}\int_0^T \left(V_{0,k}i_k(t) + r_{on,k}i_k^2(t)\right)\,dt$	V_0: threshold/saturation term; r_{on}: on-state resistance; $i_k(t)$: device current
9	Total inverter power loss	$P_{\text{loss}} = \sum_{k=1}^{N_s}\left(P_{\text{sw},k} + P_{\text{cond},k}\right) + P_{\text{passive}}$	N_s: number of active switches; P_{passive}: inductor/capacitor/transformer/snubber losses
10	Efficiency	$\eta(\%) = 100\frac{P_{\text{out}}}{P_{\text{in}}} = 100\frac{P_{\text{out}}}{P_{\text{out}}+P_{\text{loss}}}$	P_{out}: delivered AC power; P_{in}: DC input power

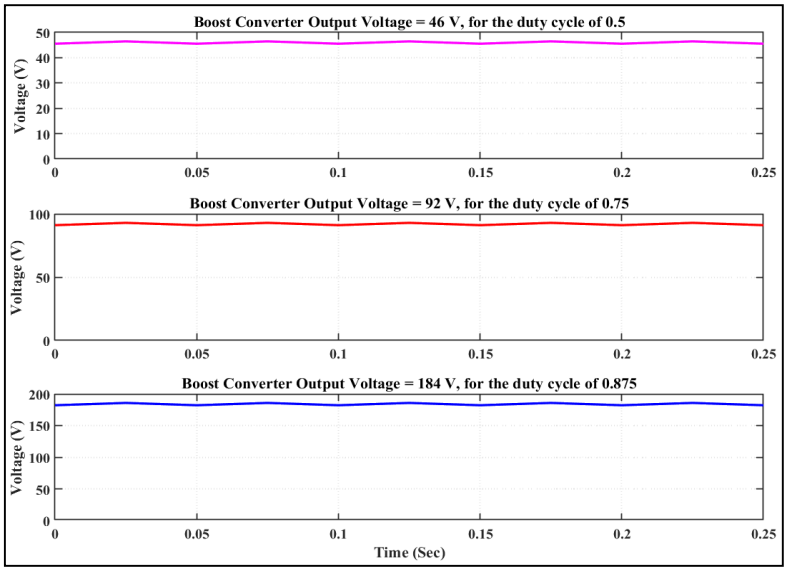

Fig. 18 Boost converter output voltages at different duty cycles

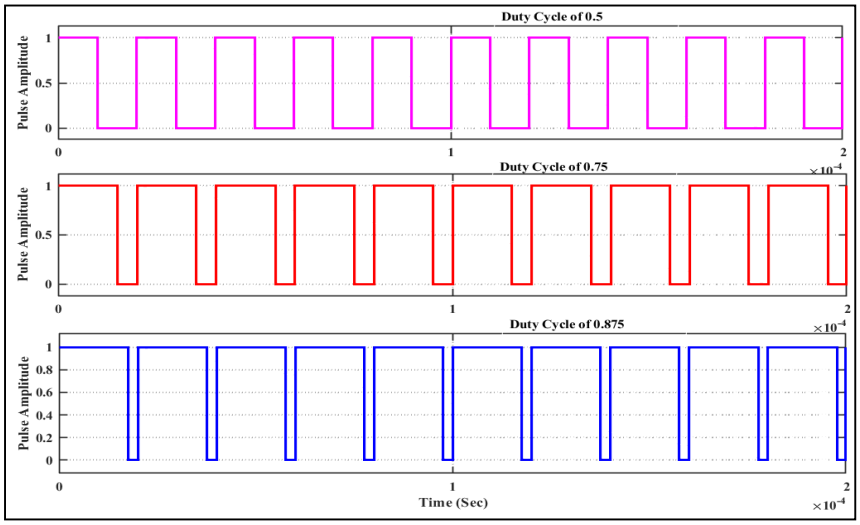

Fig. 19 Pulse generation for DC–DC converter at different duty cycles

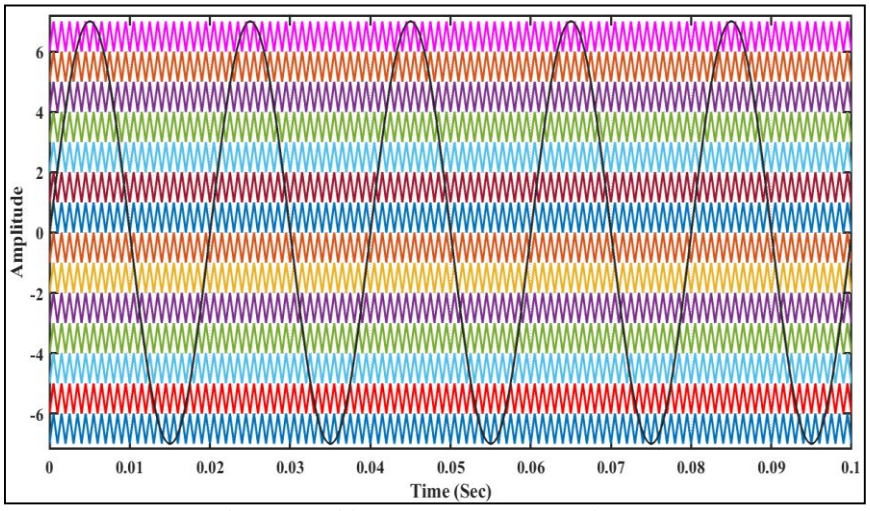

Fig. 20 Sinusoidal PWM for DC–AC fifteen-level inverter with reference and carrier wave signal

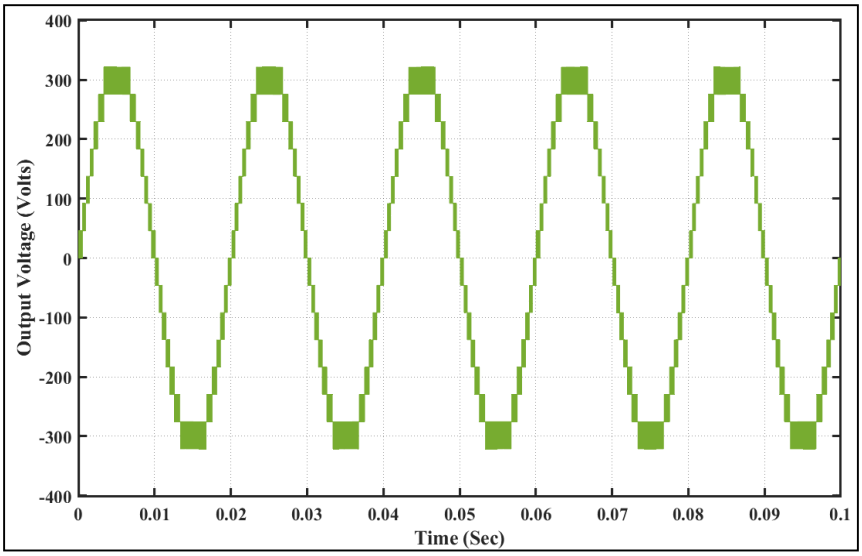

Fig. 21 Output voltage under resistive load

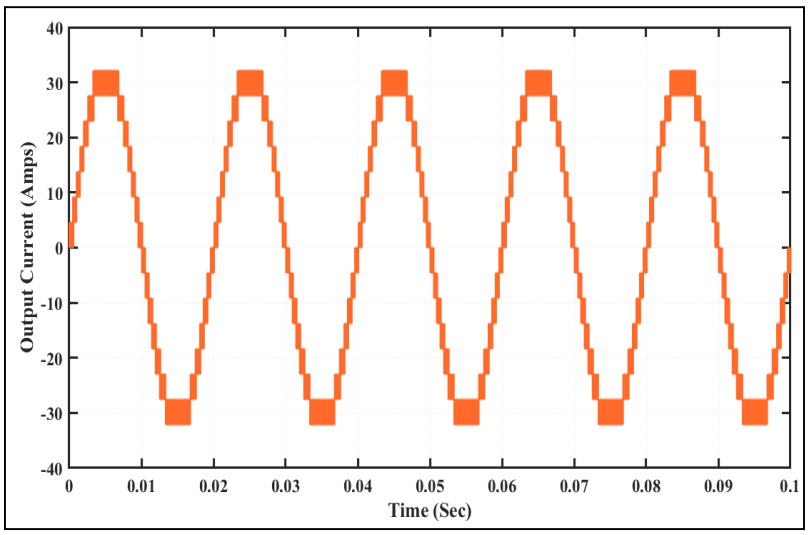

Fig. 22 Output current under resistive load

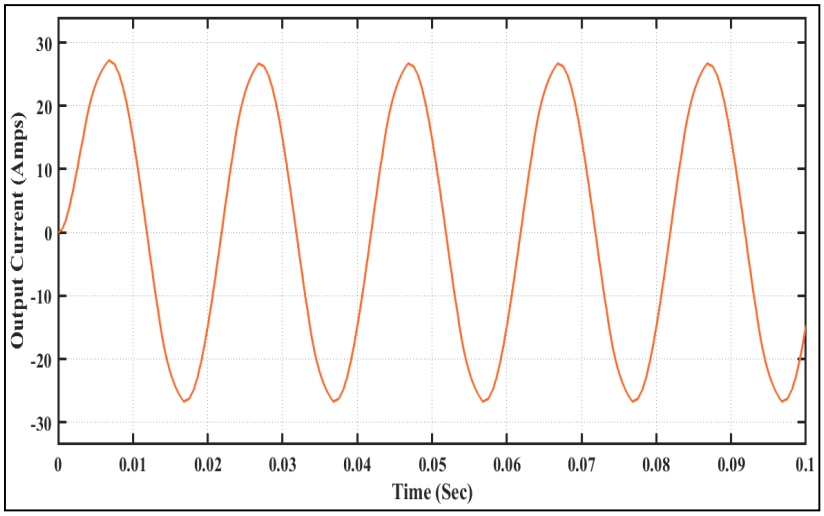

Fig. 23 Output current under resistive–inductive load

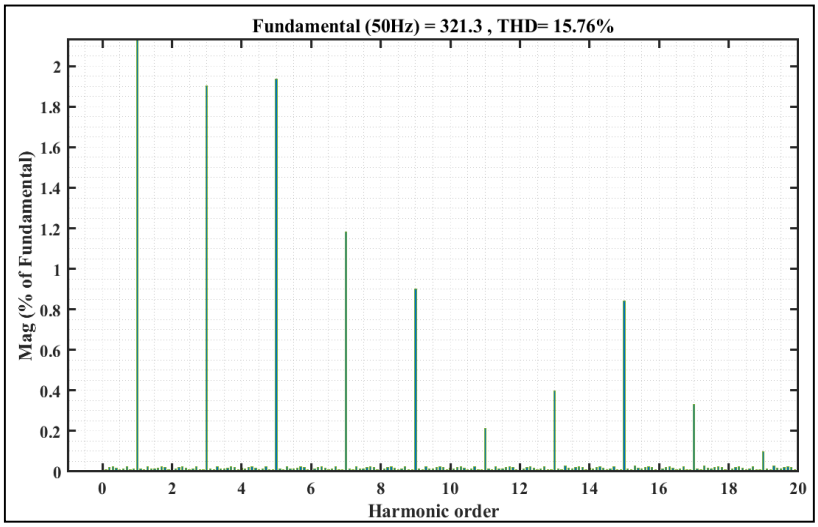

Fig. 24 Voltage THD spectrum under resistive–inductive load

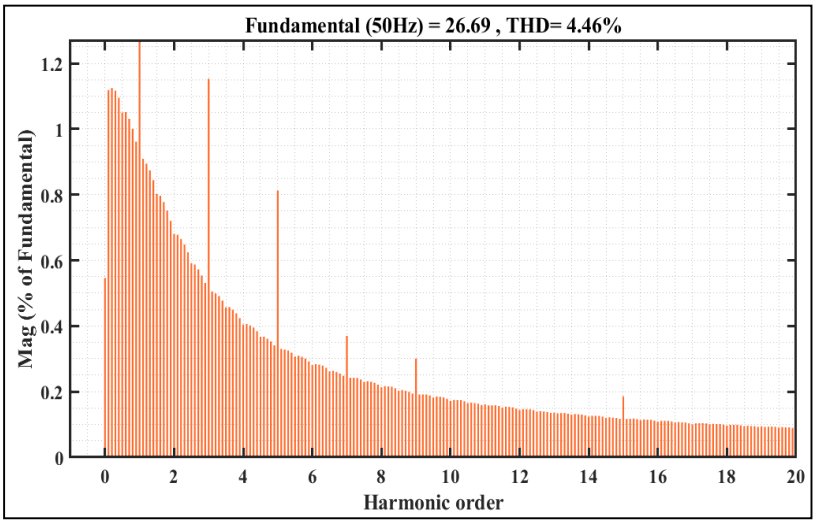

Fig. 25 Current THD spectrum under resistive–inductive load

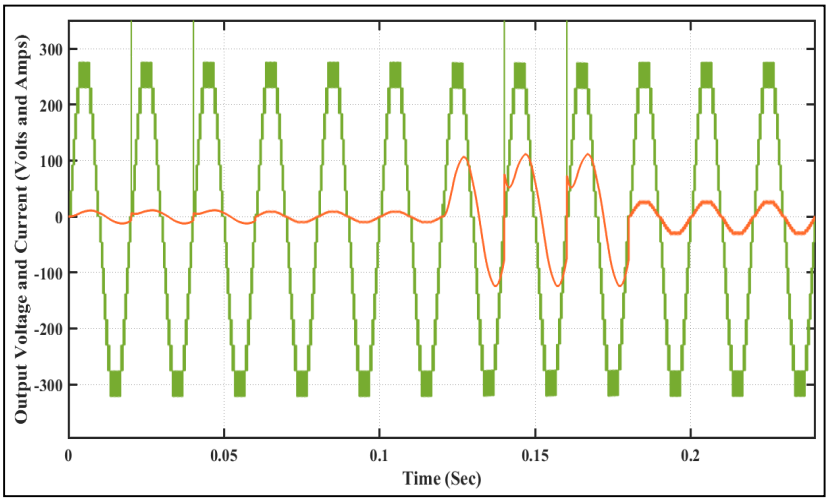

Fig. 26 Dynamic response during load transition between R and RL

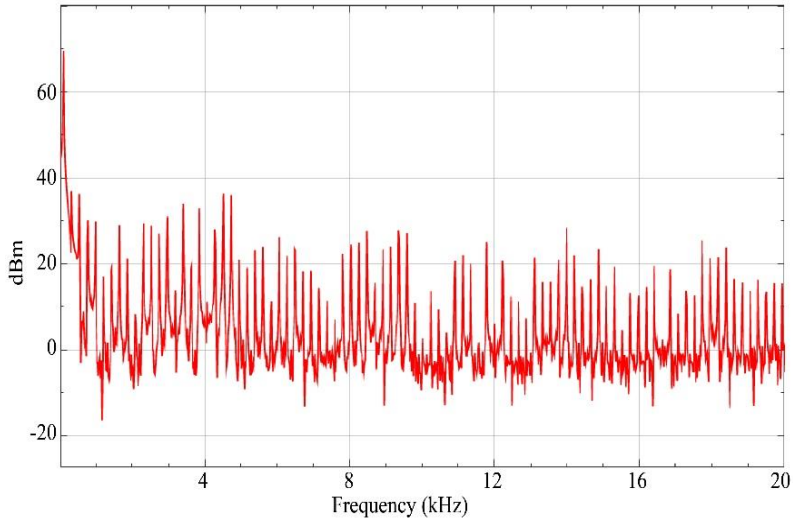

Fig. 27 Power spectrum of the modified fifteen-level inverter

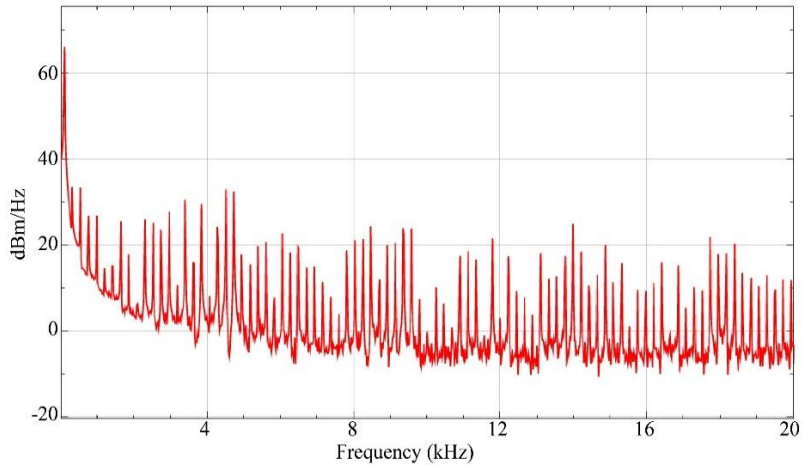

Fig. 28 Power spectral density of the modified fifteen-level inverter

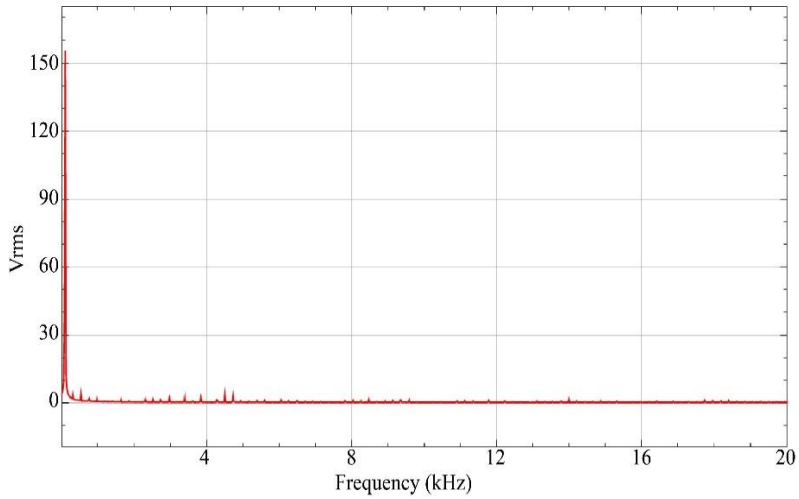

Fig. 29 RMS spectrum of the modified fifteen-level inverter

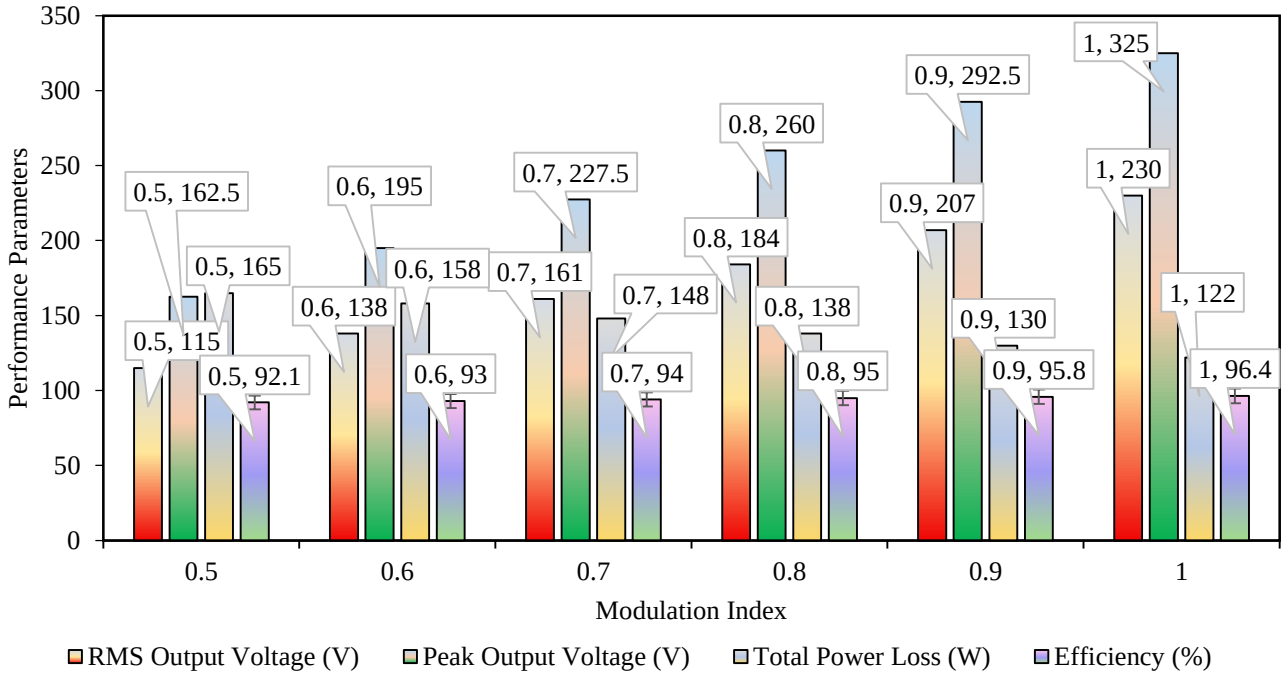

Fig. 30 Effect of modulation index on inverter performance parameters

Table 5. Performance comparison of conventional and proposed fifteen-level multilevel inverters

S.No.	Parameters	Conventional (2-Level)	NPC (15-Level)	FC (15-Level)	CHB (15-Level)	Proposed (15-Level)
1	Active switches (Ns)	2	28	28	28	7
2	Gate drivers	2	28	28	28	7
3	Clamping diodes	0	182	0	0	0
4	DC-link capacitors	1	14	14	0	3
5	Isolated DC sources	1	1	1	7	3
6	Maximum switch voltage (V)	325	23.2	23.2	46.4	184
7	Total Standing Voltage (TSV) (V)	650	650	650	1300	644
8	Switching frequency (kHz)	5	5.0	5	5	5
9	Voltage THD (%)	45	5.9	6	6.8	3.9
10	Current THD (%)	30	4.3	4.4	4.9	2.8
11	Distortion factor	0.912	0.998	0.998	0.998	0.999
12	Switching loss (W)	140	110	112	92	68
13	Conduction loss (W)	110	88	86	74	54
14	Total power loss (W)	250	198	198	166	122
15	Efficiency (%)	92.0	93.7	93.6	94.6	96.4

4. Conclusion

The analysis in this research is focused on the design of a compact and high-performance power conversion configuration by integrating the efficient circuitry of a single-input multi-output high-gain DC–DC converter with an ultracompact switching arrangement developed from the topology of a fifteen-level reduced-switch inverter suitable for renewable energy applications. The proposed topology not only steps up a low-voltage photovoltaic source but also gives several levels of DC voltages to synthesise high-quality multilevel AC output with fewer components and lower voltage stress. Simulation results show that the system provides 230 V RMS and a peak voltage of 325 V with improved power quality, taking a voltage THD of 3.9% and a current THD of 2.8%. Moreover, the shortage of switch elements and absence of clamping diodes reduces the switching and conduction losses to 68 W and 54 W, respectively, leading to the total power loss of only 122 W with a peak conversion efficiency of 96.4%. These results validate that the obtained converter-inverter arrangement has

significantly better harmonic performance, higher voltage utilisation, and increased efficiency than conventional multilevel inverter topologies in terms of vibration presented during normal operating conditions, which advocates for the main target of designing a compact yet high-quality power conversion system that is promisingly suitable for grid-connected photovoltaic systems and electric vehicle charging infrastructure as well as distributed renewable energy applications.

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