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Original Article

Performance Analysis of Energy Efficient Reversible Logic Circuits using Gate Diffusion Input Technique for Low Power Application

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Abstract *– Technologies are developing exponentially in present era and as device become more compact the consumption of power is becoming the major limitation in all devices. A new technique for designing of low power digital circuits is the Gate Diffusion Input (GDI) which retains low logic design complexity. Use of GDI technology in reversible logic drastically improves circuit complexity, power dissipation and area. The main aim of this research is to design and implement the various digital logic circuits using GDI technique for reversible logic circuit. In this research Basic reversible gates like Feynman, Toffoli, Peres gates are implement using GDI technique. Further for design various digital combinational circuits propose new GDI base reversible gates such as RGG, RGG2 and PRGG1. Some trade-offs are made in the design to increase performance efficiency. Propose gate is used to implement a digital circuit such as the Full Adder, 4:1 Multiplexer, Demultiplexer, 4-bit magnitude Comparator, 8:3 Encoder and 4:16 BCD to Decimal Decoder and executes the parametric analysis for these circuits. The propose designs found enormous improvement over power dissipation, area and gate count with the existing design. Comparison is demonstrated in the result section. For implementation and simulation EDA Tanner tool, V13 is used using 90nm technology with supply voltage 1V.*

Keywords *– Reversible Logic, GDI, Multiplexer, Magnitude comparator, Low power encoder, BCD decoder.*

1. Introduction

According to the International Technology Roadmap for Semiconductors (ITRS) it will be extremely difficult to reduce the size of a single transistor after nanometer technology. Numerous second-order phenomena, including leakage power, heat dissipation, sub-threshold, tunneling etc. would result if decreasing the size of transistor. Energy dissipation in circuits is one of the major issues in present day technology. An innovative technology must develop to keep Moore's Law alive in future. The motivation behind reversible logic is, irreversible technologies available today can dissipate lots of heat and shorten device life. R. Landauer proved that energy is lost when bits of information are lost. It has been demonstrated that every bit of information lost results in at least K.T.ln2 joules of heat energy, where T is the system's operating temperature and K is the Boltzmann constant [1]. Reversible logic is likely to be in demand for high-speed power sensitive circuits. In a reversible circuit, the input and output vectors are mapped one to one meaning is that any input vector can produce distinct output vector and vice versa. The ability to produce a one-to-one relationship between i/p and o/p is a property of reversible logic. In reversible logic circuits no information is lost only if the system is made up of reversible gates that would cause zero power dissipation [2]. Application of reversible logic is found in different area such as low power, quantum Computing, digital signal processing, cryptographic hardware etc. The GDI method was first presented by Morgenshtein [3] in year 2002. This technique allows reducing power consumption, propagation delay and area of digital circuits while maintaining low complexity of logic design. With just two transistors the GDI technique enables the construction of a large number of intricate logic operations. Compared to CMOS and current Pass Transistor Logic approaches GDI uses fewer transistors to construct fast, low-power circuits, improves logic level swing and static power characteristics and enables straightforward top-down design with a tiny cell. This research uses unique approach for design of 4:1 Multiplexer, 1:4 Demultiplexer, 4-bit magnitude comparator, 8:3 Encoder and 4:16 BCD to Decimal Decoder.

2. Literature Review

Various design are available for implementation of digital circuits using reversible logic. Sheba Thabah et.al. [4] suggested two innovative designs for decimal to binary coded decimal (BCD) encoders using Peres and Feynman gates. The methodology discussed minimizes the gate count (GC), garbage outputs (GO) and quantum cost (QC). Himanshu Thapliyal et.al.[5] used reversible Fredkin, Feynman and Toffoli Gates to build new designs for reversible sequential circuits, including latches and flip flops. Additionally, two novel reversible gates are suggested the Modified Toffoli Gate (MTG) and Fredkin Gate (MFG) in the suggested designs the number of reversible gates and garbage outputs were improvement. A. Meidy et.al.[6] proposed new reversible full and half adder design using Feynman, Toffoli and Fredkin gates. It becomes apparent that the described reversible adder is efficient in lowering the number of transistors, gates count, garbage outputs and constant inputs. The reversible ripple carry adders using PFAG and HNG are implemented. The improved performance of Ripple Carry Adder using the said gate evaluated [7]. Shukla V. et.al.[8] implemented a 4-bit array multiplier design and evaluated against previous designs based on a few chosen characteristics and found to be the best design. Additionally provided a synthesized circuit and generated output waveform for the suggested design. Mukherjee D. et.al.[9] proposed a reversible magnitude comparator that is constructed using GDI technique and makes use of the most popular reversible gates. Additionally, design approaches for the N-bit comparator are proposed. Compared the outcomes for quantum cost, number of reversible gates, garbage output, and constant input. The suggested comparators transistor representations are carried out using EDA Tanner tools integration of CMOS and GDI techniques. Seyedeh F. et.al.[10] designed CNTFET with a 32nm technology for the creation of a new full adder (FA). The Full Adder has three reversible logic gates in two of its stages that are realized by using GDI technique. Mukherjee D. et.al.[11] suggested a single 12-bit comparator with a multiplexer that uses less area and has minimal power dissipation. Another design 4-bit comparator blocks have been employed instead of a single 12-bit comparator to improve speed and power consumption, propagation delay and transistor count. Lastly in 12-bit comparator overall performance has been enhanced through insertion of the unique technique. Basha M. et.al.[12] proposed new reversible M and L gates and presented an optimized reversible comparator. The design is highly beneficial quantum computers and ultra-low power digital circuits. Vudadha C. et.al.[13] proposed reversible comparator design in three stages in this technique involves calculating the results in a hierarchical manner where intermediate results are stored and used for final comparisons. The comparator structured as a tree where each level processes pairs of values and propagates results upwards. When compared to the tree-based comparator design with existing design the suggested 64-bit comparator design resulted in lower quantum delay and garbage outputs. R-gui Zhou et.al.[14] create a quantum adder/subtractor this research built a novel reversible 4*4 gate name ZRQ gate. The ZRQ gate is suggested as the least amount gates and QC for a 1 bit and 4-bit reversible comparator using ZRQC module. Gaur H. et.al.[15] proposed comparative study and analysis of different reversible gates. Gates are synthesized using the RC-viewer tool. The comparison is carried out at two successive levels namely the construction level of gates and the circuit design level. Harsh Pallav et.al. [16] proposed 16×16 Harsh Shiva Gate1 (HSG1) performing logical output operations. HSG1 gate has one Simultaneous Mode and Cascade mode is used logical unit in ALU along with Control Unit. Mozammel K. et.al.[17] suggested three elements: reversible KMD gates for fault detection, fault coverage and fault tolerance. The suggested study of the KMD Gates supports minimum test vector, 100% fault coverage and 50% fault tolerance. Additionally, a comparison of the controlled V and V+ gate and its quantum equivalent in all KMD gate types was presented, having a notable decrease in quantum cost. Dilip P. Vasudevan et.al.[18] proposed R, R1, R2 gates, 4*4 R2 gates can be used to create online tested bidirectional logic circuits; R1 gates will execute any Boolean function. Two rail checkers that are integrated into the design allow errors to be identified online. The complimentary output at e1 and e2 in the two-rail checker will be generated by the fault-free checker. Mariam Z. M. et.al.[19] designed combination of the multiplier and adder circuit. In designs I and II, PG and TG are utilized for partial product generation. Compared to alternative designs, the suggested circuit reversible logic multiplier has less hardware complexity and a lower quantum cost. Md. Selim Al Mamun et.al. [20] proposed quantum cost optimization for reversible sequential circuits using new 3*3 reversible SAM gate which addressing the challenge of minimizing resource requirements while maintaining functionality and performance. Lafifa Jamal et.al.[21] proposed a reversible control unit. The J-K flip-flop and reversible decoder are designed using HL and BJ gates, respectively. Sequence counter, instruction register, control logic gates and a reversible decoder were proposed and compared to the ones that already existed. The comparative findings demonstrate that the suggested architecture performs better than the current designs in terms of delay, quantum cost, garbage outputs and gate counts. Kamaraj A. et. al. [22] designed a novel reversible ALU using fault-tolerant KMD gates. The functional simulation performed in QCA and the quantum circuit. Results verify that the proposed ALU is better in number of terms than the existing design. This paper presented a novel energy-efficient 4-bit Vedic multiplier utilizing GDI approach, specifically designed for implementation in 32 nm technology. Nishanth R.K. et.al.[23] proposed the Vedic multiplier architecture by incorporating the modified GDI technique which reduces switching activity and leakage power. By strategically implementing GDI gates achieved significant improvements in energy efficiency while maintaining high-speed operation. The design is simulated to evaluate performance metrics using Tanner EDA tools. Hafiz Md. Hasan Babu et.al. [24] proposed reversible low power n-bit binary comparator using new BJSS and HLNS gates. Nagamani A. N.et. al. [25] design magnitude and signed comparators, using Fredkin, Feynman, and Peres gates. A number of performance metrics are tuned, with a focus on delay optimization. Dmitri Maslov et.al.[26] introduces two algorithms: one that synthesizes all optimum implementations and the other that synthesizes a circuit for each 4-bit reversible design. The author employs a number of strategies to make the issue manageable. Fault tolerant Peres gate is design for full adder application [27]. Jebashini Ponnian et.al.[28] proposed MUX based and BDD based synthesis algorithm for power and augment improvement. MUX and DEMUX have been presented using reversible based GDI gates and compare the result with the existing literature [29-31]. Analyzed the working of 8x3 encoder and decoder, hamming encoder, decoder using reversible gates. Their functionality is verified and power is obtained using Xilinx and Cadence tools. The proposed method of encoder and decoder show improvement when compared with the existing designs [32]. Proposed N-bit reversible comparator based on TR and CNOT with a binary tree structure. Implemented NLG gate for construction of 4-bit comparator [33-34]. Two novel reversible gates were proposed by Tarlochan et al. the TCG gate, which is a 4x4 reversible gate, and the CCG gate, which is a 3x3 reversible gate. Two signals can be compared using a single bit using the TCG gate. Three SBGE circuits, one SBLT circuit and one TCG gate make up the design of the suggested 4-bit reversible comparator [35].

3. Basic Reversible Gates

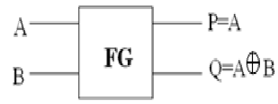
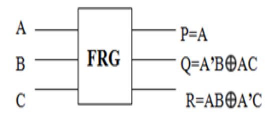
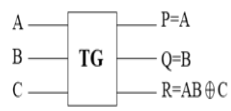
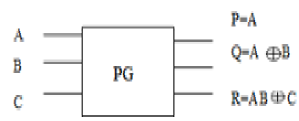
3.1 Basic Definitions:

•Garbage Output: Garbage output is the term for gate output that is not utilized as a primary output or as an input to other gates. Garbage outputs are unused outputs that are necessary to keep a reversible gate (or circuit) reversible.

•Delay: The maximum number of gates in a path from any input to any output is known as the logic circuit's delay. For 1*1 and 2*2 gates, take into account the unit delay which is 1Δ.

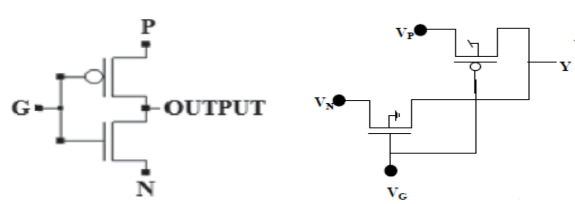
•Quantum Cost: The quantity of 1x1 and 2x2 reversible gates or quantum gates needed for a reversible gates design is known as its quantum cost. All reversible 1x1 and 2x2 gates are assumed to have quantum costs of unity.

•Ancilla Input (AI): Ancilla inputs are sets of inputs that are kept at a constant value, either logic "0" or logic "1," in order to create the specified logical function.

Basic Reversible Gate	Description
 **Fig. 1. Feynman Gate (FG):**	FG is a two input; two output basic reversible gate perform XOR operation at second output shown in fig.1 also called controlled not gate.
 **Fig. 2 Fredkin gate**	FRG is a three input three output conservative reversible gate can perform different operation by controlling the third input.
 **Fig. 3 Toffoli gate**	TG reversible gate three input three output gate which act as a universal gate for design of reversible circuits also called controlled-controlled-NOT gate.
 **Fig. 4 PG Gate**	PG is a three inputs three outputs reversible gate can perform basic application like XOR, AND output expression is shown in Fig.4.

4. Existing frame work

One of the most difficult problems with developing VLSI circuits in the context of modern technology is power efficiency. One of the utmost strategies for low power applications is reversible logic. GDI methodology is a simple method for representing any logic function. Basic cell and its alternate arrangement are shown in Fig.5.



(a) **(b)**

Fig. 5a GDI cell 5b). Alternate basic GDI cell

GDI technique allow for less logic design complexity of digital circuits use for less power consumption, low propagation delay and small area. The GDI cell contains three inputs: G (common gate input of NMOS and PMOS), P (input to the source/ drain of PMOS) and N (input to the source/ drain of NMOS).

Table 1: GDI Functionality

N	P	G	Equation	Operation
0	B	A	Ã B	Function1
B	1	A	Ã +B	Function2
1	B	A	A+B	OR
B	0	A	A. B	AND
C	B	A	Ã. B+A .C	MUX
0	1	A	Ã	NOT

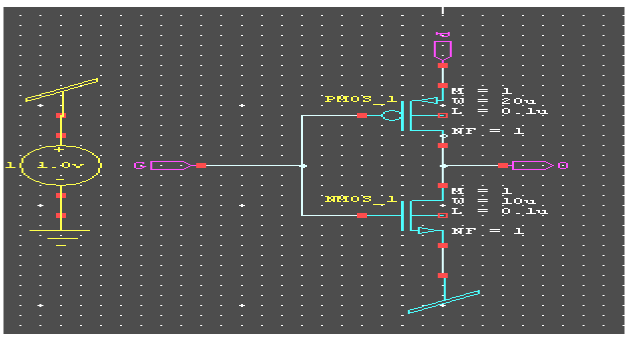


Fig. 6.a) Transistor implementation of OR gate design using GDI technique.

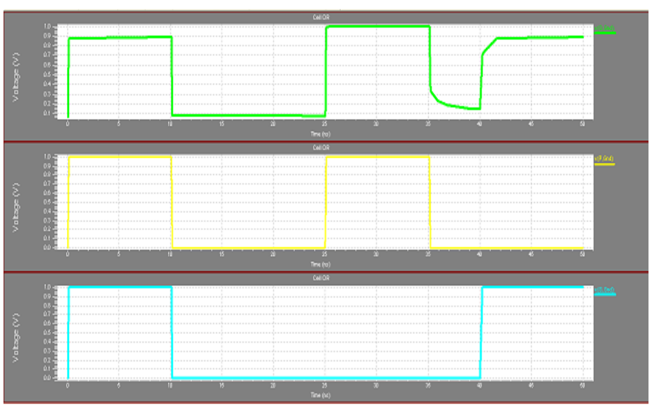


Figure 6. b) Simulation results for OR Gate using GDI.

Transistor design of GDI cell is implemented and its simulation result is shown in Fig. 6. This can be verified from the truth table for any logic function by using different inputs for P and N. Power dissipation for GDI cell is avg. power = 0.23808uW.

4.1 Design of Feynman gate (FG) Using GDI

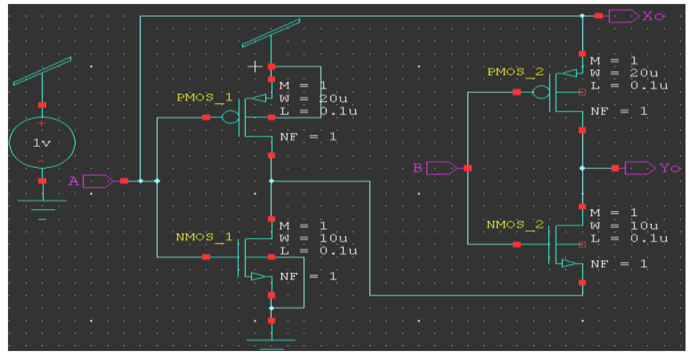


Fig. 7a) Transistor Implementation of Feynman Gate using GDI

2*2 FG is shown in figure 7. For construction single inverter and GDI cell is required. (P=A, Q=Xo⊕Yo) Output function can be verified form simulation result. For GDI implementation required only 4 transistors. Power dissipation for Feynman gate is avg. power=3.1386uW and Max. Delay=20.10ns.

Fig. 7b) Simulation result Feynman Gate Using GDI

4.2 Transistor design of Toffoli gate (TG) using GDI

3*3 TG gate can be design using two NOT gate and one GDI cell shown in figure 8. For TG implementation required only 6 transistors. Output can be verified by using equation (P=A, Q=B, R=A.B ⊕ C). Power dissipation for Toffoli gate avg. power is 6.8889uW and MAX_DELAY is 9.9ns.

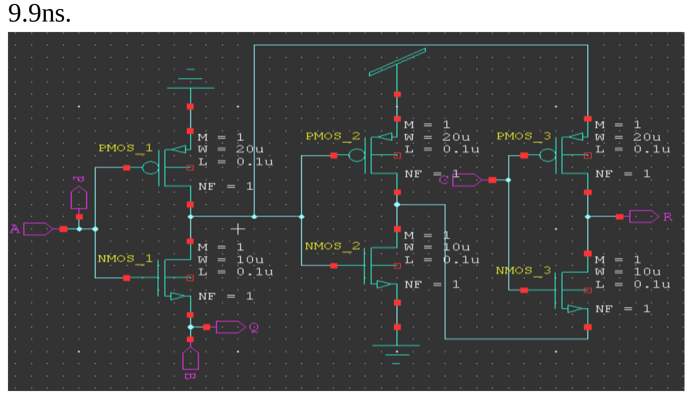


Fig. 8a) Transistor Implementation of Toffoli gate using GDI cell.

Fig. 8b) Simulation results for Toffoli Gate using GDI.

4.3 Transistor Implementation of Peres Gate (PG) using GDI

3*3 PG using GDI is shown in figure 9 where A, B, C input and P, Q, R output. GDI cell implementation required only 10 transistors required.

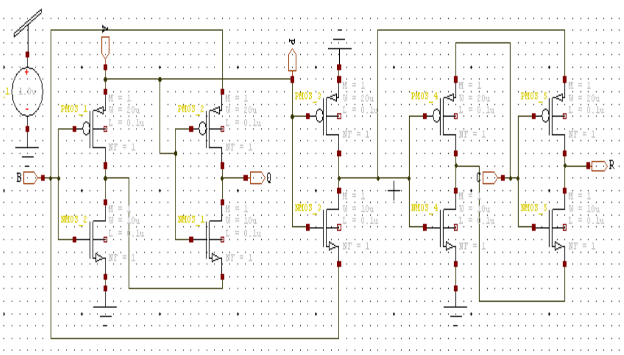


Fig. 9a) Transistor Implementation of PG using GDI

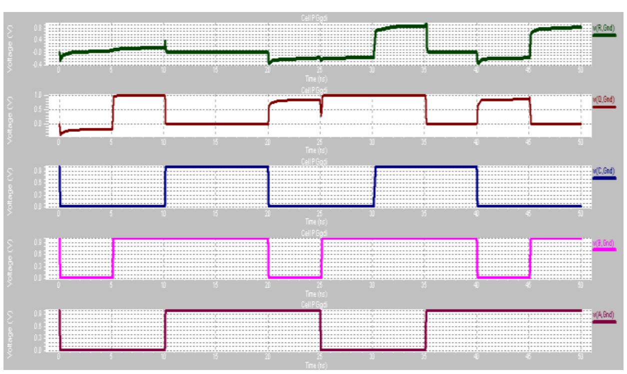


Fig. 9b) Simulation result for PG Gate using GDI

4.4. Transistor Implementation of TR Gate using GDI

TR gate is design using two NOT gate and two GDI cell shown in figure 10. Output expression for TR gate is (P=A, Q=A⨁B, R= (A'B ⨁C). Total 8 number of transistors required for its design. Power dissipation for TR is avg. power=1uW and max. delay is 10.1ns.

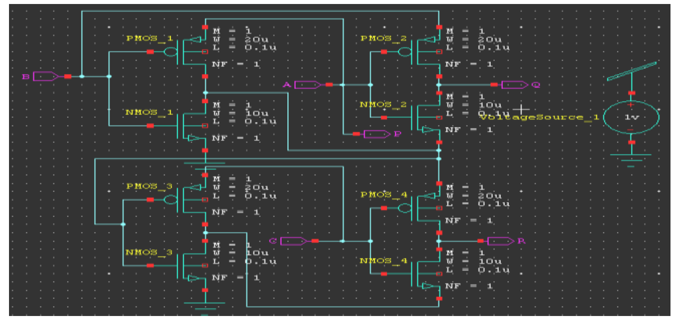


Fig. 10a) Design of TR Gate using GDI

Fig. 10 b) Simulation results for TR Gate using GDI

5. Proposed work

5.1 Transistor Design of Proposed Reversible Gate (RGG) using GDI cell

Proposed Reversible GDI Gate (RGG) is a two input two output gate. For implementation required two NOT gate and one GDI cell. Output P= (A xor B) & Q= (A xnor B). For GDI implementation required only 6 transistors as shown in figure 12. Power dissipation for Toffoli gate is 9.1327uW and MAX_DELAY is 9.9ns

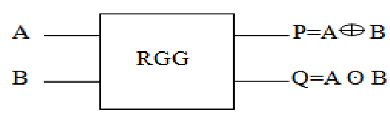


Fig. 11 Block representation of RGG

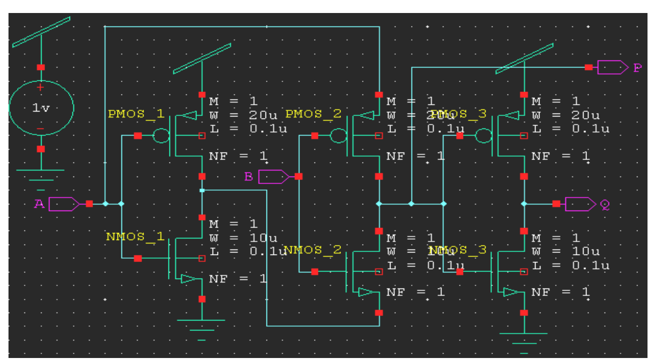


Fig. 12 Design of RGG using GDI cell.

Fig. 12b Simulation results for proposed RGG

5.2 Proposed Reversible GDI Gate2 (RGG2)

Reversible GDI Gate 2 (RGG2) is three input three output reversible gate. For design required one NOT and two GDI cell as shown in figure13. Total number of transistors required is 6. The outputs are defined by P=A, Q=(AC), R=(A'B+AC). Proposed single RGG2 can work as a 2:1 multiplexer.

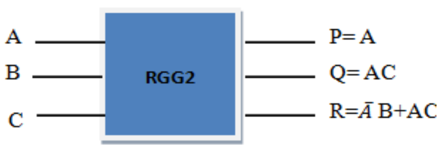


Fig. 13 Block representation of RGG2

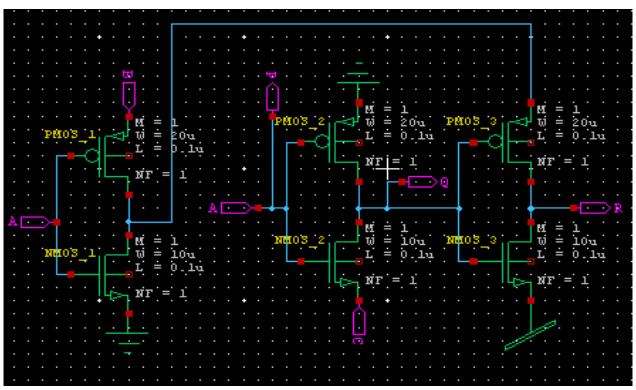


Fig. 13a) Transistor representation of RGG2

Fig. 13b) Simulation result of RGG2

5.3 Proposed Reversible GDI Gate1 (PRGG1)

PRGG1 is 3*3 reversible gate number of transistor required for design is 10. Output expression is shown in figure 14. and from simulation result output for all combination can be verified. From Measurement result summary found avg. power is 4.9183uW and max. delay is 9.9111ns

Fig. 14 Proposed design of PRGG1 gate using GDI

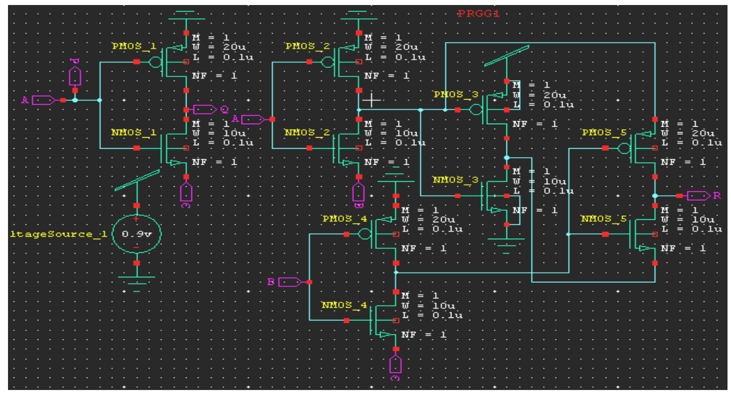


Fig. 14a) Transistor representation of PRGG1

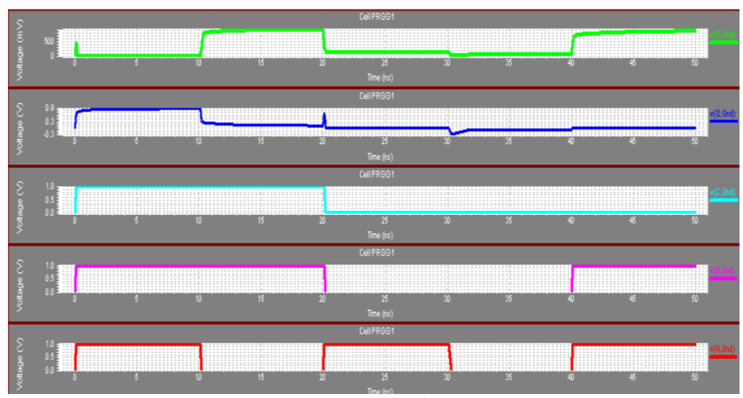


Fig. 14b) Simulation result of PRGG1

5.4 Design of full adder using proposed gate PRGG1

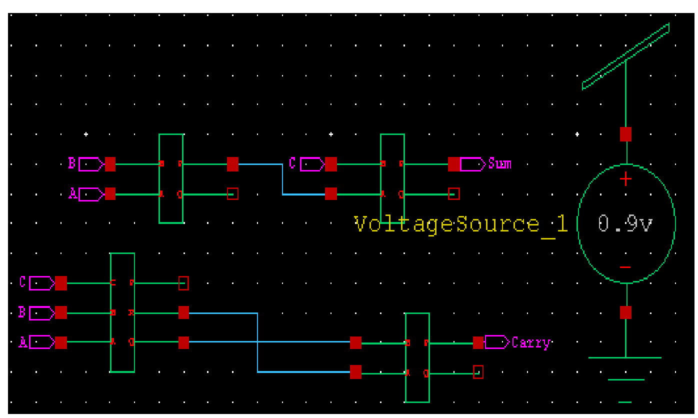


Fig. 15 a)Full Adder using proposed RGG and PRGG1 gate

GDI based Full Adder is designed using RGG and PRGG1as shown in figure 15. Only 4 gates are required for the design of full Adder. Total Transistor Count is 37, garbage output is 4, and Average Power dissipation is 10.305uW. And when compared with the existing design huge improvement in number of parameters.

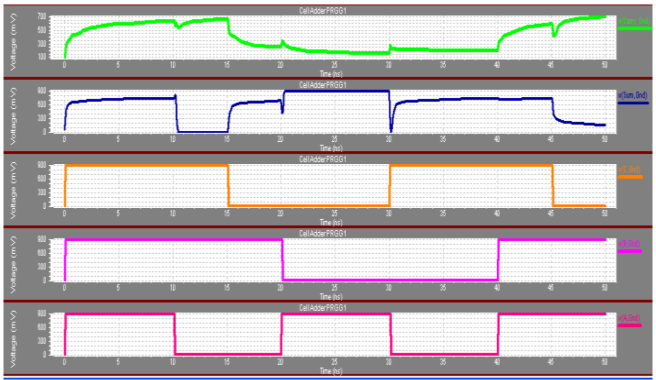


Fig. 15b) Full Adder using proposed RGG and PRGG1 gate

5.5 Design of 4:1 Multiplexer using proposed gate

4:1 Multiplexer block diagram using proposed RGG2 is shown in figure 16. For design required three RGG2 gate. For Proposed design average power is 1.9875uW, Garbage output 6, and transistor count is 18. Proposed design gives tremendous improvement for different parameter like power dissipation, Garbage output, transistor count with the existing design. Transistor implementation and Simulation result is shown in figure 17.

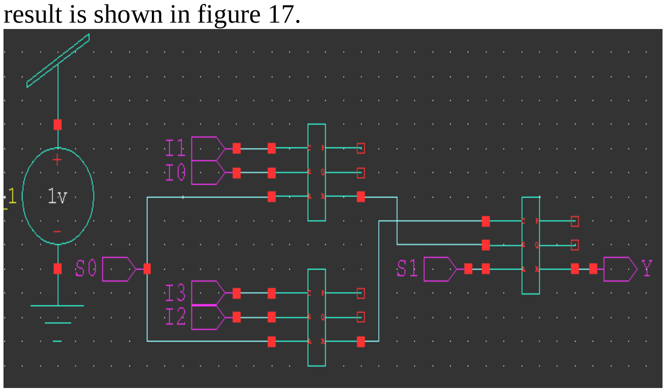


Fig. 16 Block representation of 4:1 Multiplexer using proposed RGG2

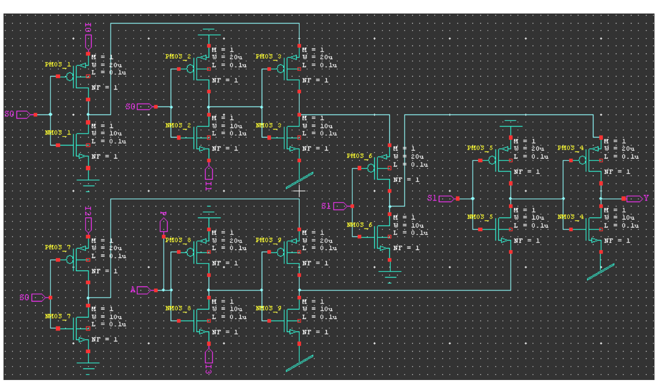


Fig. 17a) Transistor design of 4:1 Multiplexer using GDI

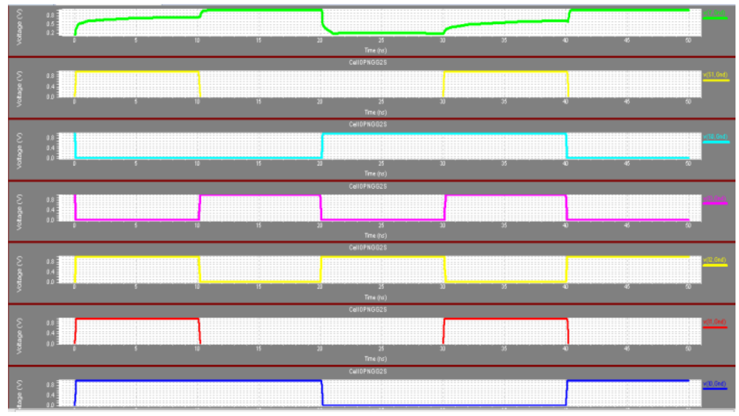


Fig. 17b) Simulation results for 4:1 Multiplexer

5.6 Design of reversible 1:4 Demultiplexer using proposed PRGG1 and Feynman Gate:

Whenever a single data needs to be transmitted to multiple devices, demultiplexer can send it to the intended devices. Block Representation of 1:4 Demultiplexer is shown in figure18 and its truth table is given in table 2.

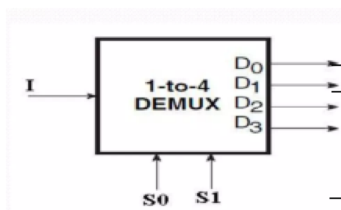


Fig. 18a) Block Representation of 1:4 Demultiplexers

Table: 2 Truth table for 1:4 Demultiplexer

S0	*S1*	*I*	*D0*	*D1*	*D2*	*D3*
0	*0*	*1*	*1*	*0*	*0*	*0*
0	*1*	*1*	*0*	*1*	*0*	*0*
1	*0*	*1*	*0*	*0*	*1*	*0*
1	*1*	*1*	*0*	*0*	*0*	*1*

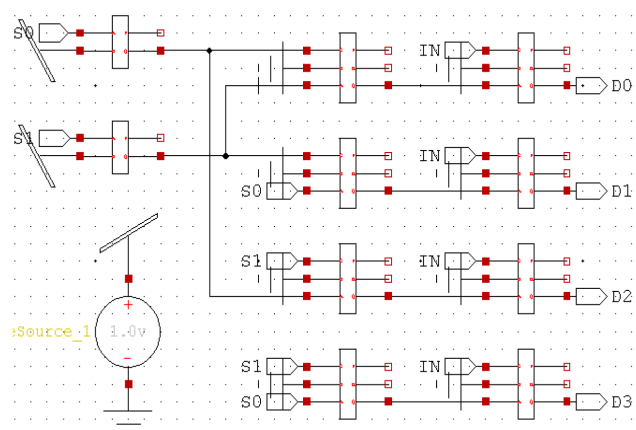


Fig. 18b) Implementation of 1:4 Demultiplexer using proposed PRGG1 and Feynman Gate

For the implementation of1:4 Demultiplexer using proposed PRGG1 and Feynman Gate are used. For inverting the input bit Feynman gates are used and for implementing the output equation: D0=IS0'S1', D1=IS0'S1, D2=IS0S1', D3=IS0S1 PRGG1 gates are used.

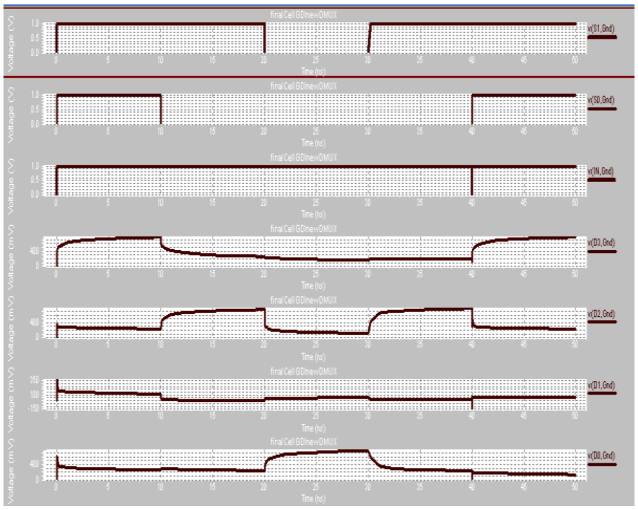


Fig. 18c) Simulation of 1:4 Demultiplexer using proposed PRGG1 and Feynman Gate

5.7 Reversible Logic 4-Bit Magnitude Comparator using GDI technique

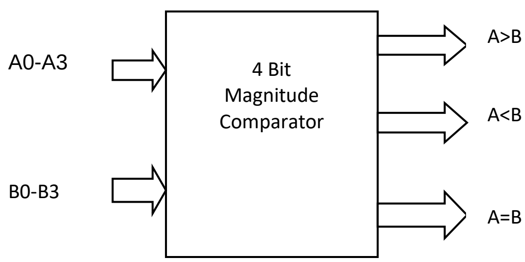


Fig. 19 Block diagram of 4-bit magnitude comparator

Block schematic of 4-bit magnitude comparator is shown in figure 19. Condition for Greater than (A>B), Less than (A<B) and Equal (A=B) are shown and the equation for the same are written based on the condition.

Step 1: Condition for A greater than B (A>B)
When A3=1 and B3=0,
When A3=B3 and A2=1 and B2==0
When A3=B3 and A2=B2 and A1==1 and B1=0
When A3=B3 and A2=B2 and A1==B1 and A0=1 and B0=0

Step 2: Condition for A Less than B (A<B)
When A3=0 and B3=1,
When A3=B3 and A2=0 and B2==1
When A3=B3 and A2=B2 and A1=0 and B1=1
When A3=B3 and A2=B2 and A1==B1 and A0=0 and B0=1

Step 3: Condition for A Equal to B (A=B)
When A3=B3 and A2=B2 and A1==B1 and A0=B0

$$A>B \rightarrow A3\,\overline{B3}+(A3\odot B3)A2\,\overline{B2}+(A3\odot B3)(A2\odot B2)A1\,\overline{B1}+(A3\odot B3)(A2\odot B2)(A1\odot B1)A0\,\overline{B0} \quad (1)$$

$$A<B \rightarrow \overline{A3}\,B3+(A3\odot B3)\ \overline{A2}\,B2+(A3\odot B3)(A2\odot B2)\ \overline{A1}\,B1+(A3\odot B3)(A2\odot B2)(A1\odot B1)\ \overline{A0}\,B0 \quad (2)$$

$$A=B \rightarrow (A3\odot B3)\ (A2\odot B2)\ (A1\odot B1) \quad (3)$$

Equation 1, 2 and 3 are implemented using condition given in step 1, 2 and 3 for A greater than B, A less than B, A equal to B respectively. Design of 4-Bit Magnitude Comparator using proposed RGG and combination of Toffoli Gate and GDI cell shown in figure 19a. The gate count for design is 4 RGG, 9 Toffoli gates, 14 GDI cell required for comparator design.

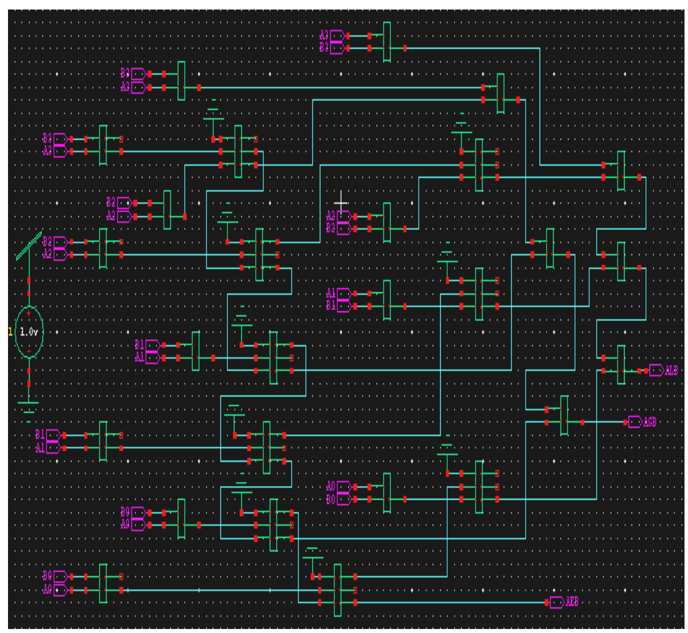


Fig. 19a) Block Schematic of 4 Bit reversible Magnitude Comparator using RGG and Toffoli Gate

From simulation result shown in figure 19c can be verified for first column, from down to up direction, for input bit pattern A0=0, A1=0, A2=0 A3=0 and B0=1, B1=1, B2=1, B3=1 output A< B is active high. So likewise, it can be verified for any combination of bit pattern.

5.8 Design of 8:3 Reversible Encoder using GDI Technique:

Encoder is a digital circuit that produces a binary output code depending on which of its inputs are activated. It has maximum of 2n input lines and n output lines. 8:3 Encoder is design using the proposed RGG gate. Block schematic is shown in figure 20. D0 to D7 are inputs and A0 to A1 are outputs. 8 RGG gates are used for construction. Output expression for 8:3 Encoder are given as: A0=D4+D5+D6+D7, A1=D2+D3+D6+D7, A2=D1+D3+D5+D7.

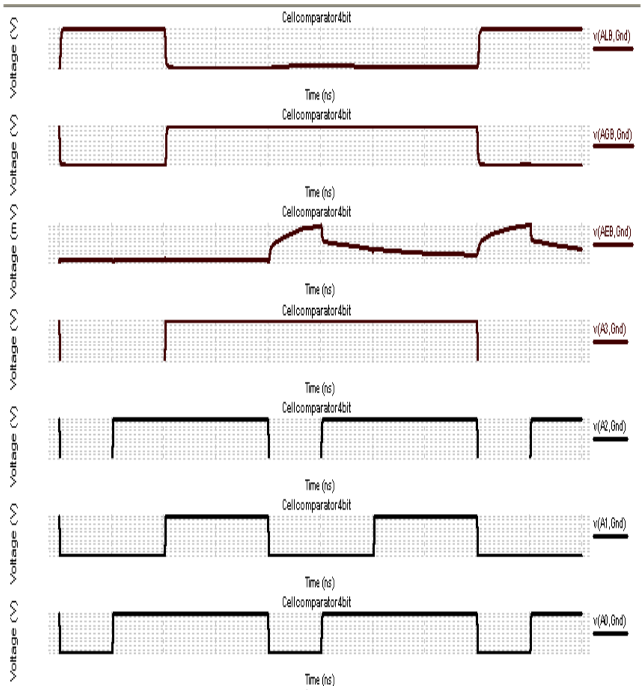


Fig. 19b) Simulation result for 4 Bit Magnitude Comparator Comparator using RGG and Toffoli Gate.

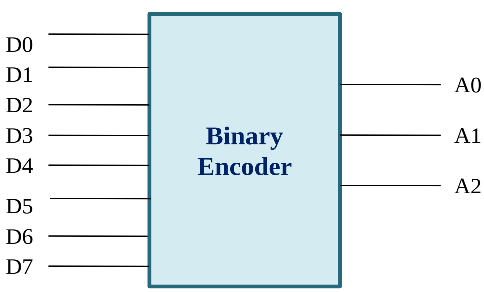


Figure 20 Block diagram of 8:3 binary Encoder

Table: 31 Truth Table for 8:3 Binary Encoder

Input								Output		
D7	D6	D5	D4	D3	D2	D1	D0	A0	A1	A2
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	1	0	0	0	1	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	0
0	0	1	0	0	0	0	0	1	0	1
0	1	0	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	0	1	1	1

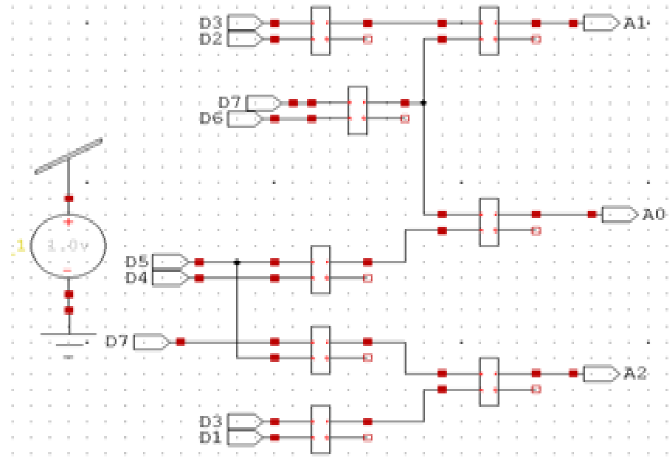


Fig. 20a) Implementation of GDI based 8:3 reversible Encoder using RGG

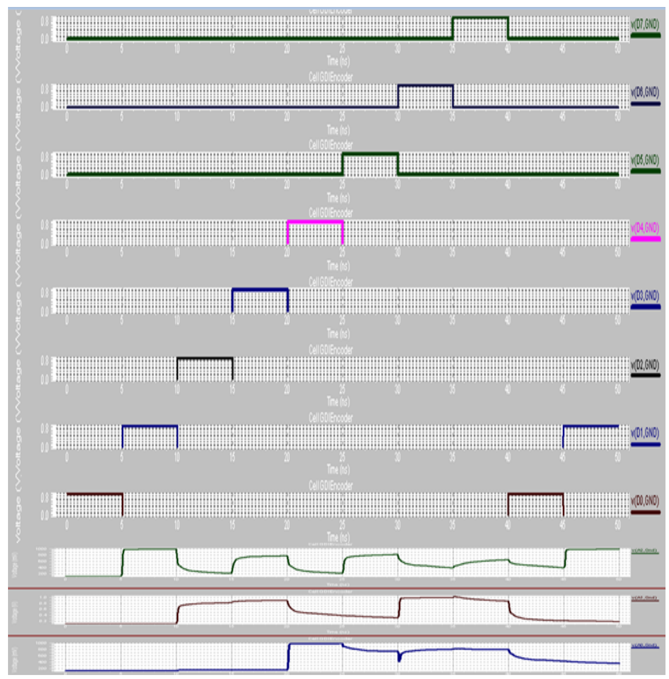


Fig. 20b). Simulation result for GDI based 8:3 reversible Encoder using RGG

5.8 Design of GDI based Reversible 4:16 BCD to Decimal Decoder using Toffoli and PRGG1 Gate

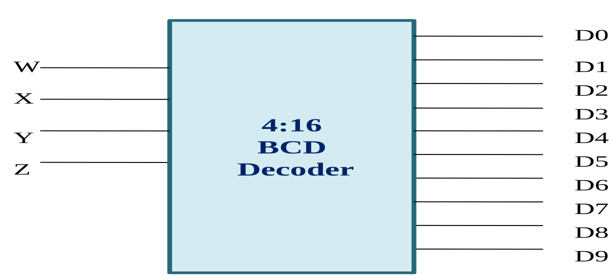


Fig. 21 Block schematic of GDI based 4:16 BCD to Decimal Decoder

Table: 4 Excitation table for 4:16 BCD to Decimal Decoder

Input				Output									
W	X	Y	Z	D9	D8	D7	D6	D5	D4	D3	D2	D1	D
0	0	0	0	0	0	0	0	0	0	0	0	0	1
0	0	0	1	0	0	0	0	0	0	0	0	1	0
0	0	1	0	0	0	0	0	0	0	0	1	0	0
0	0	1	1	0	0	0	0	0	0	1	0	0	0
0	1	0	0	0	0	0	0	0	1	0	0	0	0
0	1	0	1	0	0	0	0	1	0	0	0	0	0
0	0	1	0	0	0	0	1	0	0	0	0	0	0
0	1	1	1	0	0	1	0	0	0	0	0	0	0
1	0	0	0	0	1	0	0	0	0	0	0	0	0
1	0	0	1	1	0	0	0	0	0	0	0	0	0

A decoder is a combinational circuit that converts n bits of binary information of input lines to a maximum of 2^n unique output lines. Usually, decoders are designated as an n to m lines decoder, where n is the number of input lines and m (2^n) is the number of output lines. Block schematic of GDI based 4:16 BCD to Decimal Decoder is shown in figure 21. Output equation from excitation table is given as D0=W'X'Y'Z', D1=W'X'Y'Z, D2=X'YZ', D3=X'YZ, D4=XY'Z', D5=XY'Z, D6=XYZ', D7=XYZ, D8=WZ', D9=WZ.

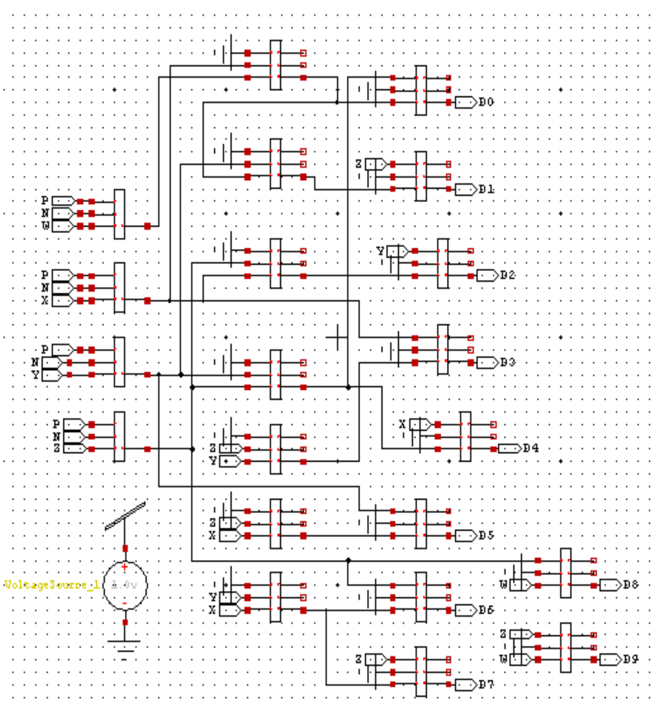


Fig. 21a). Implementation of GDI based 4:16 BCD Decoder using Toffoli and RGG2

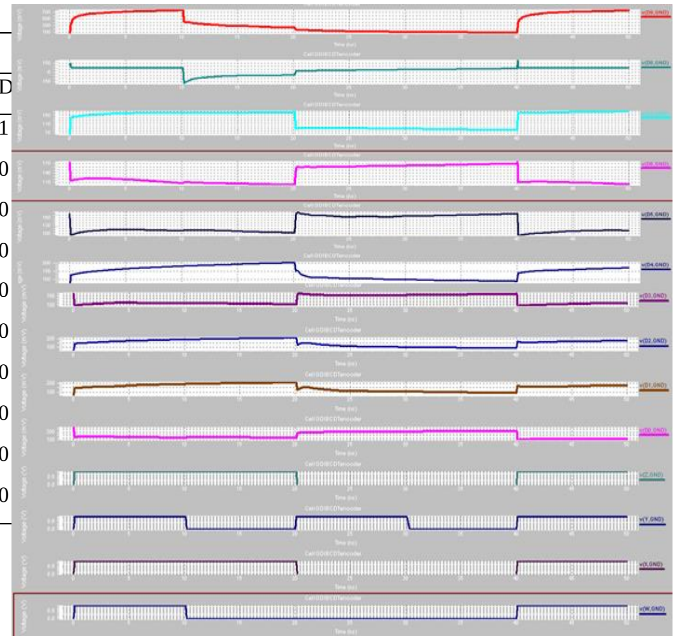


Fig. 21b). Simulation result of GDI based 4:16 BCD Decoder using Toffoli and RGG2

6. Result and Discussion

This research paper describes the insertion of GDI technology in reversible logic circuit design which enhances power efficiency and minimizes circuit complexity. Transistor implementation of many basic gates such as Feynman, Toffoli, Peres Gate using GDI is proposed here and its performance are evaluated for different transition period. Three new reversible GDI gates are proposed such as RGG, RGG2, PRGG1 and simulation done for 50ns transition time. For proposed gate it is verified from simulation that very less power consumption and less number of transistors required for construction. Single RGG2 gate can perform 2:1 multiplexer. For the design of RGG2 required transistor count is 6, number of gate1, garbage output is 2 and power dissipation 0.18646uW it gives improvement when compared with the [29]. For the design of PRGG1 number of transistors required is 10 and Measurement result summary found avg. power 4.9183uWand max. delay 9.9111ns. Comparative analysis for 4:1 Multiplexer, 1:4 Demultiplexer are given in Table 5 with the existing design. PRGG1 and Feynman gates are used for the design of 1:4 Demultiplexer design and performed its simulation. Results are verified with the existing design. Proposed design for Demultiplexer found the improvement in power dissipation and the number of transistors required.

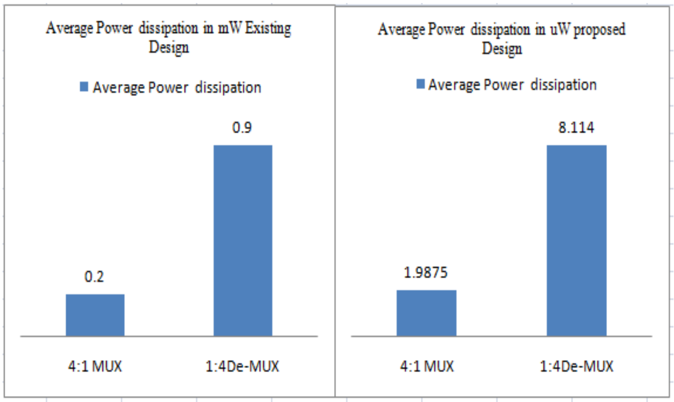


Fig. 22. Graphical representation of average power for Multiplexer, Demultiplexer for Existing and proposed design.

Figure22 shows the graphical representation of average power dissipation for Multiplexer, Demultiplexer for existing and proposed design. Comparison of multiplexer design with the existing design are performed for different parameter such as garbage output, Gate count and Transistor count. These results found tremendous achievement over power dissipation Transistor count and garbage output for 4:1multiplexer and Demultiplexer.

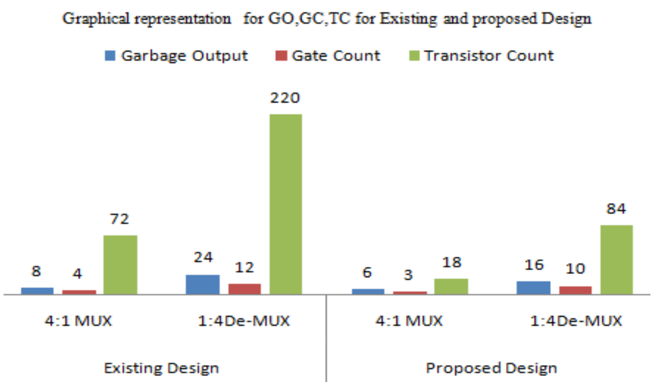


Fig. 23 Graphical representation of Multiplexer, Demultiplexer for existing and proposed design for different parameter.

Extensive research related to this topic describes how proposed gate can be used for the construction reversible 4-bit magnitude comparator.

Performance analysis of 4-bit reversible magnitude comparator is shown in Table 6. Measurement result summary for given 4 bit magnitude comparator shows that avg. power is 3.4148mW, max. delay is 10.10ns. Proposed design given in this research paper gives better performance for the construction of all circuits using GDI technique.

Table 6. Performance of 4-bit reversible magnitude Comparator

4 bit Magnitude Comparator	AI (Constant Input)	NOG (Number of Gate required)	GO (Garbage output)
Proposed Design	09	27	16
Existing design 1 [9]	11	18	16
Existing design [13]	18	14	16
Existing design [14]	20	16	17
Existing design [33]	21	32	18
Existing design [34]	59	53	23
Existing design [35]	14	12	13

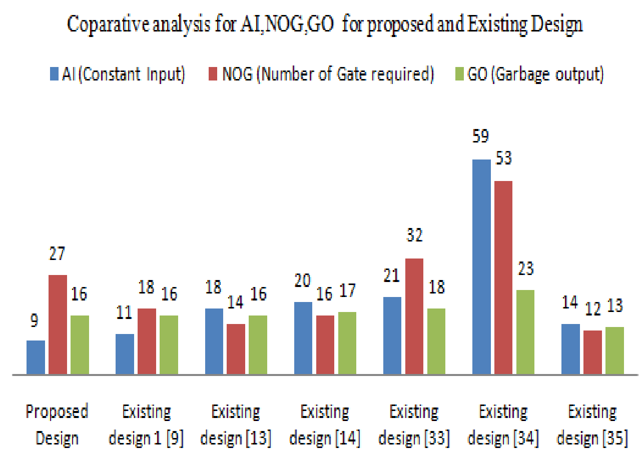


Figure 24.Comparative analysis for 4 Bit Magnitude Comparator

Design of 8:3 Reversible Encoder using GDI Technique is proposed using RGG gate and compared the result with the existing circuits. as shown in table 7.

Table 7. Performance analysis for Encoder and BCD decoder design.

Existing Design	Proposed Design

Table 5: Comparative analysis for Full adder, 4:1 Multiplexer, 1:4 Demultiplexer

	Existing Design			Proposed Design		
Parameter	FullAdder using GDI	4:1 MUX	1:4 De-MUX	Full Adder using GDI	4:1 MUX	1:4 De-MUX
Average Power dissipation	51uW[28]	0.2 mW [29]	0.9mW [29]	10.305uW	1.9875uW	8.1184uW
Garbage Output	-	8 [29]	24[29]	4	06	16
Gate Count	8 [28]	4[29]	12 [29]	4	3	10
Transistor Count	-	72 [29]	220 [29]	37	18	84

Parameter	8:3 Encoder	4:16 BCD Decoder	8:3 Encoder	4:16 BCD Decoder
Average Power dissipation	3.753uW [32]	1.938084 uW [36]	3.2847uW	1.9012 uW
Garbage Output	12 [32] 15[4]	17[32] -	8 -	34 -
Gate Count	8[32] 10[4]	17[32] -	8 -	21 -
Transistor Count	-	-	72	-

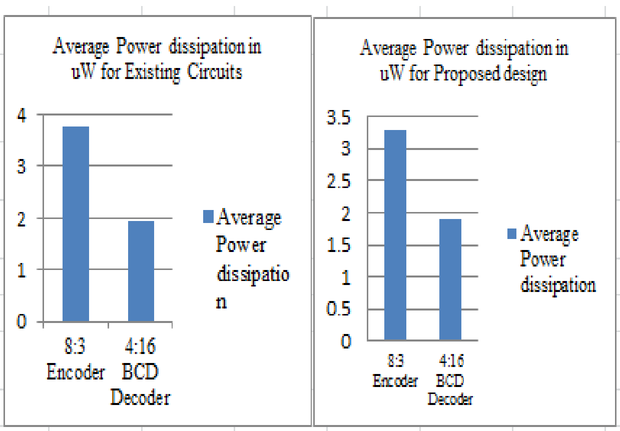


Fig. 25 Graphical representation for Encoder and BCD decoder design for average power dissipation.

7. Conclusion

In this research work design of Reversible logic circuits using GDI technique is proposed. Proposed GDI based new reversible gates likes RGG, RGG2, PRGG1 which required less number of transistors for implementation of logic function. GDI based Full Adder is design using RGG and PRGG1gate. Propose design of 4:1 Multiplexer using RGG2 is demonstrate and the power dissipation is 1.9875uW when compare with [29]. Design a reversible 1:4 Demultiplexer using proposed PRGG1, Feynman Gate and performed the power analysis. Power dissipation for proposed design is 8.1184uW when compared with [29] found the huge improvement of power dissipation using proposed design. GDI based 4-bit reversible magnitude comparator design using 4 RGG, 9 Toffoli gate, 14 GDI cell. Design is compared for different parameter such as AI (Ancilla Input), NOG (Number of Gate require) GO (Garbage output). From Table 6 it is found that propose 4-bit comparator design using GDI is better for AI when compared with [9], [13-14], [33-35]. For Number of Gate required for design show remarkable advancement when compared with [33-35]. 8:3 Encoder is design using the proposed RGG gate. Proposed design gives great improvement for garbage output and gate count when compared with [4], [32]. BCD to Decimal decoder is design using a proposed Toffoli gate and RGG gate and comparative analysis is showed in table7. Executed circuits designs outcome demonstrates that the circuits are more optimal for supply voltage of 1V. The GDI technique is the most efficient method for reducing the delay, leakage power and circuits power consumption. The performance of the suggested reversible multiplexer and comparator is superior to that of other reversible circuit present in the literature. Performance analysis for Encoder and BCD decoder design is given in table7 and shows the improvement over power dissipation.

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