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Original Article

Modular Three-Phase High Step-Up Converter with Switched Capacitors for EV Charging with Improved Power Quality

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Abstract *- Environmental awareness, coupled with tightening regulations regarding greenhouse emissions, is putting pressure on the automotive industry to shift towards sustainable propulsion methods, with vehicle electrification emerging as a feasible solution for effective CO_2 reduction. As Battery Electric Vehicles (BEVs), Hybrid Electric Vehicles (HEVs), and Plug-In Hybrids (PHEVs) find their place in the market, standardization efforts by international organizations such as SAE, CHAdeMO, and IEC have been made in developing charging standards; however, the grid-scale adoption of EVs poses significant challenges in terms of harmonic generation, increased peaks in demand, and voltage fluctuation at the point of supply. High-speed charging beyond 150 kW entails the use of highly efficient step-up AC-DC converters that also adhere to IEC 61000-3-2 harmonic limits. These requirements are not easily met by existing rectification techniques, including the traditional single-stage three-phase rectifier topology, Modular Multilevel Converter, and Vienna Rectifier, all of which face trade-offs between increased circuit complexity, component costs, current imbalance, and power losses. In this paper, a three-phase modular switched-capacitor Power Factor Correction (PFC) converter that generates an output voltage of 1600 V from a 230 V AC per-phase supply is presented. The proposed converter consists of three phases, each containing a full-wave rectifier bridge, two boost inductors, one active switch, and a three-level switched capacitor voltage multiplier. The phase modules operate in quadrature relative to each other to ensure symmetrical input currents. The switched capacitor-based configuration reduces the voltage stress across the devices to a small portion of the output level. This translates to reduced device costs and thermal management issues compared to existing PFC topologies. Dual-loop average current control architecture is adopted to provide regulation of the DC bus voltage and power factor correction through input current shaping. The simulation results obtained in MATLAB/SIMULINK prove that the output current waveform produced by the converter contains very little harmonics with the total harmonic distortion being only 5.38% when considering the fundamental value of 18.63A, which conforms to the limit imposed by IEC 61000-3-2. The output voltage shows good regulation with a constant value of 1600V under steady-state and dynamic load variations. Hardware testing of the designed converter on the Opal-RT system has verified the results from the computer simulations. It can be concluded that the developed converter is applicable for high-power electric vehicle fast charging stations.*

Keywords *- High Voltage Gain, Modular Three-Phase Converter, Switched Capacitor Topology, Power Factor Correction (PFC).*

1. Introduction

The trend towards clean transportation has gathered momentum over the last ten years due to stringent restrictions on emissions and an increasing concern for air quality in cities. Battery electric vehicles have proven to be the most effective solution in this regard, owing to the fact that they generate zero tailpipe emissions and, when powered from an electrical grid that uses even partial renewable energy sources, result in considerable reductions in carbon dioxide emissions through the entire life cycle of the battery [1]. The international efforts to develop standards have been able to keep up with technological advancements in this field; IEC 61851 now outlines the AC.

Moreover, DC charging procedures for maximum powers ranging from 3 kW up to 240 kW, and organisations like SAE and CHAdeMO have developed the standards for interoperability among vehicles and charging infrastructure from different vendors [2-4]. The number of electric vehicles connected to the distribution grid has increased in many areas to such an extent that their total charging power is beginning to show up in grid design calculations. Charging at times of peak consumption may lead to voltage variations, accelerated aging of the transformer and effects feeder with harmonic content [5]. Local energy storage, vehicle-to-grid and smart charging have been considered methods for lessening the effects of EVs on the electrical grid [6].

Battery degradation adds another facet to the question of grid infrastructure. Batteries lose capacity with each charge and discharge cycle; in general, a pack used in an electric vehicle loses about 30 percent of its capacity during about ten years of use [7]. Even when batteries reach their point of obsolescence for vehicle applications, they still retain much of their capacity to store energy, and reusing the packs as stationary power storage at fast charging stations is a strategy for reducing peak loads and extending battery life at the same time [8, 9]. However, nothing about this mitigates the basic problem facing potential consumers. Range anxiety and lengthy recharge times are consistently cited as the two top reasons for not purchasing an EV, and improving both requires higher power charging [10]. Increasing the voltage rating of a vehicle platform to 800 volts or more enables faster charging by lowering the current required in a cable with a reasonable conductor diameter for the same amount of power [11]. Thus, a large step-up conversion ratio is necessary to produce adequate voltage from the source power while maintaining input currents of minimal distortion.

Similar requirements for large step-up gains together with controlled input currents apply in numerous industrial and laboratory settings. X-ray machines, radar transmitters, and vacuum processing apparatuses all require well-regulated power supplies at relatively high DC voltages. All three of these types of equipment are subject to standards like IEC 61000-3-2, which set upper bounds for the amount of harmonics introduced by a device [12]. Compliance without the aid of bulky filters requires shaping of the input currents drawn by the device, which is why power factor correction is an absolute requirement in this class of equipment.

Conventional topologies for three-phase AC-to-DC conversion have been extensively studied. Single-stage three-phase boost rectifiers are space efficient and offer acceptable voltage gain; however, active switches face the entire output voltage, necessitating the employment of high-voltage switches with relatively slow switching speed and large conduction losses [13]. In the Vienna configuration [14], when the switch is OFF, the appeared voltage with be half the output voltage. In a modular approach, the use of three single-phase boost converter modules in parallel and 120° phase difference reduces the rated power of each module, potentially lowering input current ripples by canceling some portions of ripples between phases [15]. Previous modular systems faced the problem of input current imbalance for four-wire systems, and certain configurations created harmonic distortion at the source terminals due to interactions among the modules, although the more advanced designs have since corrected these issues. Low switching stress and near unity power factor are the advantages of multilevel converters and Vienna rectifiers; however, the number of components and control circuitry scales up drastically as the desired output voltage rises [16].

A switch-capacitor voltage multiplier offers another route toward high voltage gain. In contrast to the previous method, which requires an inductor to be operated at a high duty ratio and thus compromises efficiency and control performance, the voltage multiplier consists of capacitors that multiply the voltage across a moderately-gained boost stage by summing the capacitor voltages in series during the discharge cycle [16]. The pure switched-capacitor converter draws pulsed input currents and provides no regulation on its own; however, coupling a boost inductor with the switched-capacitor network enables continuous input currents and recovers the closed-loop frequency bandwidth to satisfy harmonic requirements.

Three-phase PFC and modular converters proposed were with conventional boost converters that cannot provide the high gain needed for the required voltage of 800 V for charging EV', with a bus voltage of 1600V from a 230 V supply. These have drawbacks that cause more stress across active elements because of the parasitic effect, and they need to operate at a high duty ratio, which may result in degradation of performance. Whereas Vienna rectifiers and multilevel converters require more components and will raise the cost. Therefore, the switched capacitor can generate the required voltage with less stress on components. However, for high power, three-phase converters are required. With modular converters continuous supply can be provided for charging EV's. Therefore, the proposed solution allows obtaining high gain and considerably reducing the voltage stress experienced by the active switch, which becomes crucial for kilovolt-level output operation.

This work proposes a three-module modular AC-DC PFC converter whose modules are designed using the single-switch switched-capacitor boost topology. Each module consists of a full-wave bridge rectifier, two boost inductors, one MOSFET active switch, and a switched capacitor network with three capacitors. The three modules have a 120° offset in their operation and have a shared DC output bus that works at 1600V from the per-phase supply of 230V. The average current control strategy applied to the three-phase system ensures that the output voltage is maintained for varying loads and that the phase currents are sinusoidal to maintain a unity power factor. Most importantly, the switch will experience less stress, which is reduced by a factor of (Vo/(2+D)), where Vo is the output voltage, and D is the duty ratio. This makes it possible to use lower voltage devices. The effectiveness of the converter is simulated in MATLAB/SIMULINK and validated using an Opal-RT real-time environment.

The remainder of the paper is organized as follows. Section II introduces the circuit topology and the operating modes of one phase of the converter. Section III analyzes the converter under steady-state conditions, presenting the voltage gain and capacitor voltages based on volt-second and charge balance considerations. Section IV details the dual-loop average current control strategy.

Section V discusses the simulation and hardware-in-the-loop results, and Section VI summarizes our findings.

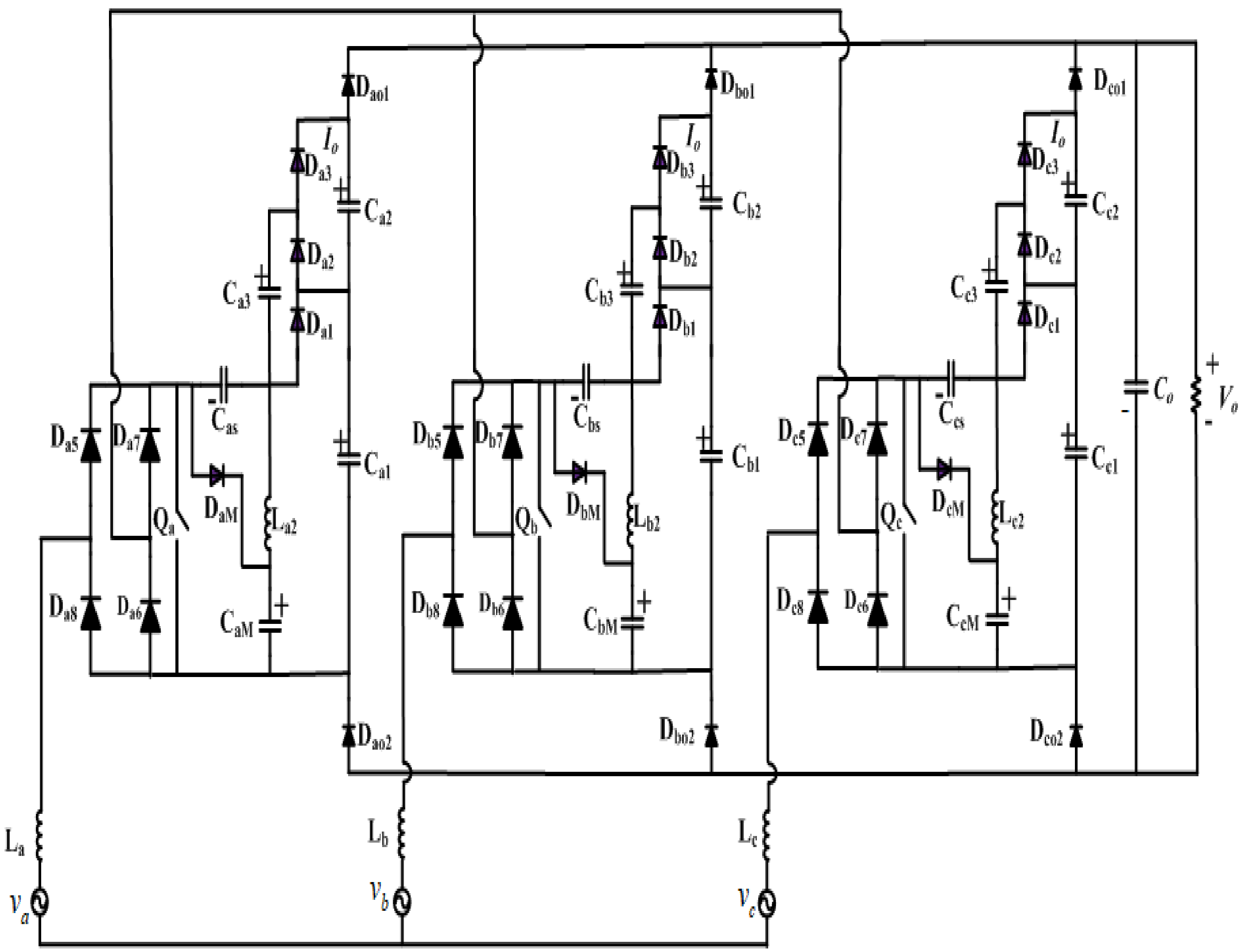


Fig. 1 Proposed Three-Phase modular converter

2. Literature Review

The conversion of three-phase AC power into a high-voltage DC bus while maintaining a high power factor has attracted significant research attention over the past decade. This section reviews the major converter topologies relevant to the proposed work, discusses their limitations, and highlights the research gap that motivates the present study.

Single-stage three-phase boost rectifiers are among the simplest solutions for AC–DC conversion with power factor correction. These converters [13] offer a compact and straightforward implementation; however, all active switches must withstand the full DC output voltage. In applications requiring a 1600 V DC output, this necessitates the use of 1700 V-class IGBTs, which typically suffer from slower switching speeds and higher conduction losses, thereby limiting overall efficiency at elevated power levels.

The Vienna rectifier [14] addresses the unity power factor and the OFF switch voltage nearly half of the output voltage; it is restricted in voltage gain and requires a voltage balance control loop, which makes the circuit complex. To address these limitations, modular converter architectures have been proposed, where three single-phase boost converter modules operate in parallel with a 120° phase shift. This arrangement reduces the power handled by each module and minimizes input current ripple through interleaving [15]. A PFC converter in modular configuration operating in Continuous Conduction Mode (CCM), achieving superior harmonic performance compared with conventional single-stage configurations. Nevertheless, because these systems are still based on traditional boost converters, each switch remains exposed to the full output voltage. As a result, achieving high voltage gain while maintaining high efficiency remains challenging.

Topologies related to Multilevel converter, such as the Neutral-Point-Clamped (NPC) converter and the Vienna Rectifier, overcome this issue by distributing the output voltage across multiple semiconductor devices. These converters are capable of achieve power factor of almost unity and low harmonic distortion. However, [13], their component count, balancing requirements, and gate-drive complexity increase substantially with higher output voltage levels, making them less attractive for compact and cost-effective high-voltage applications.

Switched-Capacitor (SC) voltage multiplier circuits have emerged as an attractive alternative for achieving high voltage gain without requiring boost converters to operate at extreme duty cycles. [16] presented a cascaded three-phase symmetrical voltage multiplier that generates a high output voltage by connecting capacitor voltages in series during discharge intervals. A key advantage of this approach is that each switch and diode experiences only a fraction of the total output voltage, enabling the use of lower-voltage devices with faster switching characteristics and lower losses. However, standalone SC converters inherently draw pulsating input currents and do not provide natural output voltage regulation. Consequently, they are typically combined with boost-inductor stages to ensure continuous input currents and facilitate closed-loop control.

Recent developments in EV fast-charging infrastructure have further increased the demand for power converters capable of interfacing 230 V three-phase AC supplies with emerging 800-1000 V battery platforms. Such systems generally require DC bus voltages in the range of 1200–1600 V [10, 11].

Despite considerable progress in converter design, existing topologies are unable to simultaneously satisfy several key requirements: (a) a voltage gain greater than 6:1 from a 230 V AC source, (b) switch voltage stress below 50% of the output voltage, (c) input current THD below 8% in compliance with IEC 61000-3-2 without relying on bulky passive filters, and (d) a modular and scalable architecture. The proposed converter addresses these challenges by integrating switched-capacitor voltage multiplication, interleaved modular operation, and dual-loop average current control within a unified topology.

3. Operation of the Proposed Converter Configuration

The modular three-phase PFC converter used in this work is illustrated in Figure 1. In this configuration, every component experiences a voltage stress of only half the output voltage. The proposed configuration achieves a higher voltage gain compared to the conventional three-phase boost PFC converter and the Vienna rectifier. Another advantage is that it can operate without requiring a neutral connection from the source. The operating principle of this three-phase converter closely follows the approach as described. The proposed high-gain non-isolated DC-DC converter employs a single active switch in conjunction with Switched Capacitor (SC) cells to achieve substantial voltage amplification, making it suitable for applications involving low-voltage sources such as photovoltaic panels or fuel cells. When functioning in the Continuous Conduction Mode (CCM), the converter operates without interruptions, providing continuous current flow through both inductors, which results in increased efficiency and decreased input current ripple. When the switch is ON, inductors Lx1and Lx2 extract energy from the input supply, and the capacitor Cx3 is being charged through the diode Dx2. Once the switch is OFF, the energy stored within Lx1 is transferred to capacitor CM whilst Lx2 charges capacitor Cx1. Meanwhile, capacitors Cx2 and Cx3 are discharging in parallel, contributing towards the output voltage. Considering the per-voltage as:

When treating the phase voltages applied to the converter input as:

$$V_a = V_p \sin(\omega t)$$
$$V_b = V_p \sin(\omega t - 120°) \tag{1}$$
$$V_c = V_p \sin(\omega t + 120°)$$

and phase currents as

$$i_a = I_p sin(\omega t)$$
$$i_b = I_p\ sin(\omega t\ -\ 120°) \tag{2}$$
$$i_c = I_p\ sin(\omega t + 120°)$$

Making these equations as per each phase, they can be generalized as follows.

$$V_x =\ V_m\ \sin(\theta - \theta_x)\ \ Where\ x\ is\ a.b.c \tag{3}$$

The steady state equations during the ON state and the OFF state are respectively as

$$0 = DV_x + (1 - D)(V_x - V_{xM}) \tag{4}$$

$$0 = D(V_{XC} - V_{CxM}) + (1 - D)(V_{x1} - V_{CxM}) \quad (5)$$

Applying KVL equations,

$$V_{x1} = V_x(\frac{1+D}{1-D}) \quad (6)$$

$$V_{x2} = V_{x3} = V_x(\frac{1}{1-D}) \quad (7)$$

$$V_o = V_{x1} + V_{x3}$$

$$V_o = V_x(\frac{2+D}{1-D}) \quad (8)$$

The inductor and capacitors are designed based on

$$L_x = \frac{V_x D}{2\Delta I_{Lx} F_{sw}} \quad (9)$$

$$c_x = \frac{I_o}{2\pi f_{ac} \Delta V_o} \quad (10)$$

The average current through the capacitor and the diode is given by

$$Ic_{a,avg} = \frac{1}{T_s}[i_{cj}^{ON} dT_s + i_{cj}^{OFF}(1 - d)T_s = 0\ j \in \{1,2,3\} \quad (11)$$

$$Id_{a,avg} = I_0 = \frac{1}{T_s}[i_{Dj}^{ON} dT_s + i_{Dj}^{OFF}(1 - d)T_s = \frac{i_{Lx}\cdot(1-D_x)}{2} j \in \{1,2,3\} \quad (12)$$

Based on the above equations, the instantaneous values of currents through the capacitor and the diodes are mentioned in Table 1. The average values are represented in Table 2. The rms expression of each element is tabulated in Table 3.

With this operation, the voltage across each of the switches, diodes and capacitors is minimized to (Vo/(2+D)). It permits utilising lower voltage ratings for these components, which leads to a greater degree of overall reliability for the converter.

Also, the converter architecture allows for a modular way to increase the voltage gain of the converter through the addition of more SC cells without having to add any additional active switches, which therefore maintains the simplicity of the circuit as well as keeping its size compact.

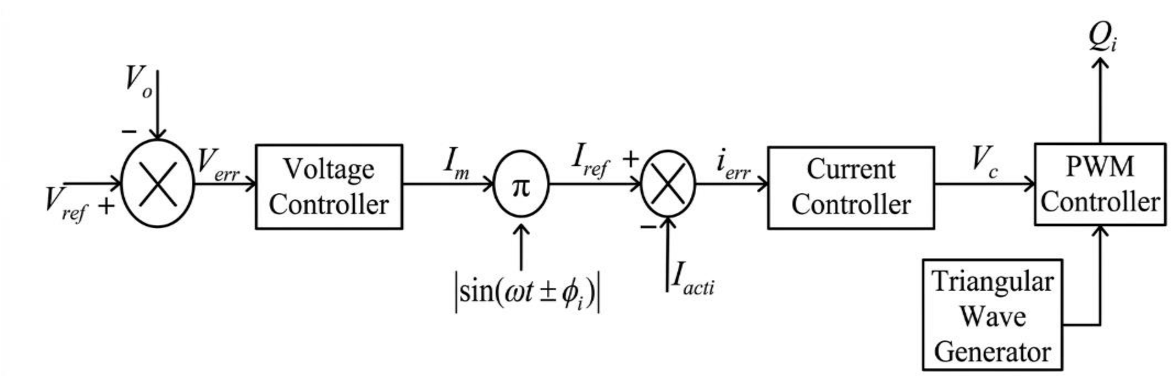


Fig. 2 Average current control method

4. Control Method

This section describes the average current control strategy used in the modular three-phase PFC converter in Figure 2. The control system consists of two loops. They are a voltage loop and a current loop. The outer one is a voltage loop, and the inner one is a current loop. The outer voltage loop compares the output voltage Vo with the reference voltage Vref to generate the error signal Verr.

This error is used to generate a sinusoidal reference current Iref synchronized with the input voltage. The current loop compares the actual inductor current Iact with Iref. Based on this comparison, a control voltage Vc is generated.

The control voltage is applied to a PWM controller using a triangular carrier waveform. The PWM controller produces the switching signal Vs for the main power switch.

This method ensures near-unity power factor, low THD, and stable output voltage. Based on Figure 2, the voltage error is given as

$$V_{err} = V_{ref} - V_o \quad (13)$$

The reference current is given as

$$I_{ref} = I_m \cdot |\sin(\omega t + \phi)| \quad (14)$$

Current error is

$$I_{err} = I_{ref} - I_{act} \quad (15)$$

The PI controller is

$$V_c(t) = K_p . I_{err}(t) + K_i \int I_{err}(t) dt \quad (16)$$

Table 1. Instantaneous values of device currents (per phase x) over switching period and line period

Element	On	Off
Dx1	0	$\frac{I_{Lx}}{2}$
Dx2	$\frac{I_{Lx}}{2}$	0
Dx3	0	$\frac{I_{Lx}}{2}$
Dxm	0	$\frac{I_{Lx}}{2}$
Cx1	$\frac{-I_{Lx}(1-d)}{2d}$	$\frac{I_{Lx}}{2}$
Cx2	$\frac{-I_{Lx}(1-d)}{2d}$	$\frac{I_{Lx}}{2}$
Cx3	$\frac{-I_{Lx}(1-d)}{2d}$	$\frac{+I_{Lx}(1-d)}{2d}$
CxM	$\frac{I_{Lx}}{2}$	$\frac{I_{Lx}d}{2(1-d)}$

Table 2. Average values of device currents (per phase x) over switching period and line period

Element	Average – switching period	Average – line period
Switch in each leg Qx	$\frac{3}{2}i_L D$	$\frac{I_o.(8-\pi M/\pi M)}{\pi}$
Diodes, DxM	$i_L(1-D)$	$\frac{3I_o}{\beta 2}$
Dx1	$\frac{i_L(1-D)}{2}$	$\frac{3I_o}{2\beta 2}$
Dx2	$\frac{i_L(1-D)}{2}$	$\frac{3I_o}{2\beta 2}$
Dx3, Dx01,Dx02	$I_o(1-D)$	$3I_o(1-1/\beta 2)$
Bridge diodes	i_{Lx}	$\frac{2I_o}{\pi M}$

Table 3. RMS values of device currents (per phase x) over switching period and line period

Element	RMS switching period	Rms line period
Lx1	i_L	$\frac{4I_o}{\sqrt{3}M\pi}$
Lx2	$i_L/2$	$\frac{2I_o}{\sqrt{3}M\pi}$
DxM	$i_L.\sqrt{(1-D)}$	$\frac{4I_o}{\sqrt{3}M\pi}$
Dx1	$\frac{i_L.\sqrt{(1-D)}}{2}$	$\frac{2I_o}{\sqrt{3}M\pi}$ $\frac{\sqrt{6}I_o}{(3M^2\sqrt{\pi\beta_2})}\sqrt{[(-8M^3-3\pi M^2-12M-6\pi)\beta_2+6\pi+12\tan^{-1}(\frac{M}{2\beta_2})]}$
Dx2	$\frac{i_L.\sqrt{(1-D)}}{2\sqrt{D}}$	$\frac{\sqrt{3}I_o}{M}\sqrt{(\frac{\sqrt{3}}{\beta_2}+\frac{1}{\beta})}$

Dx3, Da01,Dao 2	$I_o.\sqrt{(1-D)}$	$I_o\sqrt{(3(1-\frac{1}{\beta_2})}$
Switch Qx	$3i_L.\sqrt{D}$	$\frac{\sqrt{6}I_o}{(M^2\sqrt{\pi\beta_2})}\sqrt{[(9M^2\pi-8M^3-12M-6\pi)\beta_2+6\pi+12\tan^{-1}(\frac{M}{2\beta_2})]}$
Cx1, cx2,Cx3	$\frac{i_L.\sqrt{(1-D)}}{2\sqrt{D}}$	$\frac{\sqrt{3}I_o}{M}\sqrt{(\frac{\sqrt{3}}{\beta_2}+\frac{1}{\beta})}$
cxs	$\frac{3i_L\sqrt{D}(1-D)}{2\sqrt{(1-D)}}$	$\frac{3I_o}{(M^2\sqrt{6\pi\beta})}\sqrt{M[-3(3M^4+4M^2+8)+4M^3-12M(3M^2+4)]B+24\pi-48\tan^{-1}(\frac{M}{B})]}$
cxM	$\frac{i_L\sqrt{D}}{2\sqrt{(1-D)}}$	$\frac{I_o}{(M^2\sqrt{6\pi\beta})}\sqrt{M[-3(3M^4+4M^2+8)+4M^3-12M(3M^2+4)]B+24\pi-48\tan^{-1}(\frac{M}{B})]}$
Bridge	i_L	$\frac{2\sqrt{2}I_o}{(\sqrt{3}\pi\mathrm{M})}$

5. Results and Discussion

The proposed three-phase modular converter was tested in MATLAB/SIMULINK at 230 V per phase, 50 Hz, with a rated output load of 7.5 kW and a target DC bus of 1600 V. Both steady-state and step-load conditions were examined. After the simulation, the same operating conditions were applied on the Opal-RT real-time platform to verify that the results hold outside the simulation environment. The waveforms from both platforms are presented and discussed below.

Figure 3(a) shows the three-phase source currents Ia, Ib, and Ic under steady-state conditions. All three are sinusoidal and well balanced across the full cycle. There is no visible asymmetry between phases, which confirms that the three modules share the load equally. This matters practically - unequal phase loading in a grid-connected system causes neutral current and upstream transformer stress that cannot always be corrected at the charger level. The balanced result here comes directly from the 120° interleaving of the three modules and the symmetric structure of each phase module.

Figure 3(b) overlays the phase voltage and the corresponding input current for one phase. Both waveforms peak at the same point in the cycle. This alignment, near-zero displacement angle, is the direct outcome of how the inner current loop is structured.

The controller multiplies the output of the voltage loop by a unit sinusoidal template derived from the supply voltage, so the current reference is always in phase with the voltage. Without this, the switched-capacitor network would draw a heavily distorted, pulsed current. The unity displacement factor combined with low harmonic distortion gives a power factor close to 1, which is what grid operators and standards like IEC 61000-3-2 actually require.

The switch voltage waveform is given in Figure 3(c). The measured stress is well below the 1600 V output. This is one of the reasons the switched-capacitor approach was chosen here. In a conventional boost rectifier, the switch sees the full DC bus voltage during turn-off, which pushes the designer toward slow, expensive high-voltage IGBTs. Here, the multiplier network distributes the output voltage across the capacitor stack, so each switch only blocks Vo/(2+D). Lower-rated, faster devices can be used, which reduces both the switching loss and the bill of materials. At 1600 V output, this difference is not marginal; it is the difference between 1700 V class devices and 900 V or 1200 V class devices, which are significantly cheaper and more widely available.

Figure 3(d) shows the source currents during a load change. At around t = 1.5 s, the load is stepped down; at t = 3 s, it is restored. Through both transitions, the currents stay sinusoidal and balanced. The amplitude drops and recovers cleanly, without inter-phase disturbance.

What this tells is that each module's control loop responds independently without pulling the other phases out of balance, which is exactly what is required from a modular design. The settling is fast enough that the disturbance is barely visible on the waveform scale used.

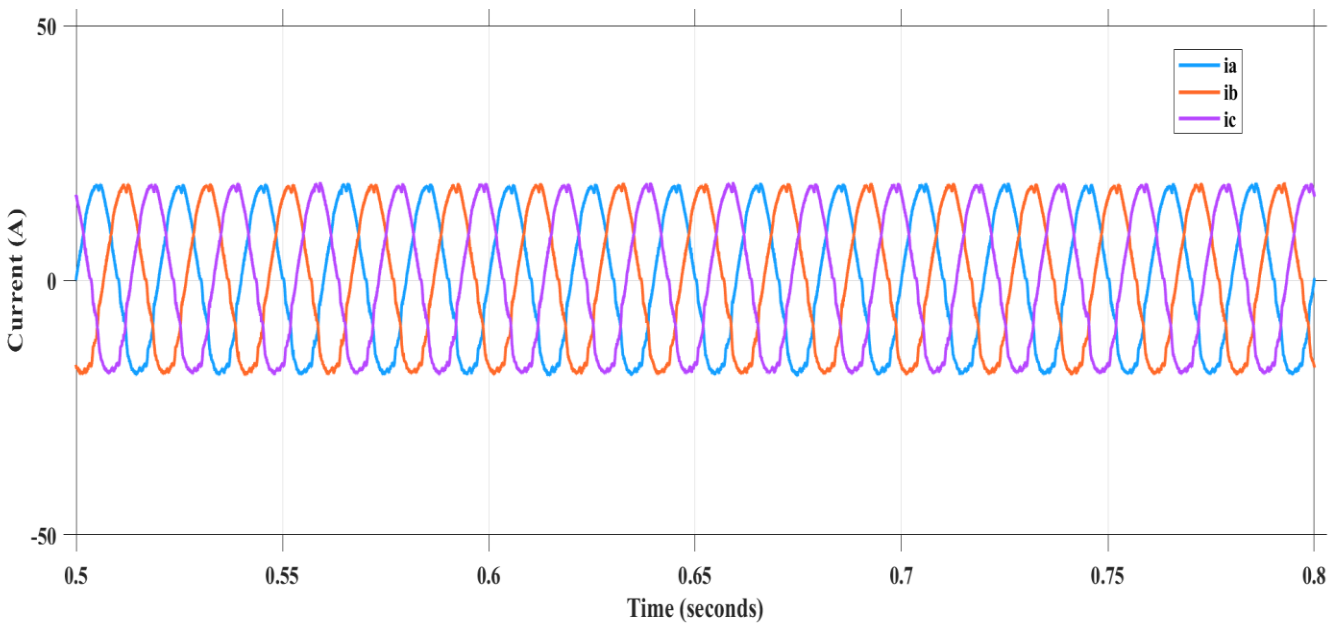
The current spectrum is shown in Figure 3(e). The 50 Hz fundamental is dominant at 18.63 A. All harmonic orders above the fundamental are small in comparison. The calculated THD of the source current is 5.38%.

IEC 61000-3-2 requires that equipment in this class stay below 8% in most harmonic categories, and 5.38% sits comfortably within that limit. Getting to this level without a large passive input filter is the direct result of the average current controller keeping the inductor current on a sinusoidal track at the switching frequency bandwidth. It is worth noting that this THD figure was obtained at rated load. THD typically rises at light load, so partial-load performance should also be evaluated before a final hardware design is committed.

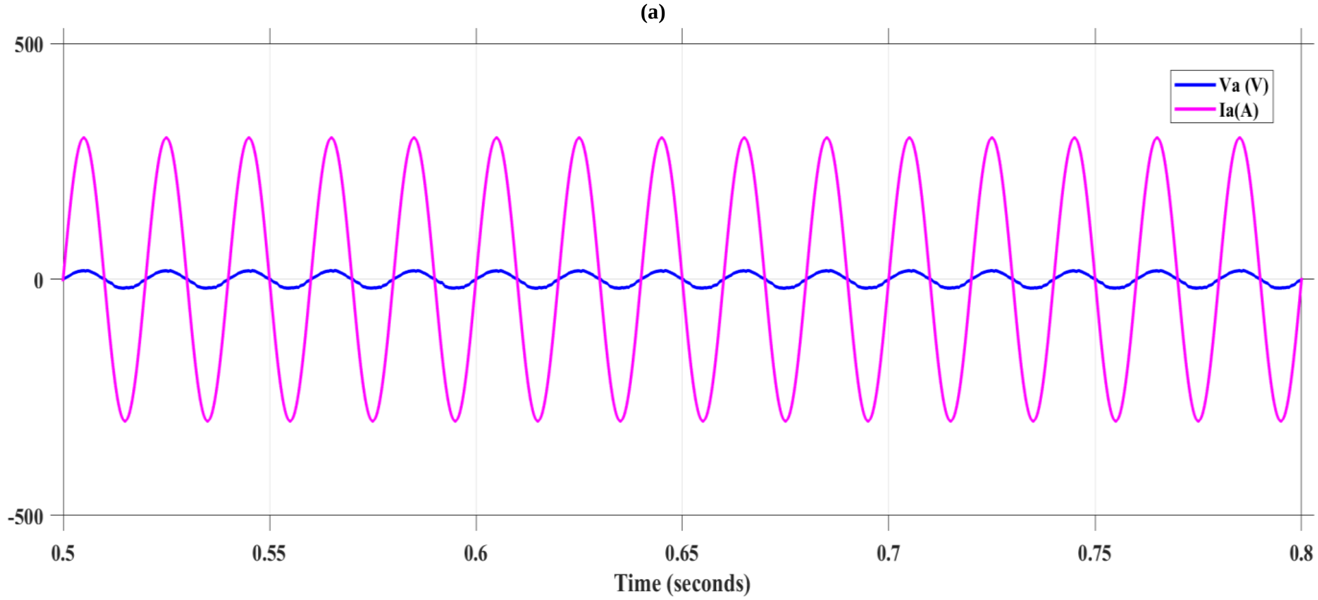
Figure 3(f) presents the DC output current Io under the same load variation. Starting at roughly 4.5 A at full load, the current drops to about 2.5 A when the load is reduced, then returns when the load is reapplied. Both transitions settle without sustained oscillation or significant overshoot. The settling time is short relative to the line cycle, which reflects the bandwidth margin built into the outer voltage loop. A slow voltage loop would allow the output current to drift for several cycles before correcting, which is not what is seen here.

The output voltage through the same load variation is given in Figure 3(g). Despite the step changes in Figure 3(f), the output voltage stays essentially flat. There is a small dip and a small overshoot at each transition, but both are corrected within a short interval. The voltage never leaves the acceptable regulation band.

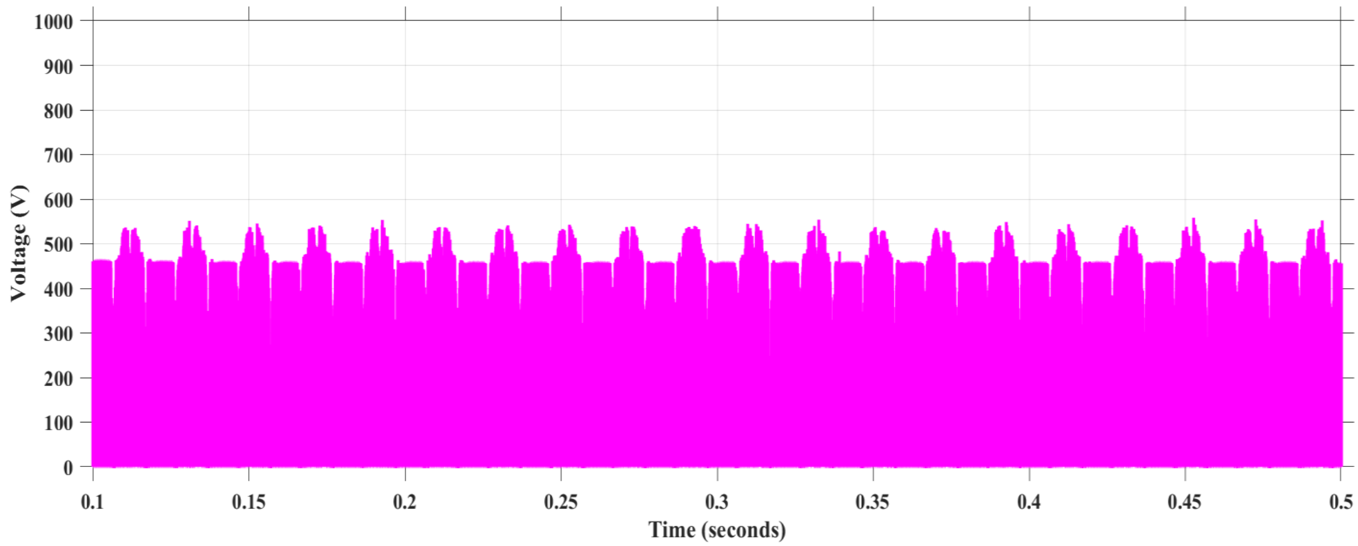
The switched-capacitor bank contributes here in a way that a single large output capacitor would not. Energy is distributed across multiple capacitors in the multiplier stack, so the effective stored energy per unit voltage deviation is larger, which naturally limits how far the output drops before the control loop has time to respond.



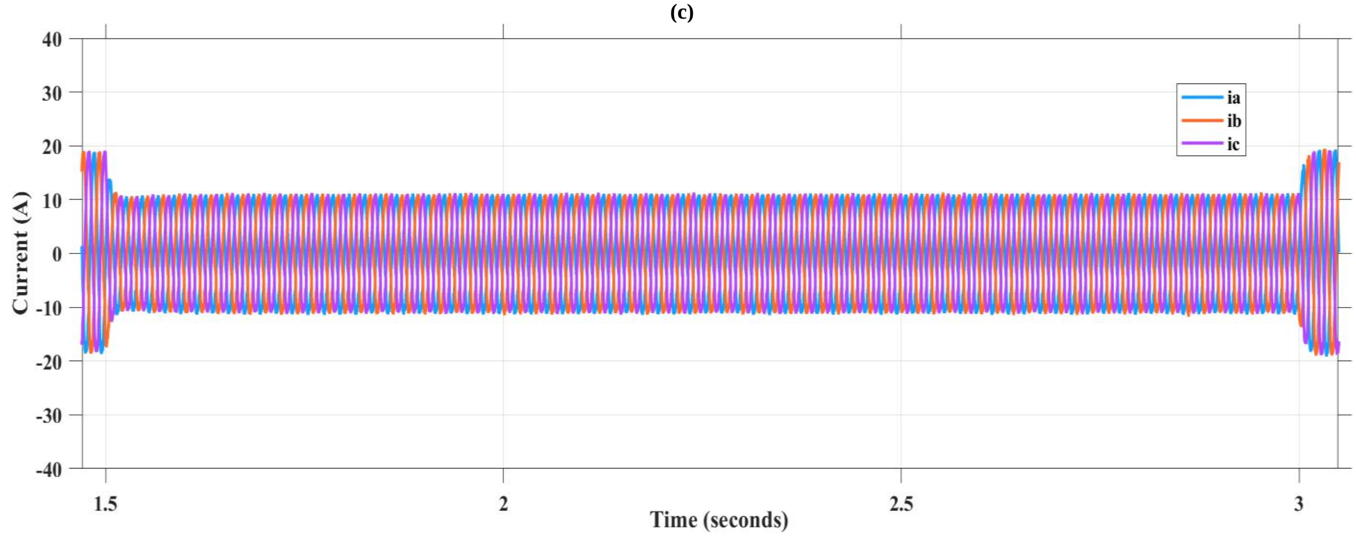
(a)



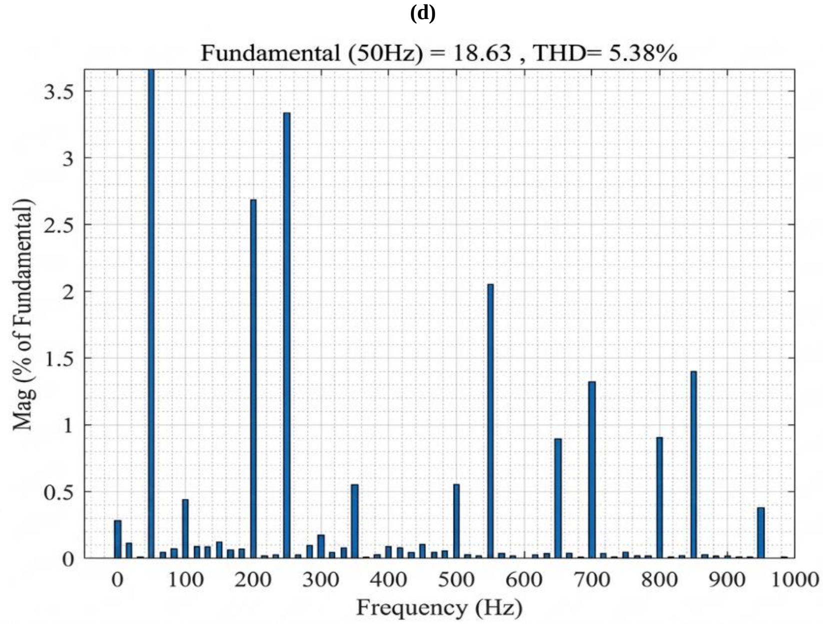
(b)


Voltage (V)
Time (seconds)
1000
900
800
700
600
500
400
300
200
100
0
0.1
0.15
0.2
0.25
0.3
0.35
0.4
0.45
0.5

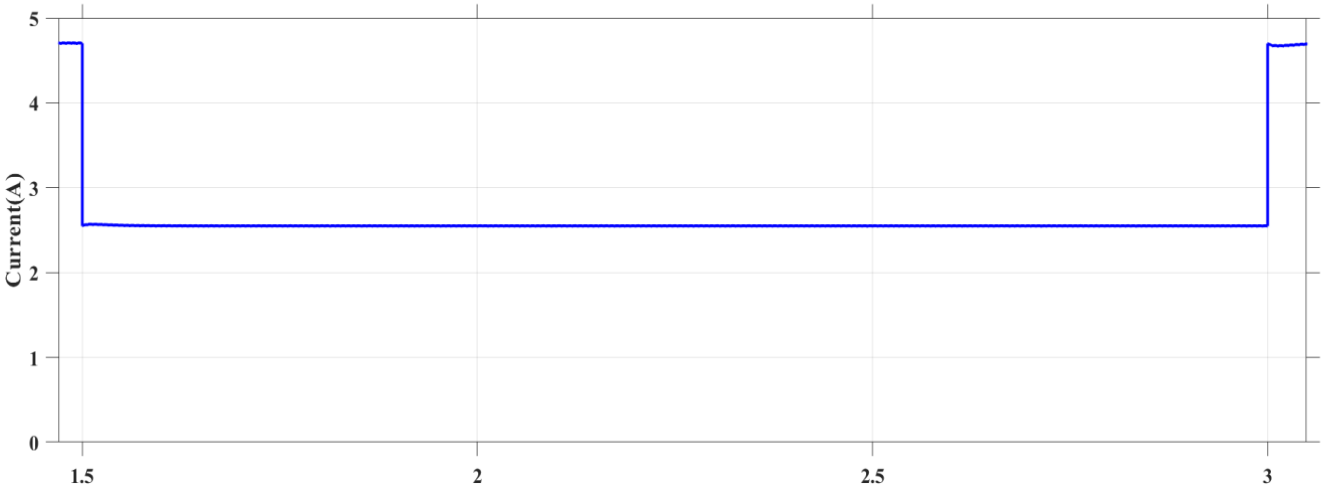
(c)


Current (A)
Time (seconds)
ia
ib
ic
40
30
20
10
0
-10
-20
-30
-40
1.5
2
2.5
3

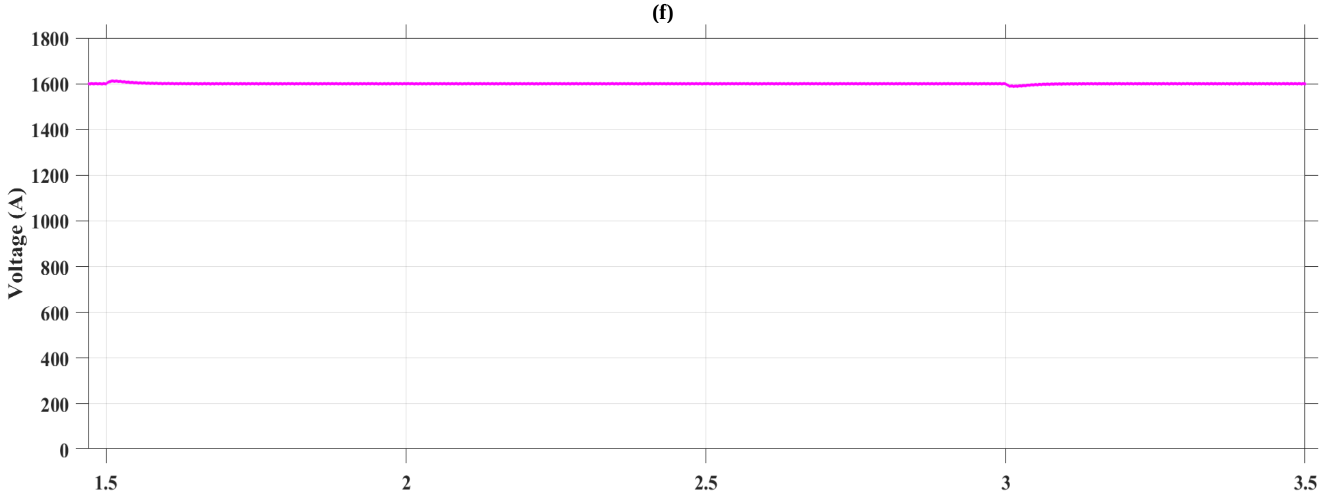
(d)


Fundamental (50Hz) = 18.63 , THD= 5.38%
Mag (% of Fundamental)
Frequency (Hz)
3.5
3
2.5
2
1.5
1
0.5
0
0
100
200
300
400
500
600
700
800
900
1000

(e)

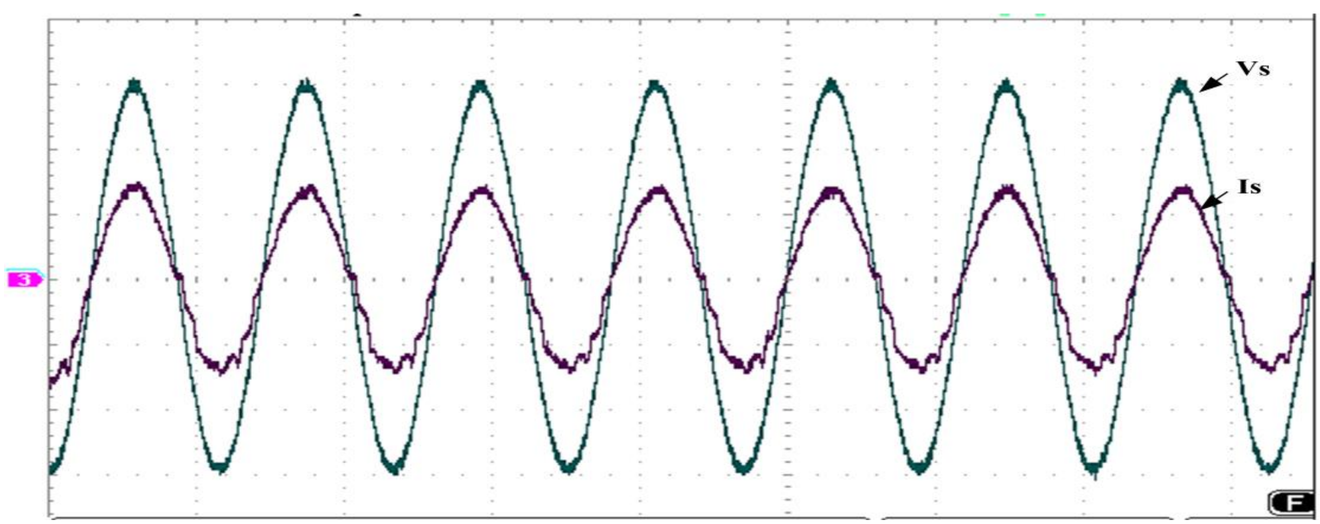


(f)

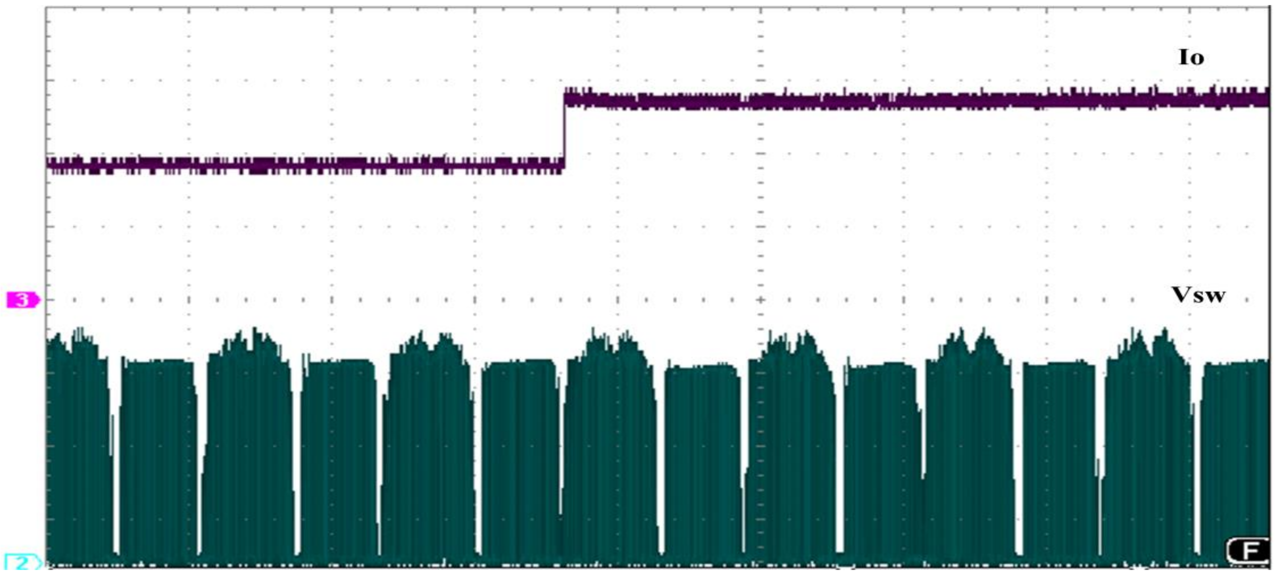


(g)

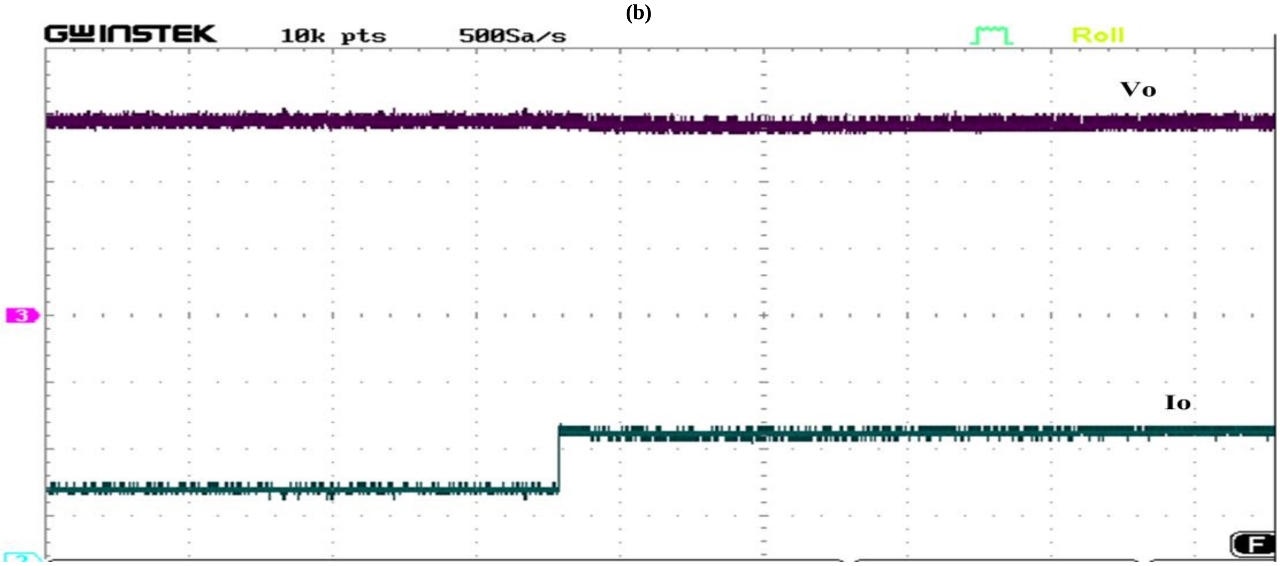
Fig. 3 Simulation results of (a) Three-Phase currents, (b) Phase voltage and current, (c) Switch voltage, (d) Dynamic change of source currents with change in load, (e) THD analysis of source current, (f) Io load current with dynamic change, and (g) Vo output voltage with change in load



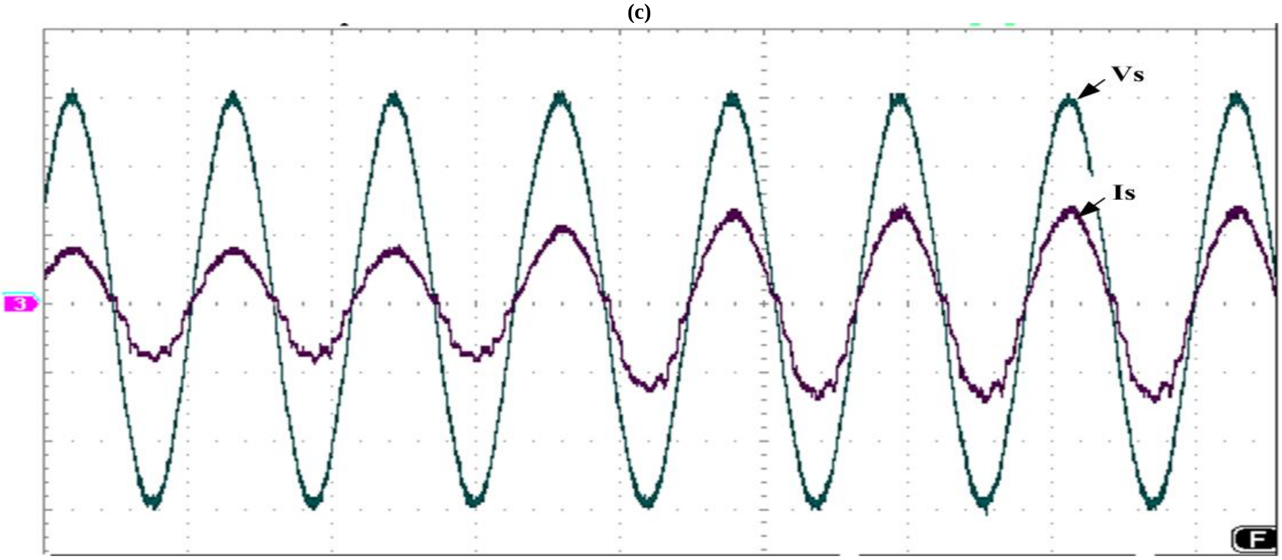
(a)



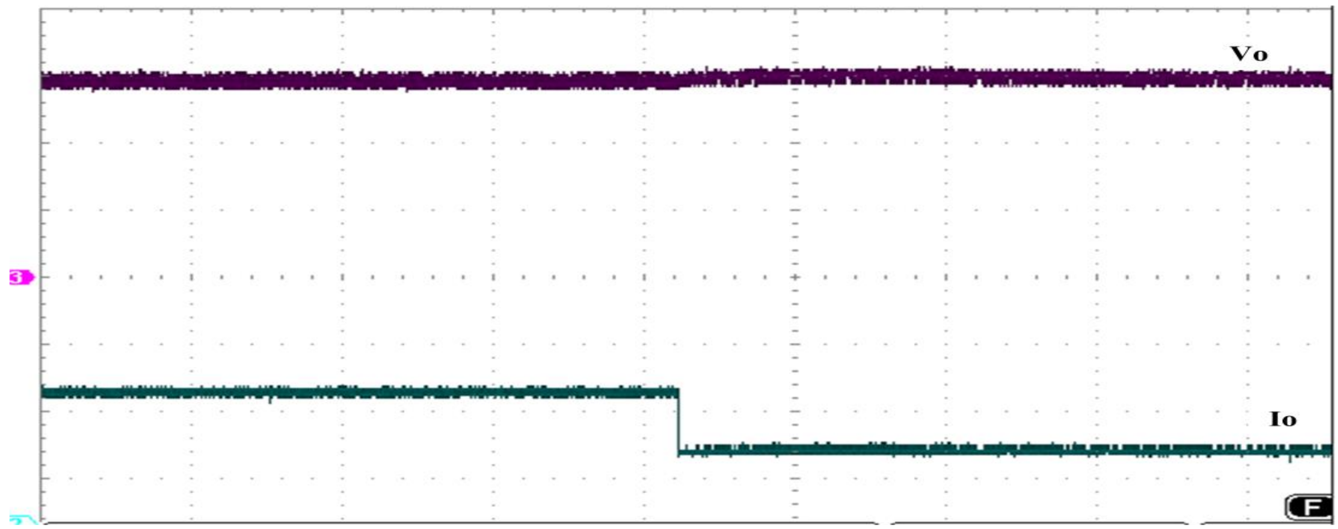
(b)



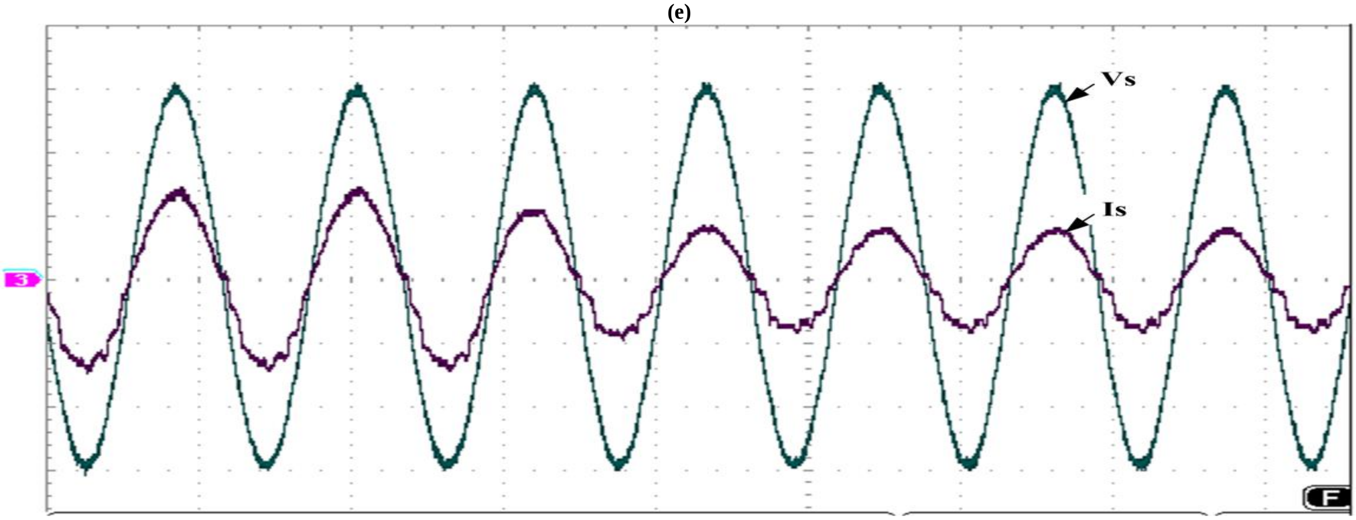
(c)



(d)



(e)



(f)

Fig. 4 Example for large figures Opal-Rt results of (a) Supply voltage and current, (b) Dynamic change of Io and switch voltage, (c) Io and Vo with increase in load, (d) Vs and Is with increase in load, (e) Io and Vo with decrease in load, and (f) Vs and Is with decrease in load.

Table 4. Comparison of various configurations

Parameter	**[13]**	**[14]**	**[15]**	**Proposed**
Rated power (kW)	2	0.648	12	7.5
Input voltage (per phase)	80	60	380	230
Output voltage (V)	300	180	500	1600
Attained gain	1.88	3	1.32	4.88
THD (%)	4.32	-	4.2	5.38
Power factor	Near unity	Near unity	Near unity	Near unity
Voltage gain	1/(1-D)	2/(1-D)	1/((1-D)	(2+D/(1-D)
Switch	1	3	3	3
Diodes	6	6	12	24
Inductors	3	3	6	6
capacitors	1	2	1	12
Stress on switch	Vo	Vo/2	Vo	Vo/(2+D)

Figure 4 shows the Opalrt results of the proposed modular converter. Figure 4 (a) illustrates the source current (Is) and source voltage (Vs). These are the results obtained at steady state at 50 Hz frequency. It shows that both these parameters are nearly sinusoidal and in phase with each other indicates that the converter is operating at nearly unity power factor. Figure 4 (b) illustrates the voltage stress that appears across the active switch and load current during the dynamic state. It is observed that the reverse bias voltage across the switch in each module converter has a reduced value, as illustrated in the simulation results. Figure 4 (c) depicts the DC output current and output voltage during the dynamic state. It was observed that with an increase in load, the output voltage dips during that particular instant and settles to its final value of 1600V with the provided control technique. Figure 4 (d) illustrates results with an increase in load current. With an increase in load current, the corresponding change in source current or phase current can be observed, whereas source voltage remains unchanged. Figure 4 (e) depicts the DC output current and output voltage during the dynamic state with reduce in load current. It was observed that with a decrease in load current, the output voltage slightly increases during that particular instant and settles to its final value of 1600V with the provided control technique. Figure 4 (f) illustrates results with a decrease in load current. With a decrease in load current, the corresponding change in source current or phase current can be observed, whereas source voltage remains unchanged. These results show that output voltage Vo remains the same with dynamic change. Table 4 represents the comparison performance of various three-phase PFC converters [13-15] with the proposed one. The voltage gain attained by the proposed one is more when compared to [13-15]. This gain allows the proposed converter to operate at a high voltage of 1600 V, whereas existing topologies [13-15] cannot obtain 1600 V at this power, as they may move to an unstable state. Though the proposed converter requires a larger number of capacitors, these are switched capacitors, but not bulk energy storage. Therefore, the size of these capacitors is smaller, resulting in occupying less space and weight. The diodes other than the bridge rectifier operation are part of voltage multiplication, making the size of the diodes as small and cheap as possible. The THD of the proposed converter is 5.38 %, which is below the IEC 61000-3-2 limit. The proposed modular converter has low stress on the active switch device when compared to [13-15].

6. Conclusion

This study looks at how a modular three-phase PFC converter was built and tested. It does a great job of boosting voltage and improving power quality. Designed using MATLAB/Simulink, the converter shows impressive features: smooth current flow, very little distortion, a power factor close to 1, and a steady high-voltage output, with less stress on the switch. The switched-capacitor modular design makes the system safer and easier to expand. It spreads out the voltage levels and avoids using bulky transformers. The converter responds quickly and accurately, making it ideal for tough jobs like EV chargers, factory power systems, and renewable energy setups. Future research could look into building real hardware, using smarter control methods, and connecting the converter to green energy sources to make it even more efficient, reliable, and compact.

Conflicts of Interest

"The author(s) declare(s) that there is no conflict of interest regarding the publication of this paper."

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