SSRG International Journal of Electrical and Electronics Engineering
ISSN: 2348-8379/ https://doi.org/10.14445/23488379/IJEEE-V13I9P112

Volume 13 Issue 9, 148-158, September 2026


*Original Article*

# Design and HIL Validation of Van der Pol-based Virtual Oscillator Control for Two Parallel Inverters

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Received: 07 May 2026 Revised: 27 August 2026 Accepted: 15 September 2026 Published: 26 September 2026

***Abstract*** *- Islanded AC microgrids with parallel inverters require coordinated voltage formation and load sharing. This study presents a Van der Pol-based virtual oscillator controller for two parallel single-phase voltage-source inverters. The voltage reference of each inverter is generated from its local output-current measurement, and no communication channel is used between the two control units. The controller parameters are selected from the inverter power rating, nominal voltage and frequency, allowable frequency variation, transient requirement, and third-harmonic constraint. The proposed method is evaluated in a MATLAB/Simulink model and then executed on a TMS320F28379D DSP connected to a Typhoon HIL 402 real-time simulator. The test cases include resistive-load operation with equal 1:1 and unequal 1:2 current-sharing conditions, resistive load steps, and a nonlinear rectifier-load case. For the tested conditions, the inverter voltages settle near 220 V RMS, and the current waveforms follow the selected sharing settings in both the simulation and Controller-Hardware-in-the-Loop (CHIL) results. Under the nonlinear load, the inverter currents are distorted, whereas the inverter voltages remain synchronized and nearly sinusoidal. The results show that the controller can be implemented on the selected DSP-HIL platform for communication-free parallel-inverter operation.*

***Keywords*** *- Virtual Oscillator Control, Van der Pol oscillator, Parallel inverters, Islanded AC microgrid, Hardware in the Loop (Typhoon HIL).*

## 1. Introduction

The increasing penetration of Distributed Generation (DG) and renewable energy sources has led to a growing interest in inverter-dominated AC microgrids. In islanded operation, parallel-connected inverters are required to achieve precise proportional power sharing of both active and reactive, while simultaneously maintaining voltage magnitude and frequency within permissible tolerances [1]. Conventional droop-based primary control can achieve decentralized power sharing but suffers from steady state voltage and frequency deviations, limited dynamic performance, and sensitivity to line impedance mismatches. These drawbacks become more critical in low-inertia microgrids with frequent load changes and high-power-density converters [2-6].

Several approaches have been developed to improve conventional droop control, including robust droop formulations, adaptive virtual-impedance techniques, and distributed secondary controllers. These methods can improve voltage-frequency regulation and power-sharing accuracy [5, 7, 8]. However, virtual-impedance and adaptive schemes introduce additional tuning requirements, whereas distributed secondary schemes generally require communication or coordination among inverters. As an alternative, Virtual Oscillator Control (VOC) emulates the dynamics of coupled nonlinear oscillators, allowing parallel inverters to synchronize through electrical coupling at the common AC bus. By generating voltage references directly in the time domain, conventional Van der Pol-based VOC generates the voltage reference directly in the time domain and can avoid dedicated power-calculation and phase-locked-loop blocks, while enabling communication-free synchronization and load sharing among parallel inverters [9-12].

Previous studies have established synchronization properties of Virtual Oscillator Control (VOC), identified droop-like characteristics embedded in nonlinear oscillator dynamics, and reported faster transient behavior than conventional droop control under selected operating conditions. These contributions have been supported by analytical studies, numerical simulations, and selected experimental demonstrations [12-14]. However, the practical implementation of Van der Pol-based VOC remains sensitive to the selection of oscillator and scaling parameters, which must be coordinated with the inverter rating, voltage and frequency specifications, transient-response targets, and harmonic-performance requirements. A reproducible design-to-validation workflow that combines multi-constraint Van der Pol VOC parameter selection with Controller-Hardware-in-the-Loop (CHIL) testing of parallel single-phase inverters remains insufficiently documented. This work addresses this need through real-time validation on a DSP-Typhoon HIL platform.

The transition toward low-inertia, inverter-dominated power systems has increased the importance of grid-forming inverters that can autonomously establish and regulate local voltage and frequency [15-17]. Although the communication-free synchronization capability of Virtual Oscillator Control (VOC) has been established through analytical and experimental studies, the real-time implementation of a Van der Pol-based VOC remains sensitive to the selection of oscillator parameters, scaling gains, and digital implementation settings [9, 12, 18, 19]. In particular, the oscillator and scaling parameters should be selected consistently with the inverter power rating, nominal voltage and frequency, transient-response requirements, and harmonic limits [9]. During digital implementation, the selected design must also be assessed with respect to the sampling interval, PWM update process, and controller-execution delay [20].

This paper addresses these gaps by: (1) A Van der Pol-based VOC scheme is developed for two parallel single-phase inverters, in which local current feedback enables autonomous synchronization and prescribed active-power sharing under equal and unequal sharing ratios. (2) A systematic parameter-design procedure is established for the voltage and current scaling gains, nonlinear oscillator coefficients, and virtual inductance and capacitance. The procedure relates these parameters to the rated power, nominal voltage and frequency, transient-response target, and harmonic-performance constraint specified by IEEE Std 519-2014 [9, 21]. (3) Implementing the proposed controller on a Typhoon HIL 402 platform and a C2000 DSP, and validating it under multiple loading scenarios, including resistive loads, nonlinear loads, equal and unequal power ratings (1:1 and 1:2 sharing), and step load changes.

Table 1 summarizes the main differences between droop control and VOC in terms of stability, power-sharing performance, control complexity, and application scope. Although droop control is basic and low complexity, VOC achieves better local stability with self-synchronization and enables plug-and-play operation in dispersed microgrids.

**Table 1. Comparison of Droop Control and Virtual Oscillator Control (VOC)**

| Criteria | Droop | VOC |
|---|---|---|
| Stability | Moderate, requires secondary control [16, 22] | Good local stability due to self-synchronization [9] |
| Power sharing | Simple, but with limited power-sharing accuracy [17] | Good; supports plug-and-play operation [9] |
| Complexity | Low [22] | Moderate, based on oscillator models [9] |
| Applications | Small microgrids, weak grids [17], | Distributed microgrids and self-synchronizing systems [9] |

## 2. Van der Pol-based VOC and Power Sharing

### *2.1. Parallel Inverters AC Microgrid*

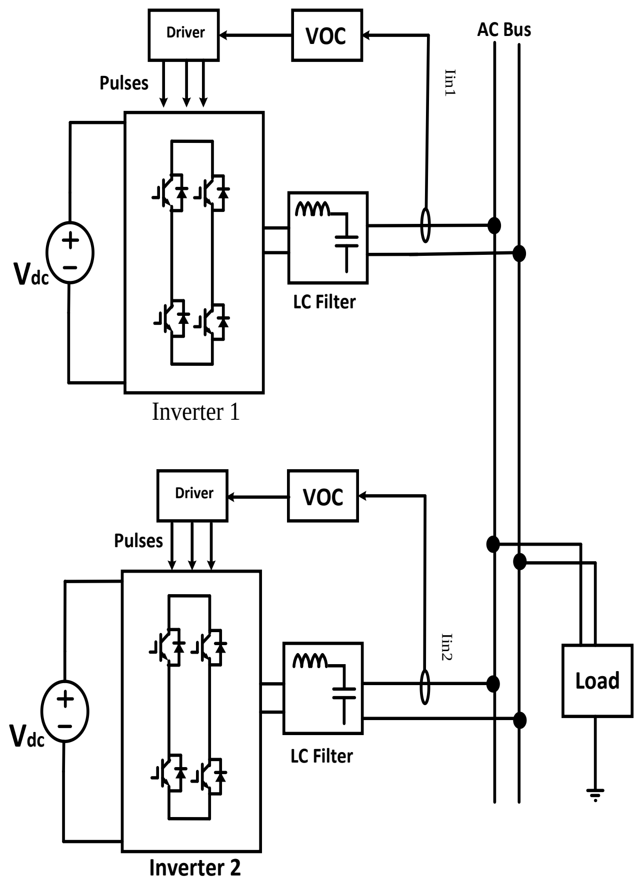



**Fig. 1 System configuration of two parallel inverters using VOC**

The studied islanded AC microgrid consists of two single-phase Voltage-Source Inverters (VSIs) connected in parallel to a common AC bus, as illustrated in Figure 1. Each VSI is supplied by an independent DC source and connected to the Point of Common Coupling (PCC) through an LC output filter. A common load is supplied at the PCC.

The parallel configuration requires the two VSIs to maintain a synchronized bus voltage while sharing the load power according to the assigned operating condition. This arrangement is therefore suitable for assessing the synchronization and power-sharing characteristics of the proposed Van der Pol-based VOC.

### *2.2. Van der Pol-based VOC Structure for Parallel Inverters*

The proposed Virtual Oscillator Control (VOC) scheme is built around an electrical realization of a Van der Pol oscillator, which generates the voltage reference for each inverter and couples its dynamics to the AC bus through the inverter output current. In its canonical form, the Van der Pol oscillator is described by [9, 23-25].

$$\ddot{v} - \varepsilon \ (1 - v^2)\dot{v} + \omega_0 v = 0 \qquad (1)$$

where $v$ is the oscillator state, $\omega_0$ is the natural frequency, and $\varepsilon$ controls the nonlinearity and the limit-cycle amplitude. When $\varepsilon$ is properly tuned, the limit-cycle waveform is approximately sinusoidal at the desired frequency, making the oscillator suitable to generate AC voltage references for inverters [4, 5].

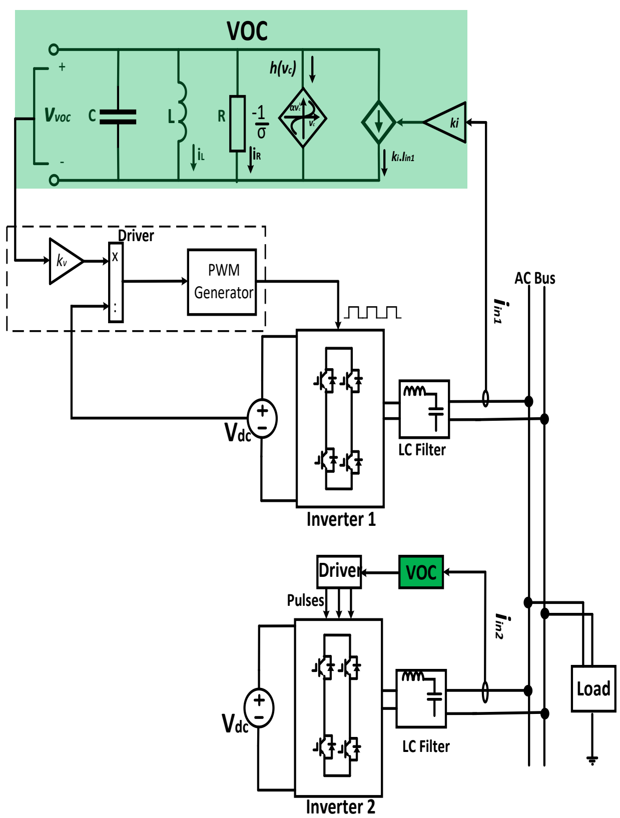



**Fig. 2 Van der Pol-based VOC structure with current feedback for parallel inverters**

In the upper part of Figure 2, the Virtual Oscillator Controller implements this behavior by means of a parallel connection of a capacitor *C*, an inductor L, a resistor R, and a nonlinear element $h(v_c)$ at the node with voltage $v_c$. The nonlinear characteristic is chosen as: $h(v_c) = \alpha v_c^3$, which provides negative damping for small amplitudes and positive damping for large amplitudes, so that the circuit converges to a stable limit cycle with a nearly sinusoidal waveform. Applying Kirchhoff's current law to the LC-R-h($v_c$) network yields a second-order nonlinear differential equation in $v_c$ that can be cast into the Van der Pol form, with an oscillation frequency approximately equal to $\omega_0 = 1/\sqrt{LC}$. The parameters L, C, R, and $\alpha$ are selected such that the limit-cycle amplitude of $v_c$ matches the desired inverter output voltage level [9].

The current-controlled source and the gain block depicted in Figure 2 construct a specialized feedback path with gain. $k_i$ that routes the inverter output current $i_{inv}$ back to the oscillator. This feedback incorporates a term proportional to $i_{inv}$ into the oscillator dynamics, allowing the Van der Pol oscillator to react to both its intrinsic parameter settings and the power it provides to the load.

In this way, the oscillator "feels" the loading conditions and the interaction with the AC bus, which is crucial for self-synchronization and power sharing among parallel inverters [4, 5].

The oscillator voltage $v_C$ is scaled by the gain $k_v$ to produce the inverter reference voltage $v_{ref}$ , as shown in the lower left block of Figure 2. The PWM generator and driver then receive the signal $v_{ref}$ and use it to create the matching gate pulses for the full bridge inverter, causing the inverter output voltage to follow the Van der Pol oscillator's limit-cycle waveform.

Each inverter (Inverter 1 and Inverter 2) is connected to the common AC bus through an LC filter and supplies the shared load. When both inverters operate under this VOC structure, their oscillators are coupled through the network and naturally synchronize in amplitude and phase without an inter-unit communication link, while the choice of the gains. $k_i$ determines the desired power-sharing ratios, as discussed in Section 2.3.

### *2.3. Power Sharing Mechanism in Van der Pol-based VOC*

In Van der Pol-based VOC, power sharing among parallel inverters is adjusted through the current feedback gain. $\mathbf{k_i}$ associated with each oscillator. When two inverters have identical parameters and equal values of $\mathbf{k_i}$, Their steady-state active power tends to be distributed nearly evenly, i.e., with an approximate 1:1 ratio [9].

If the gains are chosen with a prescribed ratio $\boldsymbol{k_{i1}}:\boldsymbol{k_{i2}}$ , the nominal active power ratio $\boldsymbol{P_1}:\boldsymbol{P_2}$ will approximately follow this ratio under operating conditions close to the rated point. In this way, desired power-sharing ratios (e.g., 1:1 or 1:2) can be set directly at the design stage via $\boldsymbol{k_i}$, without requiring dedicated power-control loops or communication between the inverters [4, 5].

## 3. Parameter Design of the Proposed Control System

### 3.1. System Description

As shown in Figure 2, the system under study is made up of two single-phase full-bridge voltage-source inverters coupled in parallel to a shared AC bus. Each inverter is supplied from an independent DC source with a bus voltage of $V_{dc}$ = 400 V and is rated at $P_{rated}$ = 3 kW, with a nominal output voltage of 220 V (RMS) at 50 Hz. The output of each inverter is connected to the AC bus through an identical LC filter, which attenuates the high-frequency switching harmonics generated by the bipolar Pulse-Width Modulation (PWM) scheme. Throughout all test scenarios taken into consideration in this work, the system functions in islanded mode with a common linear load connected at the Point of Common Coupling (PCC). The VOC algorithm is executed digitally on a Texas Instruments TMS320F28379D Digital Signal Processor (DSP), which generates the PWM gate signals for both inverters. The feedback signals, specifically the output currents of each inverter, are measured and fed back to the DSP via the analog input (ADC) channels at a sampling rate equal to the PWM switching frequency of 10 kHz. In the equal power-sharing scenario, both inverters operate with identical control gains; in the unequal power-sharing scenario, the current gain $\boldsymbol{k_i}$ of one inverter is scaled to realize a 1:2 power ratio, as detailed in Section 3.3.

### 3.2. Design Requirements

The VOC parameters and the LC output filter are designed to satisfy the following performance specifications, which are derived from the system ratings and relevant power quality standards [21].

Nominal Operating Point:

Open circuit voltage: $V_{oc} = 220V$ (RMS)
Rated active power per inverter: $P_{rated}$ = 3000 W
Voltage at rated power: $V = 198V$ (RMS)
Rated reactive power: $Q_{rated}$ = 3000 VAr
Nominal angular frequency: $\omega_0 = 2\pi$ (50) rad/s

Steady State Regulation:

Maximum allowable angular frequency deviation: $\Delta\boldsymbol{\omega_{max}} \leq \Delta\boldsymbol{\omega_0}\ (\boldsymbol{rad/s})$.

Voltage deviation at PCC bounded within $|\Delta\boldsymbol{V}| \leq \mathbf{5}\%\boldsymbol{V_{oc}}$.

Dynamic Response:

Voltage rise time (10% - 90%) for a step change in load: $\boldsymbol{t_{rise}} \leq \mathbf{0.2}\boldsymbol{s}$.

Harmonic Performance:

The third-harmonic ratio was limited to 2% as a conservative internal design target. Compliance with IEEE Std 519-2014 was assessed using the voltage distortion measured at the PCC. For the 220 V PCC in this study, the applicable voltage-distortion limits are 5% for an individual harmonic and 8% for total voltage harmonic distortion [21].

Accordingly, $\mathbf{V_{oc}}$, $\mathbf{P_{rated}}$, $\mathbf{t_{rise}}$ and $\boldsymbol{\delta_{3:1}}$ are adopted as the main design specifications for selecting $\mathbf{C_{osc}}, \mathbf{L_{osc}}, \mathbf{k_v}, \mathbf{k_i}, \boldsymbol{\sigma}, \boldsymbol{\alpha}$ in the following subsection.

### 3.3. Parameter Design of Van der Pol-based VOC

The design of the VOC parameters follows the averaging-based methodology established in the literature, and proceeds in five steps [5].

(i) Voltage Gain $\boldsymbol{k_v}$

The voltage gain $\boldsymbol{k_v}$ scales the normalized oscillator state $\boldsymbol{v_c}$ to the physical inverter reference voltage $\boldsymbol{v_{ref}} = \boldsymbol{k_v}\boldsymbol{v_c}$. It is selected so that the unit amplitude of the Van der Pol limit cycle corresponds to the desired open circuit voltage: $\boldsymbol{k_v} = \boldsymbol{V_{oc}} = \mathbf{220}\boldsymbol{V}$.

(ii) Current Gain $\boldsymbol{k_i}$

The measured inverter output current is scaled by the current gain. $\mathbf{k_i}$ before being injected into the oscillator, it is chosen so that, when the inverter operates at rated power $P_{rated}$, the oscillator current. $\mathbf{k_i}$ equals unity, thereby normalizing the operating point:

$$\mathbf{k_i} = \frac{\mathbf{1}}{\mathbf{I_{rated}}} = \frac{\mathbf{1}}{\mathbf{P_{rated}/V}} = \frac{\mathbf{198}}{\mathbf{3000}} = \mathbf{0.066} \tag{2}$$

For the 1:2 unequal power-sharing scenario, the current gain of the second inverter is set to $\boldsymbol{k_{i2}} = \mathbf{2}\boldsymbol{k_{i1}}$, so that Inverter 2 supplies twice the active power of Inverter 1 at steady state.

(iii) Nonlinearity Parameter σ and α

The nonlinearity coefficient σ (equivalently, α in $\boldsymbol{h}(\boldsymbol{v_c}) = \boldsymbol{\alpha v_c^3}$) governs the trade VOC-controlled inverter system off between convergence speed and harmonic distortion. Following the design constraint derived from the averaged model, the oscillator capacitance $C_{osc}$ must satisfy simultaneously [9]:

- Lower bound from frequency regulation:
  $\boldsymbol{C_{osc}} \geq \boldsymbol{C_{min,1}}$

- Lower bound from harmonic distortion:
  $(\boldsymbol{\delta_{3:1}} \leq \mathbf{2}\%\boldsymbol{C_{min,1}}): \boldsymbol{C_{osc}} \geq \boldsymbol{C_{min,2}}$

- Upper bound from rise time requirement:
  $(\mathbf{t_{rise}} \leq \mathbf{0.2s}): \mathbf{C_{osc}} \leq \mathbf{C_{max}}$

$$\mathbf{C_{osc}} = \mathbf{0.18}\boldsymbol{F}, \boldsymbol{\sigma} = \mathbf{1/C_{osc}} = \mathbf{5.55} \tag{3}$$

(iv) Oscillator Inductance $L_{osc}$

Given $C_{osc}$ the virtual inductance is computed from the resonance condition $\boldsymbol{\omega_0} = \mathbf{1}/\sqrt{\boldsymbol{L_{osc}}.\boldsymbol{C_{osc}}}$

$$\boldsymbol{L_{osc} = \frac{1}{\omega_0^2 C_{osc}} = \frac{1}{(2\pi 50)^2(0.18)} = (5.63)10^{-5} H} \quad (4)$$

(v) Summary Table 2

Table 2 lists the final VOC parameters for both inverters. The equal power sharing configuration uses identical gains for both units, while the unequal configuration doubles $k_i$ for Inverter 2.

**Table 2. VOC parameters for the two parallel inverters**

| Symbol | Inverter 1 | Inverter 2 (equal) | Inverter 2 (1:2 ratio) |
|---|---|---|---|
| $\boldsymbol{k_v}$ | 220 | 220 | 220 |
| $\boldsymbol{k_i}$ | 0.066 | 0.066 | 0.132 |
| σ | 5.55 | 5.55 | 5.55 |
| $C_{osc}$ | 0.18 F | 0.18 F | 0.18 F |
| $L_{osc}$ | $(5.63)10^{-5}$ H | $(5.63)10^{-5}$ H | $(5.63)10^{-5}$ H |

### *3.4. LC Output Filter Design*

Before the inverter terminal is connected to the AC bus, each inverter has an LC output filter installed to reduce switching frequency ripple. Two common criteria are used to choose the filter inductance $L_f$ and capacitance $C_f$.

(i) Inductance $L_f$

At the switching frequency $f_{sw}$ =10 kHz, the inductance is selected to restrict the peak-to-peak current ripple $\Delta i_{ripple}$ to no more than 20% of the rated peak current $I_{rated}$:

$$\boldsymbol{L_f = \frac{V_{dc}}{4 f_{sw} \Delta i_{ripple}} = \frac{400}{(4)(10000)(0.2)(12)} = 4.2\ mH} \quad (5)$$

Thus, the filter inductance is selected as $\boldsymbol{L_f = 4.2\ mH}$

(ii) Capacitance $C_f$

The selected filter capacitor value is:

$$\boldsymbol{C_f = \frac{1}{(2\pi f_c)^2(L_f)}; f_c = 1000\ Hz} \quad (6)$$

$$\boldsymbol{C_f = \frac{1}{(2\pi 1000)^2(4.2)10^{-3}} = 6\ \mu F} \quad (7)$$

Where $f_c$ = 1000 Hz is the selected filter frequency, which is less than one tenth of the switching frequency, and $L_f$ is the inductance value.

(iii) Resonance frequency verifications

$$\boldsymbol{f_{res} = \frac{1}{2\pi\sqrt{(4.2)(10^{-3})(6)10^{-6}}} \approx 1002 Hz} \quad (8)$$

The selected LC filter, therefore, provides a practical compromise between switching ripple attenuation and dynamic compatibility with the VOC-controlled inverter system.

**Table 3. LC output filter and system parameters**

| Symbol | Parameter | Value |
|---|---|---|
| $V_{dc}$ | DC bus voltage | 400 V |
| $f_{sw}$ | PWM switching frequency | 10 kHz |
| $I_{rated}$ | Rated peak output current | 12 A |
| $\Delta i_{ripple}$ | Allowable current ripple | 2.4 A |
| $L_f$ | Filter inductance | 4.2 mH |
| $C_f$ | Filter capacitance | 6.0 $\boldsymbol{\mu F}$ |
| $f_{res}$ | LC resonance frequency | ≈ 1000 Hz |

## 4. Design simulation using MATLAB/Simulink and HIL Implementation

### *4.1. MATLAB/Simulink Model*

In this work, a MATLAB/Simulink model is employed to examine how a VOC scheme derived from Van der Pol oscillator characteristics behaves in a parallel single-phase inverter setup. The arrangement consists of two inverters connected to the same AC busbar. Each inverter is assigned a dedicated VOC controller, which synthesizes its voltage reference and uses locally measured feedback signals to achieve the desired sharing of power between the units. The VOC controller parameters obtained via the averaging method analysis are listed in detail in Table 2. In the nominal case, the two inverters are configured with the same control settings, so their dynamic responses remain comparable. By enforcing this symmetry, the test system provides a clear basis for evaluating how well the inverters synchronize their voltages and share power when operating in parallel. The overall control architecture is illustrated in Figure 3. In this setup, the filtered output current of each inverter is routed to its associated VOC controller. Using this feedback, the virtual oscillator synthesizes a voltage reference that drives the PWM stage, which in turn produces the gate pulses for the inverter's semiconductor switches. With this arrangement, each inverter can automatically synchronize to the system and share power, eliminating the need for explicit communication between the converters. Apart from the VOC control block, each inverter is supplied by a DC source and connected to the common AC load through an output LC filter. This filter suppresses harmonics generated by PWM switching, improves the voltage quality at the load terminals, and helps ensure that the measured feedback current faithfully represents the actual power condition of each inverter. The parameters of the two inverters are the same and are shown in Table 2.

### *4.2. CHIL Setup*

A CHIL setup was developed using a Typhoon HIL 402 real-time simulator in order to confirm the viability of implementing the controller in conditions similar to a real system. Typhoon HIL 402 is a real-time hardware-in-the-loop simulator for power electronics and renewable energy applications, enabling real-time simulation with very small-time steps, approximately 0.5 $\mu s$.

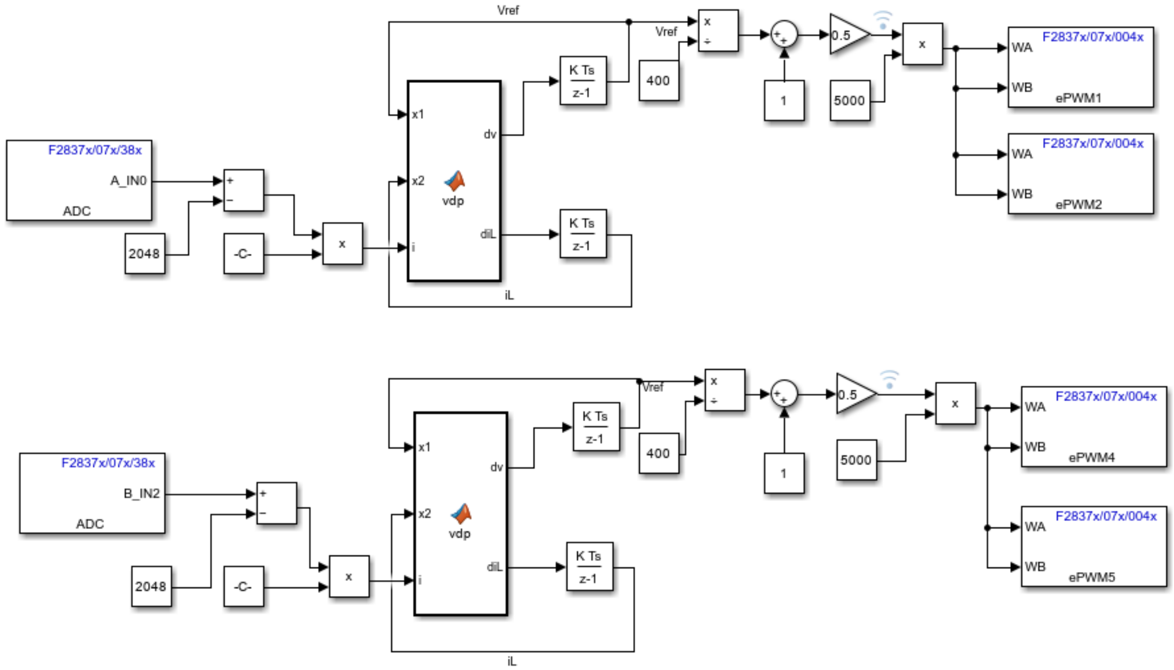



**Fig. 3 Control structure diagram for 2 inverters working in parallel in MATLAB/Simulink**

Figure 4 depicts the CHIL implementation hardware architecture. In this setup, the HIL DSP interface board connects the Typhoon HIL 402 pin-to-pin to the TMS320F28379D digital signal processor. The HIL device provides 0 - 3 V analog output channels to the DSP's ADC pins, and simultaneously receives PWM control signals from the DSP via digital input channels to simulate the switching of the power circuit in real time.

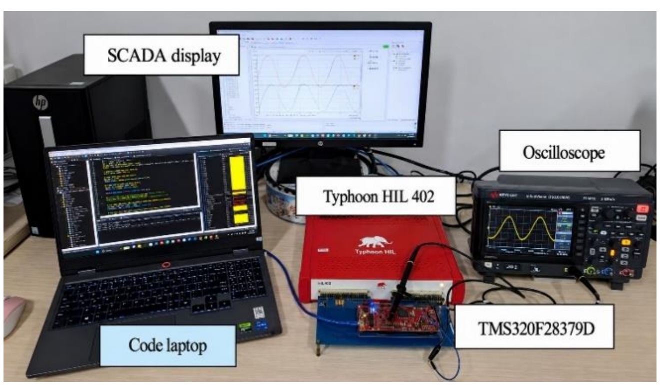



**Fig. 4 CHIL setup implemented using the TMS320F28379D DSP and Typhoon HIL 402**

The power circuit diagram implemented in Typhoon HIL is shown in Figure 5. In principle, this circuit corresponds to the model built in MATLAB/Simulink, consisting of two single-phase inverters connected in parallel, a DC power source, an LC filter, and an AC load. The current signals $I_{a1}$ and $I_{a2}$ are measured directly in the CHIL setup and sent to the DSP as feedback signals for the control algorithm. To implement the VOC algorithm on the digital controller, the team used MATLAB/Simulink in combination with the C2000 Microcontroller Blockset to build the program for the TMS320F28379D DSP. The connection configuration between the TMS320F28379D and the Typhoon HIL 402 is shown in Figure 5, where the ADC channels are used to receive the feedback current signal, while the ePWM channels are responsible for generating control pulses for the two simulated inverters in the HIL. The sampling frequency and pulse generation frequency were chosen as 10 kHz, consistent with the DSP's ePWM configuration and the control system's dynamic requirements.

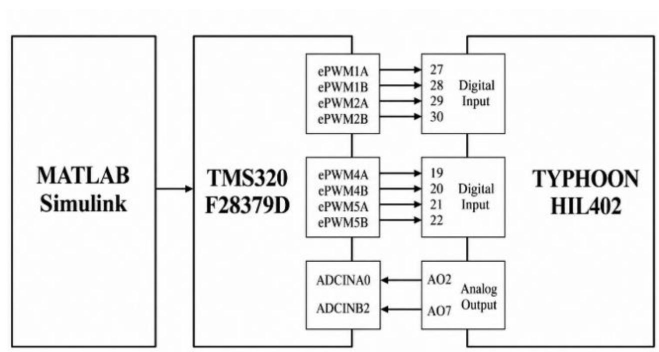



**Fig. 5 Pin-mapping between the TMS320F28379D DSP and the Typhoon HIL 402**

### *4.3. Simulation and CHIL Results*

This section details the simulation and CHIL validation scenarios designed to evaluate the precise power sharing and voltage synchronization among the parallel inverters.

#### 4.3.1. Case 1 - Resistive load, 1:1 sharing

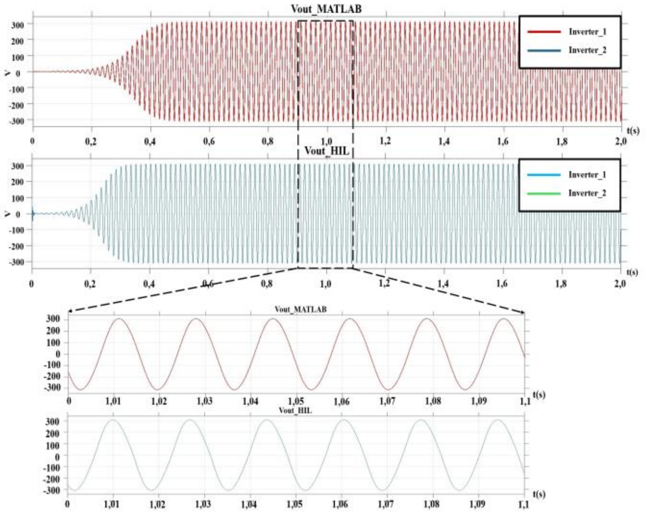



**Fig. 6 Output voltage waveforms under Case 1 (resistive load, 1:1 sharing) in MATLAB and CHIL**

Assuming a 1:1 power sharing ratio between the two inverters, the characteristic results shown in Figure 6 demonstrate that the voltage waveforms remain synchronized in both the MATLAB and CHIL scenarios. The measured peak voltage of 311 V, equivalent to 220 V RMS, aligns accurately with the calculated value. Furthermore, the system exhibits excellent transient response, settling within a brief period of 0.4 seconds. With a 1:1 power sharing ratio between the two inverters, MATLAB and CHIL simulation results regarding current characteristics (Figure 7) demonstrate that the currents flowing through the two units are identical, ensuring accurate power sharing.

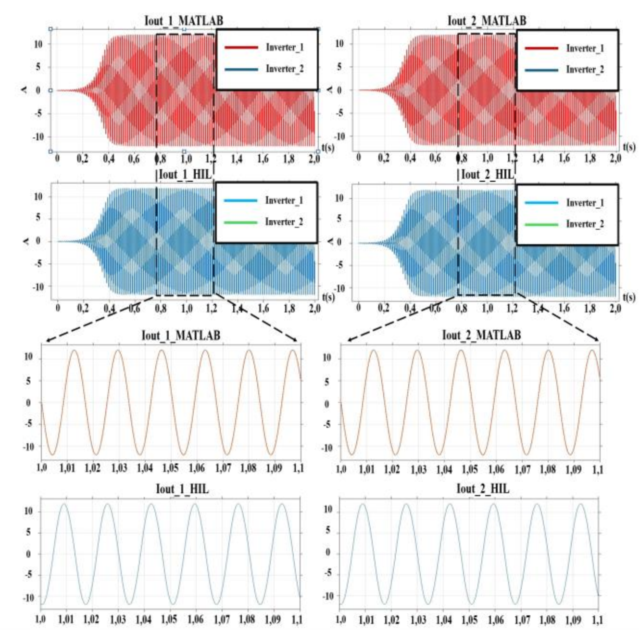



**Fig. 7 Output current waveforms under Case 1 (resistive load, 1:1 sharing) in MATLAB and CHIL**

#### 4.3.2. Case 2 - Resistive load, 1:2 sharing

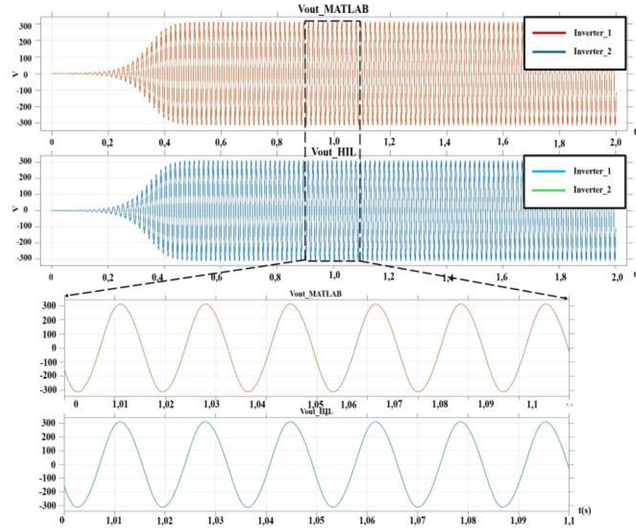



**Fig. 8 Output voltage waveforms under Case 2 (resistive load, 1:2 sharing) in MATLAB and CHIL**

As shown in Figure 8, the voltage amplitude profiles for both the MATLAB and CHIL cases are synchronized. The measured peak voltage of 311 V, equivalent to 220 V RMS, aligns accurately with the calculated value. Furthermore, the system demonstrates excellent transient response, settling within a short period of 0.4 seconds. Figure 9 shows the inverter currents for the 1:2 sharing case. After the start-up period, the peak current of Inverter 2 is approximately twice that of Inverter 1 in both the MATLAB/Simulink and CHIL results. The enlarged waveforms show the same relationship over successive cycles. This current ratio follows the selected current-feedback gains and corresponds to the intended 1:2 active-power-sharing condition.

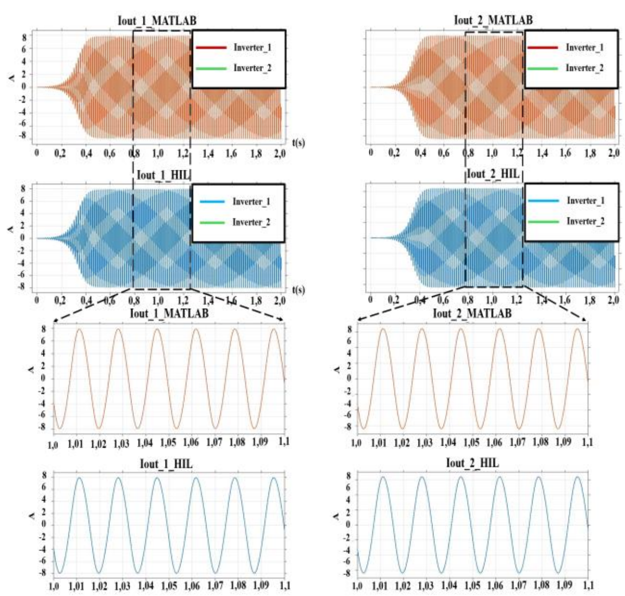



**Fig. 9 Output current waveforms under Case 2 (resistive load, 1:2 sharing) in MATLAB and CHIL**

#### *4.3.3. Case 3 - Load Increase and Decrease, 1:1 Sharing, Resistive Load*

As illustrated in Figure 10, the output voltage waveforms under Case 3 remain sinusoidal and well-regulated during both the load increase and load decrease events. After each step change, the transients last only a few hundred milliseconds before the voltages in MATLAB and CHIL settle back to steady 220 V RMS operation with very small mismatch in amplitude and phase.

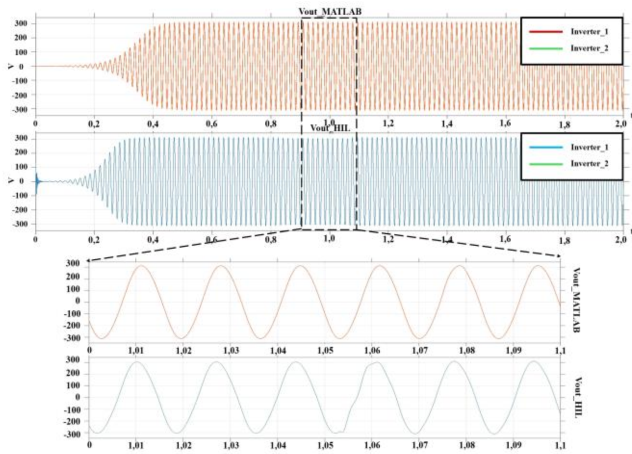



**Fig. 10 Output voltage waveforms under Case 3 (resistive load step, 1:1 sharing) in MATLAB and CHIL**

As illustrated in Figure 11, the output current waveforms in Case 3 show that both inverters respond coherently to the load steps, with their currents increasing and decreasing almost simultaneously. In steady state before and after each load change, the current amplitudes of the two inverters remain nearly equal in both MATLAB and CHIL, confirming that the VOC maintains the desired 1:1 power sharing ratio despite the resistive load variations.

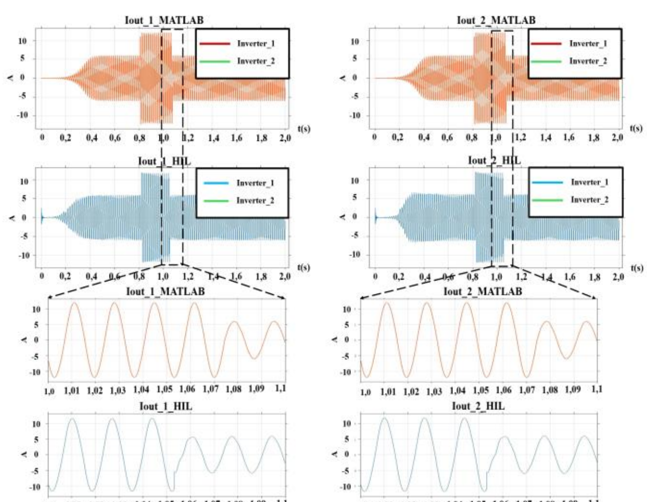



**Fig. 11 Output current waveforms under Case 3 (resistive load step, 1:1 sharing) in MATLAB and CHIL**

#### *4.3.4. Case 4 - Nonlinear Load under 1:1 Power Sharing*

Case 4 evaluates the proposed Van der Pol-based VOC under a nonlinear load while maintaining a 1:1 power-sharing objective. In this case, the common load connected at the PCC is replaced by a single-phase nonlinear rectifier load. The two inverters are operated with identical controller parameters and equal current-feedback gains. Therefore, both units are expected to contribute equally to the load demand without using an inter-unit communication link.

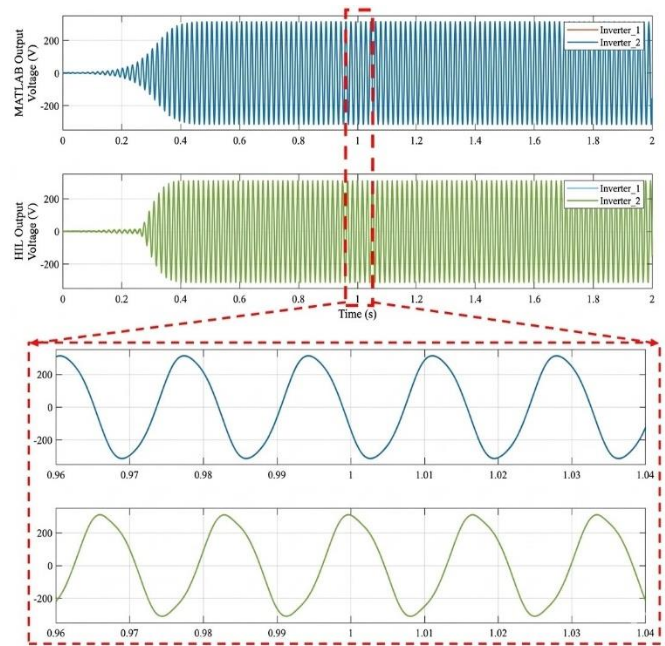



**Fig. 12 Output voltage waveforms under Case 4 (Nonlinear load under 1:1 power sharing) in MATLAB and CHIL**

Figure 12 compares the output-voltage waveforms of the two parallel inverters under the nonlinear rectifier-load condition. Although the nonlinear load draws a distorted current, the output voltages remain nearly sinusoidal in both MATLAB/Simulink and the Controller-Hardware-in-the-Loop (CHIL) results.

The measured voltage peak is approximately 311 V, corresponding to 220 V RMS. The enlarged waveforms between 0.96 s and 1.04 s show close voltage-amplitude agreement and phase alignment between the two inverters. These results indicate that the proposed Van der Pol-based VOC preserves voltage synchronization and nominal voltage regulation under the tested nonlinear-load condition.

Figure 13 compares the inverter output currents obtained in MATLAB/Simulink and the controller-hardware-in-the-loop test when the common PCC load is replaced by a nonlinear rectifier load. The current waveforms are non-sinusoidal and contain pronounced positive and negative peaks, confirming that the load introduces a distorted current demand. Despite the nonlinear loading condition, the current waveforms of Inverter 1 and Inverter 2 remain closely matched in both platforms.

The enlarged views between 0.96 s and 1.04 s show that the two inverters supply similar current pulses during each conduction interval. These results provide qualitative evidence that the proposed Van der Pol-based VOC maintains approximately equal current sharing under the tested nonlinear-load condition.

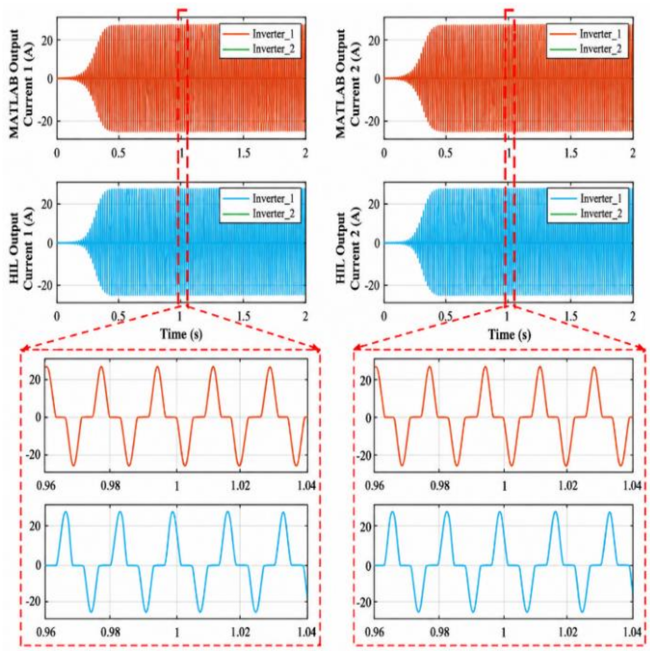
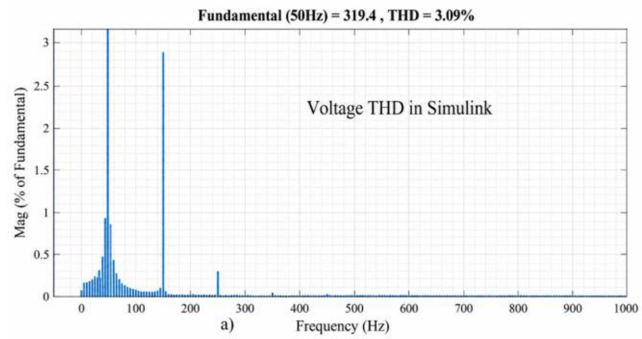
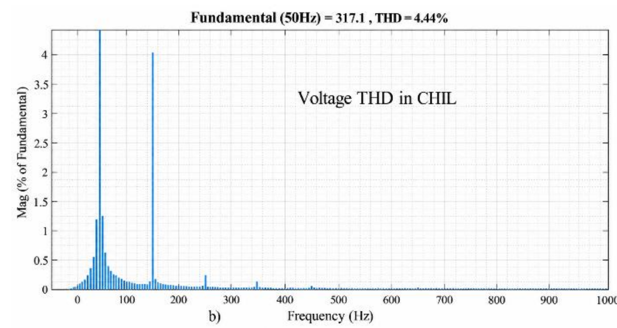



**Fig. 13 Output current waveforms under Case 4 (Nonlinear load under 1:1 power sharing) in MATLAB and CHIL**

The voltage harmonic spectra of the MATLAB/Simulink simulation and the HIL implementation for Case 4 (1:1 power sharing with a nonlinear load) are shown in Figure 14. In both cases, the major voltage component is the fundamental frequency of 50 Hz, whereas harmonic components are quite tiny. The spectra present comparable harmonic structures. The most visible low-order components are about 150 Hz and 250 Hz, corresponding to the third- and fifth-order harmonics. The voltage THD is 3.09% for MATLAB/Simulink simulation and 4.44% for CHIL implementation. The CHIL is 1.35 percentage points higher, but is still below the total voltage-distortion limit of 8% as per IEEE Std 519-2014 for a PCC voltage of up to 1 kV. The discrepancy is due to real-time implementation issues such as sampling and quantization, finite numerical precision, measurement noise and delays in control execution. The harmonic spectra of the simulation and HIL are in good agreement, which confirms the validity of the suggested control approach under nonlinear-loading situations. Although the load current harmonic distortion is high, the THD of voltage is restricted, which means the system is functioning with the anticipated power sharing ratio of 1:1, and the voltage quality is adequate.

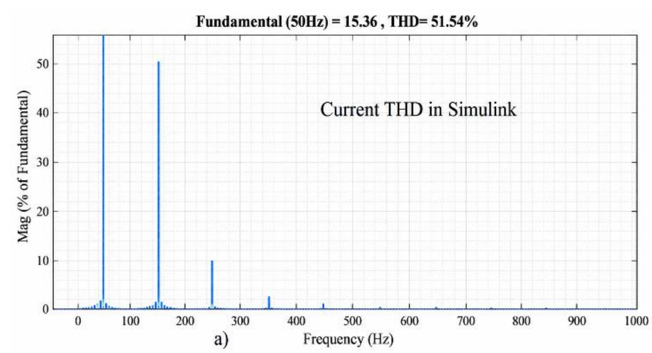



**(a)**

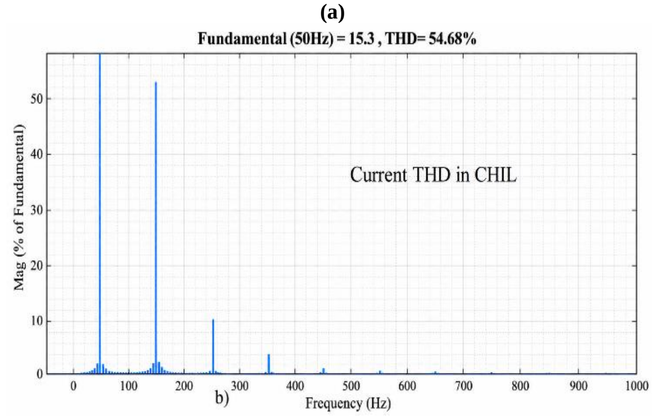



**(b)**

**Fig. 14 Voltage harmonic spectra and THD results under Case 4 (Nonlinear load with 1:1 power sharing): (a) MATLAB/Simulink simulation, and (b) CHIL implementation.**




**(a)**




**(b)**

**Fig. 15 Current harmonic spectra and THD results under Case 4 (Nonlinear load with 1:1 power sharing): (a) MATLAB/Simulink simulation, and (b) CHIL implementation.**

The comparison between the current harmonic spectra derived from MATLAB/Simulink model and HIL test is shown in Figure 15. The two results reveal a similar distribution of harmonics. The major low-order components are located at 150 Hz and 250 Hz, i.e. at the third-and fifth-order harmonics, respectively. These components are mostly on account of nonlinear load. Currently, the THD is 51.54 % in the simulation and 54.68 % in the HIL test. The HIL value is a little higher, although the difference is minor, roughly 3.14 percentage points. This variance is to be expected as the HIL platform incorporates actual phenomena that are not fully modeled in the simulation, such as sampling and numerical mistakes, signal noise and implementation delays. Overall, the HIL findings are in good agreement with the simulation results, which validates the suggested control approach under nonlinear loading. The high current THD further proves the considerable influence of the nonlinear load on the current waveform.

## 5. Conclusion

This paper presented a Van der Pol-based Virtual Oscillator Control (VOC) strategy for two parallel single-phase inverters operating in an islanded AC microgrid. The proposed controller generates the voltage reference of each inverter from locally measured output-current feedback and does not require an inter-unit communication link. A parameter-selection procedure was applied to determine the oscillator and scaling parameters based on the inverter ratings, nominal operating conditions, transient-response requirements, and harmonic-design targets. The proposed method was evaluated in MATLAB/Simulink and in a CHIL setup using a TMS320F28379D DSP and a Typhoon HIL 402 real-time simulator. The test cases included equal 1:1 sharing, unequal 1:2 sharing, resistive load changes, and a nonlinear rectifier load. Under the resistive-load conditions, the inverter voltages remained synchronized near 220 V RMS, while the output currents followed the intended sharing ratios. Under the nonlinear-load condition, the voltage THD was 3.09% in the MATLAB/Simulink simulation and 4.44% in the CHIL test. The CHIL voltage THD remained below the 8% total voltage-distortion limit specified in IEEE Std 519-2014 for PCC voltages not exceeding 1 kV.

The agreement between the simulation and CHIL results indicates that the proposed VOC can be implemented for communication-free operation of two parallel inverters under the tested conditions. Future work will include validation using a physical power-converter prototype, investigation of a broader range of nonlinear-load conditions, and extension to multi-inverter and three-phase microgrids.

## Acknowledgments

This research was supported by Hung Vuong University, Phu Tho province, Vietnam (Code HV32.2024).

## References

[1] Qiang Lin et al., "Field Demonstration of Parallel Operation of Virtual Synchronous Controlled Grid-Forming Inverters and a Diesel Synchronous Generator in a Microgrid," *IEEE Access*, vol. 10, pp. 39095-39107, 2022. [CrossRef] [Google Scholar] [Publisher Link]

[2] Vikash Gurugubelli, Arnab Ghosh, and Anup Kumar Panda, "Parallel Inverter Control using Different Conventional Control Methods and an Improved Virtual Oscillator Control Method in a Standalone Microgrid," *Protection and Control of Modern Power Systems*, vol. 7, no. 1, pp. 1-13, 2022. [CrossRef] [Google Scholar] [Publisher Link]

[3] Hua Han et al., "Review of Power Sharing Control Strategies for Islanding Operation of AC Microgrids," *IEEE Transactions on Smart Grid*, vol. 7, no. 1, pp. 200-215, 2016. [CrossRef] [Google Scholar] [Publisher Link]

[4] M.C. Chandorkar, D.M. Divan, and R. Adapa, "Control of Parallel Connected Inverters in Standalone Ac Supply Systems," *IEEE Transactions on Industry Applications*, vol. 29, no. 1, pp. 136-143, 1993. [CrossRef] [Google Scholar] [Publisher Link]

[5] Qing-Chang Zhong, and Yu Zeng, "Universal Droop Control of Inverters with Different Types of Output Impedance," *IEEE Access*, vol. 4, pp. 702-712, 2016. [CrossRef] [Google Scholar] [Publisher Link]

[6] Vivek Khatana, Soham Chakraborty, and Murti V. Salapaka, "A Plug and Play Distributed Secondary Controller for Microgrids with Grid-Forming Inverters," *IECON 2024 - 50th Annual Conference of the IEEE Industrial Electronics Society*, Chicago, IL, USA, pp. 1-6, 2024. [CrossRef] [Google Scholar] [Publisher Link]

[7] Qing-Chang Zhong, "Robust Droop Controller for Accurate Proportional Load Sharing Among Inverters Operated in Parallel," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 4, pp. 1281-1290, 2013. [CrossRef] [Google Scholar] [Publisher Link]

[8] Zilin Li et al., "Adaptive Droop Control using Adaptive Virtual Impedance for Microgrids with Variable PV Outputs and Load Demands," *IEEE Transactions on Industrial Electronics*, vol. 68, no. 10, pp. 9630-9640, 2021. [CrossRef] [Google Scholar] [Publisher Link]

[9] Brian B. Johnson et al., "Synthesizing Virtual Oscillators to Control Islanded Inverters," *IEEE Transactions on Power Electronics*, vol. 31, no. 8, pp. 6002-6015, 2016. [CrossRef] [Google Scholar] [Publisher Link]

[10] Siyi Luo et al., "A New Virtual Oscillator Control without Third-Harmonics Injection For DC/AC Inverter," *IEEE Transactions on Power Electronics*, vol. 36, no. 9, pp. 10879-10888, 2021. [CrossRef] [Google Scholar] [Publisher Link]

[11] Mingshen Li et al., "Advanced Synchronization Control for Inverters Parallel Operation in Microgrids using Coupled Hopf Oscillators," *CPSS Transactions on Power Electronics and Applications*, vol. 5, no. 3, pp. 224-234, 2020. [CrossRef] [Google Scholar] [Publisher Link]

[12] Brian B. Johnson et al., "Synchronization of Parallel Single-Phase Inverters with Virtual Oscillator Control," *IEEE Transactions on Power Electronics*, vol. 29, no. 11, pp. 6124-6138, 2014. [CrossRef] [Google Scholar] [Publisher Link]

[13] Mohit Sinha et al., "Uncovering Droop Control Laws Embedded within the Nonlinear Dynamics of Van Der Pol Oscillators," *IEEE Transactions on Control of Network*, vol. 4, no. 2, pp. 347-358, 2017. [CrossRef] [Google Scholar] [Publisher Link]

[14] Minghui Lu et al., "Comparison of Droop Control and Virtual Oscillator Control Realized by Andronov-Hopf Dynamics," *IECON 2020 The 46th Annual Conference of the IEEE Industrial Electronics Society*, Singapore, pp. 4051-4056, 2020. [CrossRef] [Google Scholar] [Publisher Link]

[15] Roberto Rosso et al., "Grid-Forming Converters: Control Approaches, Grid-Synchronization, and Future Trends-A Review," *IEEE Open Journal of Industry Applications*, vol. 2, pp. 93-109, 2021. [CrossRef] [Google Scholar] [Publisher Link]

[16] Sara Anttila et al., "Grid Forming Inverters: A Review of the State of the Art of Key Elements for Microgrid Operation," *Energies*, vol. 15, no. 15, pp. 1-30, 2022. [CrossRef] [Google Scholar] [Publisher Link]

[17] Yuting Teng et al., "Review on Grid-Forming Converter Control Methods in High-Proportion Renewable Energy Power Systems," *Global Energy Interconnection*, vol. 5, no. 3, pp. 328-342, 2022. [CrossRef] [Google Scholar] [Publisher Link]

[18] Brian Johnson et al., "Comparison of Virtual Oscillator and Droop Control," *2017 IEEE 18th Workshop on Control and Modeling for Power Electronics (COMPEL)*, Stanford, CA, USA, pp. 1-6, 2017. [CrossRef] [Google Scholar] [Publisher Link]

[19] Dayan B. Rathnayake et al., "Grid Forming Inverter Modeling, Control, and Applications," *IEEE Access*, vol. 9, pp. 114781-114807, 2021. [CrossRef] [Google Scholar] [Publisher Link]

[20] Gab-Su Seo et al., "Dispatchable Virtual Oscillator Control for Decentralized Inverter-Dominated Power Systems: Analysis and Experiments," *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Anaheim, CA, USA, pp. 561-566, 2021. [CrossRef] [Google Scholar] [Publisher Link]

[21] Langella, Roberto, Testa, Alfredo, and, Alii, "IEEE Recommended Practice and Requirements for Harmonic Control in Electric Power Systems," *IEEE Recommended Practice*, 2014. [Google Scholar] [Publisher Link]

[22] F. Blaabjerg et al., "Overview of Control and Grid Synchronization for Distributed Power Generation Systems," *IEEE Transactions on Industrial Electronics*, vol. 53, no. 5, pp. 1398-1409, 2006. [CrossRef] [Google Scholar] [Publisher Link]

[23] M. Ali, H.I. Nurdin, and J.E. Fletcher, "Synthesizing Averaged Virtual Oscillator Dynamics to Control Inverters with an Output LCL Filter," *IECON 2020 - 46th Annual Conference of the IEEE Industrial Electronics Society*, Singapore, pp. 3265-3270, 2020. [CrossRef] [Google Scholar] [Publisher Link]

[24] Minghui Lu, Sairaj Dhople, and Brian Johnson, "Benchmarking Nonlinear Oscillators for Grid-Forming Inverter Control," *IEEE Transactions on Power Electronics*, vol. 37, no. 9, pp. 10250-10266, 2022. [CrossRef] [Google Scholar] [Publisher Link]

[25] Minghui Lu et al., "Adaptation of Commercial Current-controlled Inverters for Operation with Virtual Oscillator Control," *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Anaheim, CA, USA, pp. 3427-3432, 2019. [CrossRef] [Google Scholar] [Publisher Link]