Design and Analysis of 16-Bit Pipelined Subranging SAR ADC and TDC

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Abstract

Analog to digital converters plays an important role in medical and signal processing applications. This paper proposes a 16-bit time based analog to digital converter (ADC) architecture by combining SAR Analog to Digital Converter and Vernier Time to Digital Converter. SAR analog to digital Converter is best suited for low power, high resolution and moderate applications. Vernier Time to Digital Converter with a high resolution to increase the conversion gain of VTC. The SAR ADC and Vernier TDC are pipelined to increase the conversion speed and reduce the area, power dissipation significantly smaller. A 16-bit combined pipelining SAR ADC and Vernier TDC was designed and simulated in Tanner EDA Tool.

Keywords - *Successive Approximation Register, Time to Digital Converter, Voltage to Time Converter.*

I. INTRODUCTION

Analog to Digital Converters are essential components in digital world. One crucial element in the data communication is the Analog-to-Digital Converter (ADC), converting the real-life electric signals through the air to the original digital message .There are different types of analog to digital converters ,depending on their characteristic we choose them for specific applications .

Successive approximation register based analog to digital converters are mainly used for low power applications. SAR ADC converts analog data to digital data by binary search algorithm. It is more power efficient and consumes less area when compared to other analog to digital converters.

Time to digital converter basically measures time information of one or more discrete amplitude signals and provides digital representation for further signal processing.

In time based digital approach, the resolution is no longer dependent on sampling clock but depends on propagation of a delay gate which lowers with technology scaling.

With these advantages of scaling, promising digital TDC implementation is preferable for ADC.

Vernier Time to Digital Converter used in high resolution and high speed operation. Mismatching delay is low due to same delay.

II.RELATED WORK

Yongs Heng Xu , Ge Wu , Life Fellow , presents a 5-bit non interleaved time based analog to digital converter (ADC).It operates at 5-Gs/s rate. The ADC is designed for the used in radio astronomy telescopes for which time interleaving is not acceptable.The ADC employs a dynamic , differential voltage to time converter . A Folded Flash time to digital converter and calibration circuitry to generate reference delays .The calibration circuitry utilizes a delay time reference network. The ADC achieves the signal to Noise pulse distortion ratio. The low power consumption is 21.5mw Nyquist. But the problem is low speed , need more capacitance .

Suspeng Liu , Yuajin Zheng , are presented a Time to digital converter (TDC) architecture capable of achieving subgate delay resolution and large detection range at same time with low power consumption. The TDC is based on parallel sampling ring oscillator with power gating and dynamic element matching . The time resolution is determined by delay difference between successive sampling clocks instead of buffer delay .The barrel shift algorithm achieve immunity to leakage issues and mitigates buffer mismatch impact. It achieves high linearity , and the single shot precision is less than 11ps. But the power consumption is less , pulse width is too large.

Xinpeng Xing, Georges G.E Gielen, Fellow presents a 42 fJ/Step -FoM Two –step VCO Based Delta Sigma ADC in 40-nm CMOS. The nonlinearity of coarse and fine VCO based quantizers are mitigated by distortion cancellation and voltage swing reduction schemes respectively. The intrinsic DEM of VCO based quantizer output, the matching requirement of ADC cells are greatly relaxed. The design is implemented in 40nm CMOS technology. It achieves open loop structure, high bandwidth, and also robust performance. But it blocks the propagation delays and more noise distortion

III.PROPOSED ARCHITECTURE

In our proposed method, an architecture of combining 16-bit SAR ADC and Vernier TDC to

achieve both high speed and high resolution. Combining 16-bit SAR ADC and Vernier TDC by using pipelining.

Pipelining is speed comparable to parallel architecture. The concurrent operation of the stages that is at any time, the first stage operates on the most recent sample while all other stages operate on residues from previous samples. Once pipelined is primed, converted digital data are always available at every clock cycle.

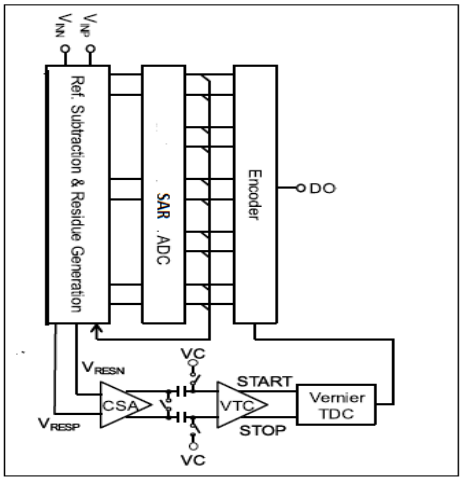


Fig 1: Block diagram of 16-bit subranging ADC

It consists of SAR ADC, Reference subtraction and residue generation circuit, charge steering amplifier, vernier TDC and VTC.

IV.CIRCUIT ANALYSIS

A.Sar Adc

SAR analog to digital converter consists of comparator, successive approximation register and includes sample and hold circuit.

SAR ADC has three phases of operation namely, sampling phase, hold phase , redistribution phase.

In sampling phase all switches are connected to top plates of capacitor and VIN samples are connected are connected bottom plates. In Re-distribution phase digital data determines the status of the control switches and actual conversions will take place. In hold phase bottom plates are connected to capacitors and switches are open.

Initially input voltage is sampled and SAR register is reset to 0. Conversion starts with setting MSB of SAR register to logic '1', now the DAC output is VREF/2. If VIN is more than VOUT ,the output of comparator is set to logic '1' and MSB is retained as logic '1' and else MSB is reset to logic '0'.

B. Reference Subtraction and Residue Generation

The reference subtraction and residue generation circuits are merged to reduce the circuit area and power dissipation. In tracking phase input analog signal is stored in capacitor C, by turning ON switches. The reference subtraction is performed by turning ON switches, Vref-Vinp is generated. In the residue generation phase, either S1 or S2 turns ON in accordance with the comparator output. Moreover charge redistribution is performed and residue signal is generated.

C. Voltage to Time Converter

The voltage to time converter is comprised of differential pair in which loads are made up of two capacitors. It consumes no dc current and it does not dissipate much power. Its linearity is poor. The VTC has two operation phases conversion phase and reset phase. In reset phase , the control signal RAMP is low and the nodes DN and DP are precharged to VDD. In the conversion phase RAMP becomes high. And the MOS transistor is ON. The input voltages are determined by discharging loads of the capacitors. Vernier TDC with high time resolution to suppress the increase in the conversion gain of the dynamic VTC. The combination enables a high speed and high linearity operation.

D. Charge-Steering Amplifier

In our proposed architecture, the residue has to be transferred between first and second pipeline stages. Two methods are used for residue transfer. In first method uses a residue amplifier such as pipeline ADC. It consumes a large amount of dc power. In second method uses charge redistribution. However, the transferred signal is halved because of charge sharing.

In reset phase, the clock signal becomes low and the nodes are precharged to VDD. And then phase changes to amplification phase when clock signal becomes high. The residue signal generated in the first stage is amplified by a two stage CSA and transferred to the second stage. The gain of charge steering amplifier is designed to be one.

The gain can be adjusted by the voltage of the gain control signal. The voltage difference between BP and BN is transferred to OUTP and OUTN.

E. Vernier TDC

In vernier TDC uses two delay lines fast and slow delay lines with different delay times. The time resolution is determined by the difference between the delay times of two delay lines.

Once the delay operation starts when the input signal rises. Only one MOS transistor is connected to the output node. The delay time and power consumption are less than inverter delay circuit. The node of FINISH is precharged to VDD. After the start and stop signal rise the node of FINISH overtake the signal in the fast delay line. The reset signals are generated immediately after FINISH becomes low. And the waste signal propagation can be stopped, resulting in a power saving.

V.RESULT AND ANALYSIS

Fig 2: 16-bit SAR ADC

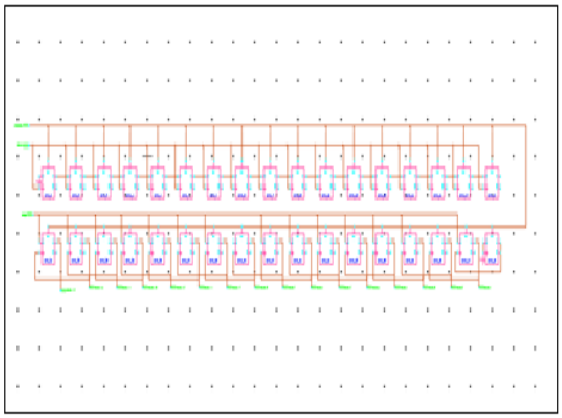


Fig 3: Refernce substraction and Residue Generation

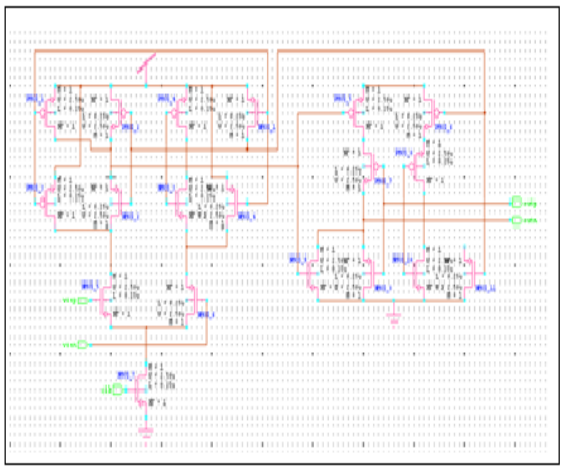


Fig 4:Voltage to Time Converter

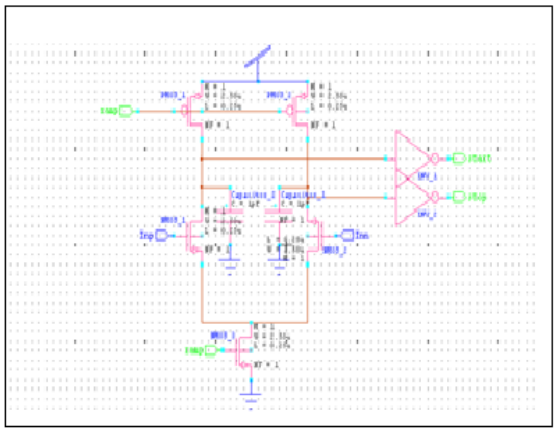


Fig 5: Charge Steering Amplifier

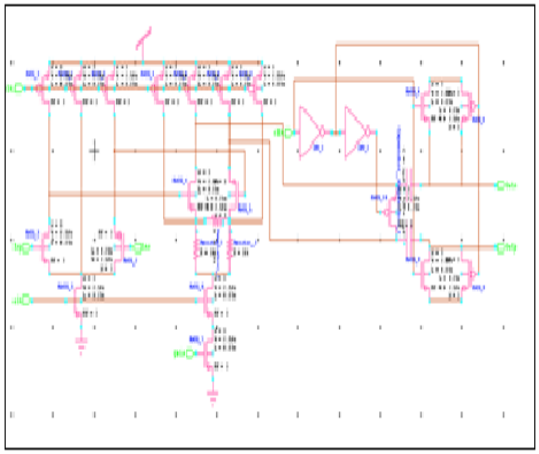


Fig 6: Vernier TDC

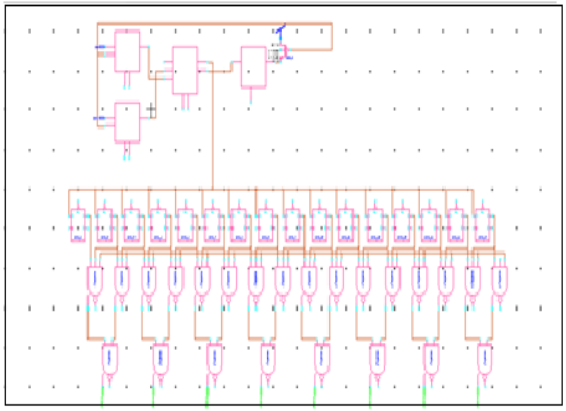


Fig 7: 16-bit Pipelined Subranging SAR ADC and Vernier TDC Architecture

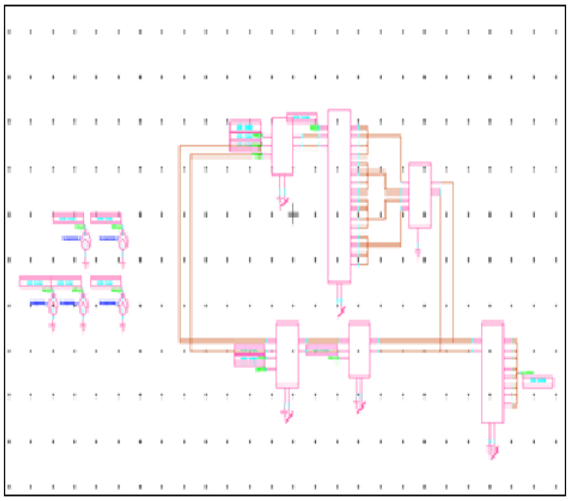


Fig 8: Output Waveform of 16-bit Pipelined Subranging SAR ADC and Vernier TDC Architecture

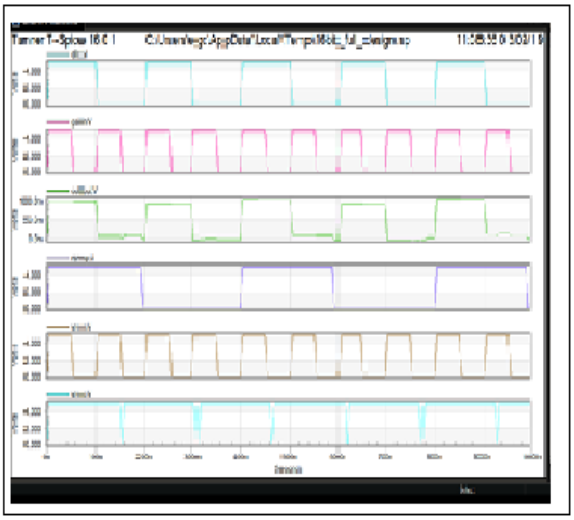


Fig 9: Pipelined SAR ADC with combined GRO based TDC Architecture

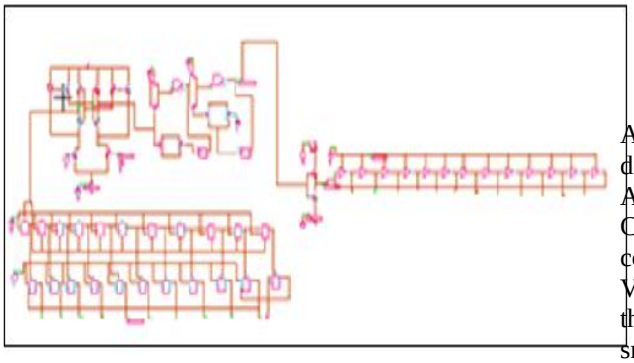
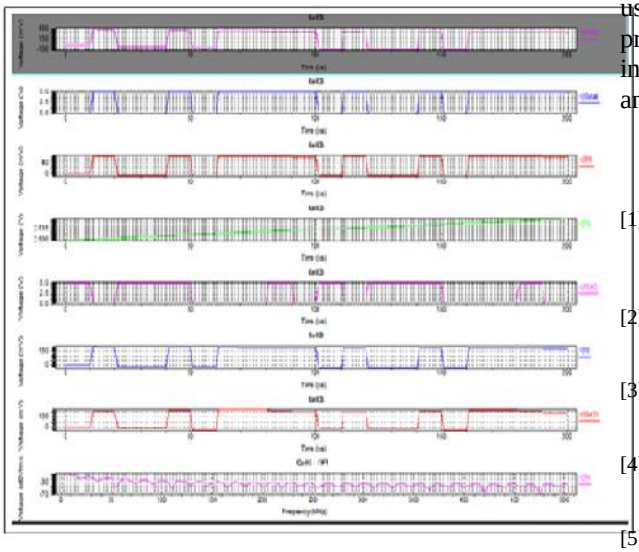


Fig 10: Output wave forms of SAR ADC with combined GRO based TDC architecture



VI. PERFORMANCE ANALYSIS OF DIFFERENT TYPES OF ADC AND TDC

Table 1.1 Shows that the parameters like Resolution, Power and Number of Transistors are compared with different types of ADC and TDC.

LOGIC	Power (uw)	Resolution (bits)	Number of Transistors
Flash ADC	2.500	10	140
SAR ADC with GRO based TDC	4.21	10	32
SAR ADC with Vernier TDC	5.07	16	43

VII. CONCLUSION

The combining pipelined sub ranging 16-bit SAR ADC and Vernier TDC is proposed. The Proposed design aims at low power consumption. 16-bit SAR ADC is used in high resolution applications. Conversions are done in many cycles with only one comparator. 16-bit SAR ADC is combined with Vernier TDC by using pipelining. Pipelining reduces the implementation area and power dissipation is smaller. Vernier TDC circuit is simple and used in high speed operation. The architecture consumes less area and power. The design and simulation done by using Tanner EDA Tool. It is used in signal processing and low power applications. In future to increase the resolution and use different types of ADC and TDC for reducing area, and Power Dissipation.

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