Implementation of Low Power High Speed Hybrid Adder in Radix - 4 Booth Multiplier

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Abstract

Adders are very important in Digital Signal Processing (DSP) for filter designing. It is profoundly accepted that the main processing unit of any device capable of carrying out computations is the Central Processing Unit (CPU). The most fundamental and integral part of CPU is an Arithmetic and Logical Unit (ALU). Adders are the primary and indispensable component of ALU. There are various adders available in the literature such as Ripple carry adder (RCA), Carry look ahead adder (CLA), Carry Skip adder (CskA) and Carry increment adder (CIA), etc. In this paper, a new hybrid adder is designed by combining the two significant adders such as Carry Skip adder and Carry increment adder. The hybrid adder has two main peripheral components namely RCA and Multiplexer. Then, the hybrid adder is implemented in Radix-4 booth multiplier. In this paper, the GDI technique is applied to design a new low power high speed Radix-4 booth multiplier. Simulation is done using Tanner EDA tool in 180nm technology and the results obtained shows a significant improvement in power consumption and delay

Keywords - *Carry Increment adder, Carry Skip adder, Gate Diffusion Input (GDI) Technique, Hybrid adder,Radix-4 Booth multiplier.*

I. INTRODUCTION

Very Large-Scale Integration is the process of creating an Integrated Circuit by combining thousands of transistors into a single chip. Multipliers are main components of many high-performance systems such as FIR filters, microprocessors, digital signal processors, etc. A system's performance is generally determined by the performance of the multiplier because the multiplier is generally the slowest element in the system. Furthermore, it is generally the most area consuming. Multiplication is a fundamental operation in most signal processing algorithms. Multipliers have large area, long latency and consume considerable power. Therefore low-power multiplier design has been an important part in low- power VLSI system design. Fast multipliers are essential parts of digital signal processing systems. The speed of multiplier operation is of great importance in digital signal processing as well as in the general-purpose processors today. The basic multiplication principle is twofold i.e., evaluation of partial products and accumulation of the shifted partial products

Addition is one of the fundamental arithmetic operations. It is used extensively in many VLSI systems such as application specific DSP architectures and microprocessors. In most of these systems the adder is part of the critical path that determines the overall performance of the system. That is why to enhance the performance of the adder cell, the hybrid adder is one of the significant goals.

Adder is the core element of complex arithmetic circuits like addition, multiplication, division, exponentiation, and so forth. The demand of Very Large-Scale Integration (VLSI) is blooming. In any device capable of bringing about computation Arithmetic Logic Unit (ALU) and Floating - Point Unit (FPU) happens to be the main brain. Arithmetic Logic Unit is responsible for all the logical computations such as addition, subtraction, multiplication, division and logical operations. Adders are the main component of ALU, FPU Multiplier and they are also used in filter designing. So, to make this device faster we need to modify the basic and most heavily used circuit, i.e, Adders.

The semiconductor industry has witnessed an explosive growth of integration of sophisticated multimedia-based applications into mobile electronics gadgetry since the last decade. However, the critical concern in this arena is to reduce the increase in power consumption beyond a certain range of operating frequency. The main problems that a design engineer faces from time to time are the management between: Delay, Area and power consumptions.

Different logic styles tend to favour, one performance aspect at the expense of the others. The logic style used in logic gates basically influences the speed, size, power dissipation, and the wiring complexity of a circuit. The circuitdelay is determined by the number of inversion levels, the number of transistors in series, transistor sizes (i.e., channel widths), and the intra cell wiring capacitances. Circuit size depends upon the number of transistors, their sizes and on the wiring complexity. Some of them use one logic style for the whole full adder while the other use more than one logic style for their implementation.

An adder is a digital circuit that performs addition of numbers. In many computers and other kinds of processors adders are used in the arithmetic logic units or ALU. They are also utilized in other

parts of the processor, where they are used to calculate addresses, table indices, increment and decrement operators and similar operations.

Adders are the main component of ALU, Floating point unit (FPU) Multiplier and they are also used in filter designing. So, to make these devices faster we need to modify the basic and most heavily used circuit, i.e. Adders. Adders are classified into various types. They are, Half adderand Full adder.

HALF ADDER:

A device capable of computing the sum of 2 bits as input and producing two outputs which are Sum and Carry is called Half Adder. It is an example of one of the simplest functional digital circuit which can be implemented using just two logic gates.

LOGICAL OPERATION:

- The output sum will be high when any one from the input – A or B in the high state.
- If both A and B are high or low, the sum will be 0.
- Carry bit will only be high when both the inputs are high.

The equations representing the sum and carry of the half adder are,

The sum can be represented as:

$$Sum = A'B+AB'$$

The carry can be represented as:

$$Cout = A.B$$

FULL ADDER:

If a device capable of computing the sum of 3 bits as input and producing two outputs which are Sum and Carry is called Full Adder. A full adder circuit adds binary numbers and an account for the values carried in as well as out, it is a combinational circuit that performs the addition operation of three inputs, A, B and Carry in (Cin). There are 8 possible input combinations for each case of sum(S) and carry out (Cout). The Full adder circuit is represented based on simple logical gates.

The equations representing the sum and carry of the full adder are, The sum can be represented as:

$$Sum = A \text{ XOR } B \text{ XOR } C$$

The carry function is given by:

$$Cout = AB + BC + CA$$

There are so many ways to design the Full Adder. A few logics to design a full adder are: Complementary metal oxide semiconductor devices (CMOS), Complementary pass logic (CPL), and Transmission Gate (TG) logic.

As the demand of high computational speed along with compact area and low power consumption is becoming indispensable, it's very important for the most fundamental components to be highly efficient.

Hybrid adder is the combination of two different adders or implementing a new logic style in the conventionally existing adders. In hybrid adders, the addition is performed using two adders. The addition of Least Significant Bit (LSB) is carried out by one adder and the Most Significant Byte (MSB) is carried out by another adder. The main objective to design hybrid adder is to take up the advantages of the adders connected to make it more efficient than individual adder.

ADVANTAGES OF HYBRID ADDER:

- High Speed,
- Reduce Power consumption,
- Reduction transistor counts,
- Minimize the delay.

APPLICATIONS OF HYBRID ADDER:

- Cellular phones,
- Smart cards,
- Laptops.

In this project, a new hybrid adder is designed by combining Carry Skip adder and Carry Increment adder. Further, Gate Diffusion Input Technique (GDI Technique) is used. The proposed hybrid adder using GDI Technique has several advantages over the conventional hybrid adders like improved in power consumption and delay. The proposed hybrid adder is then implemented in Radix-4 booth multiplier to improve the power consumption and delay.

II. LITERATURE REVIEW

Power consumption and propagation delay is tuned by sizing the transistors. This [1] adder operates successfully on low voltages and provides full output voltage swing and thus exhibits a smaller power delay product at low voltages. In this paper, the transmission gates are used for Multiplexer.The 6T XNOR is connected with Carry propagation adder to fasten the process. [2] Compared with 6T XOR/XNOR, the modified 6T XNOR offered low-power and high-speed. In [3] existed 6 transistors XNOR module is replaced with 4 transistors XNOR module. This modified XNOR module is responsible for most of the power consumption of the entire adder circuit. Due to this reduction of the transistor the performance of the adder is improved. If supply voltage is above the threshold voltage, then in [4] suggested to use PTL-GDI adder, instead if the adder is used in the wide range of supply voltages, then the author suggested to use GDI design.

III. GDI BASED HYBRID ADDER

The circuit diagram of the 4-bit Hybrid adder is shown in figure 1. It consists of two adders. The hybrid adder is either designed by combining two separate adders or by implementing a logic styles in the existing adder. The two adders which are used for the design of hybrid adder are Carry skip adder and Carry increment adder.

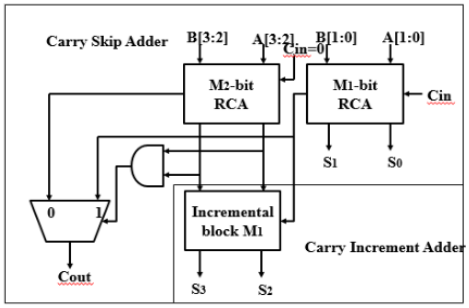

Fig 1 Circuit diagram of 4-bit Hybrid Adder

A carry-skip adder (CSkA) is also known as a carry-bypass adder. This is an adder implementation that improves on the delay of a ripple carry adder with little effort compared to other adders. In this proposed, hybrid adder the Carry Skip adder consists of Ripple Carry Adder (RCA), AND gate and Multiplexer. The RCA circuit is designed simply by cascading Full adder blocks. The carry-out of any full adder is propagated to the next stage as carry-in and the calculation continues in the next block.

ADVANTAGES OF CSkA

- Critical pathdelay is much smaller than RCA.
- Efficient in terms of power consumption and area usage.
- Power delay product is smaller than those of carry select adder and parallel prefix adder structure.
- Benefits from relatively short wiring lengths as well as a regular and simple layout.

The AND gate is used to generate the select line input for the Multiplexer. The input of the AND gate would be the propagate value of the M2-bit RCA. The input of the Multiplexer would be the Cout of the M1-bit RCA and the M2-bit RCA.

The Conventional Full adder and Multiplexer are the two main peripheral components of this hybrid adder: by the optimized design of these two components low power high speed hybrid adder can be obtained. The Figure 1 shows the Circuit diagram of 4-bit Hybrid adder.

A multiplexer (or mux) is a device that selects one of several analog or digital input signals and forwards the selected input into a single line. A multiplexer of inputs has select lines, which are used to select which input line to send to the output. Multiplexers are mainly used to increase the amount of data that can be sent over the network within a certain amount of time and bandwidth. A multiplexer is also called a data selector. Multiplexers can also be used to implement Boolean functions of multiple variables. In analog circuit design, a multiplexer is a special type of analogswitch that connects one signal selected from several inputs to a single output. In digital circuit design, the selector wires are of digital value. In the case of a 2-to-1 multiplexer, a logic value of 0 would connect I0 to the output while a logic value of 1 would connect I1 to the output. In larger multiplexers, the number of selector pins is equal to where is the number of inputs. Figure 2 represents the circuit diagram of 2 to 1 Multiplexer. A 2-to-1 multiplexer has a boolean equation where 'A' and 'B' are the two inputs, S is the selector input, and Z is the output,

$$Z = (A.S') + (B.S)$$

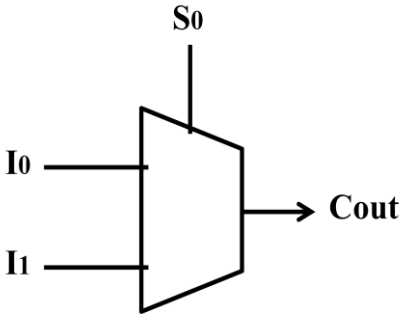

Fig 2 Circuit diagram of 2 to 1 Multiplexer

A Carry Increment Adder, an adder implementation that uses HA blocks for carry propagation. Carry propagation in HA is much faster than that of FA. That's why the total propagation delay in CLA is much less that other adder circuits. First two sums from the RCA is directly taken from the block, but rest is calculated from the carry-out of the first block and rest input through conditional incremental circuit. Second block will continue the operation by summing and creating carry-out. Incremental circuit is containing Half Adders. The increment operation will take place based on the carry-out of the 1st block.

As carry propagation delay is less in half adder than in full adder so, the total propagation delay through the increment adder is less. As the incremental circuit contains Half Adder it takes less time to generate the carry, so the delay is less than RCA circuit.

ADVANTAGES OF CIA

- Circuit complexity is less.
- It has a simple and regular layout in comparison with Carry Look Ahead Adder.
- Effective in higher (more numbers of) bit operation.

The GDI Logic based full adder consists of only 10 transistors to implement the sum and carry function. The Circuit delay is determined by the number of inversion levels, the number of transistors in series, transistor sizes (i.e., channel widths), and the intra cell wiring capacitances. Circuit size depends upon the number of transistors, their sizes and on the wiring complexity. Figure 3 represents the Circuit diagram of 4-bit Hybrid adder using GDI technique.

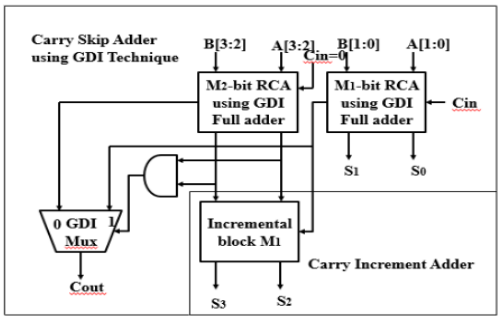

Fig.3 Circuit Diagram of 4-bit Hybrid adder using GDI Technique

In GDI logic based full adder, only 10 transistors are used to implement the sum and carry function. The sum and carry cell are implemented in a cascaded way i.e. firstly the XOR cell is implemented and then using that XOR as input, sum as well as carry cell is implemented. For GDI adder the sum as well as carry cell is designed using GDI technique. The advantage of this adder is if this adder is to be used in a wide range of supply voltages (for example 0.8V-3V), then this GDI design is suggested to use. Figure 4 represents the circuit diagram of Ripple carry adder using GDI technique.

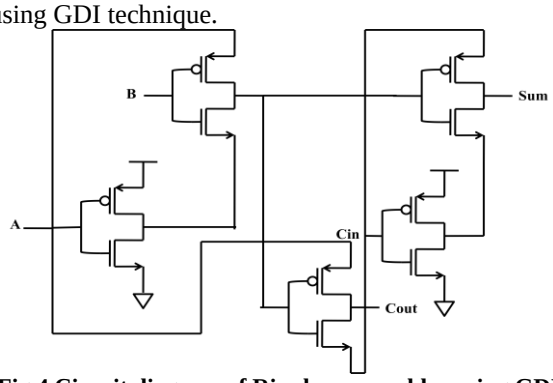

Fig.4 Circuit diagram of Ripple carry adder using GDI technique

The GDI method is based on the use of a simple cell. At the first look the design is seems to be like an inverter, but the main differences are the connections. Figure 5 shows the circuit diagram of GDI Multiplexer. GDI multiplexer consists of only two transistors. By using this GDI technique, the power consumption is reduced with the delay because it uses minimum number of transistors to calculate the output.

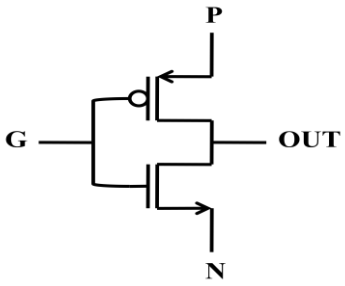

Fig 5 Circuit diagram of GDI Multiplexer

Incremental circuit is a part of the hybrid adder using GDI techniques. The incremental circuit that uses half adder (HA) blocks for carry propagation. Carry propagation in HA is much faster than that of full adder (FA). That's why the total propagation delay in CLA is much less that other adder circuits. First two sum from the RCA is directly taken from the block, but rest is calculated from the carry-out of the first block and rest input through conditional incremental circuit. Second block will continue the operation by summing and creating carry-out. Incremental circuit is containing Half Adders. The increment operation will take place based on the carry-out of the 1st block.

As carry propagation delay is less in half adder than in full adder so, the total propagation delay through the increment adder is less. As the incremental circuit contains Half Adder it takes less time to generate the carry, so the delay is less than RCA circuit.

IV. IMPLEMENTING GDI BASED HYBRID ADDER IN RADIX-4 BOOTH MULTIPLIER

The block diagram of the Radix-4 booth multiplier is shown in figure 6. It consists of four basic components. They are,

- ✓ Booth Encoder
- ✓ Booth Decoder
- ✓ Partial product
- ✓ Hybrid adder

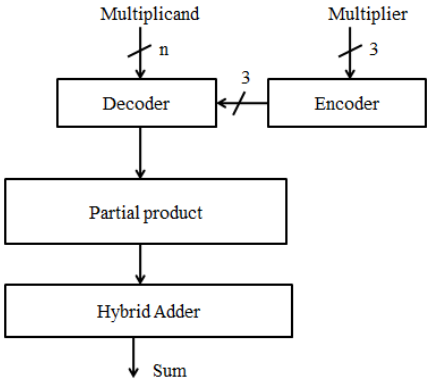

Fig 6 Block diagram of the Radix-4 booth multiplier.

The Booth encoder/decoder is the first part of the multiplier when we start to calculate the value of multiplicand and multiplier.The Booth encoder/decoder makes the calculation faster. The radix-4 modified booth encoder is useful for the parallel multiplier by 3-bit encoding if the bit number of the operation is not incredibly large. The n-bit multiplier input, denoted as X, is divided into 3-bit groups for the Booth encoder.The encoded information is for the n-bit multiplicand input, which is represented as Y, to get the n/2 rows partial product

valueafter the decoding. After the decoder, we get the (n+3) bits of output at the first row, and the (n+2) bits at the others. There would be 2 bits left and shifted between each row, not including the first row, After the decoder, the sign extention method is used to reduce the processing time The hybrid adder is used to calculate the output, carry out and sum values, to result the final value of the product of X and Y.

The GDI technique is implemented in Radix-4 Booth multiplier wherever it can be implemented such as in Encoder, Decoder, and also in Hybrid adder.

V. RESULTS AND DISCUSSION

The proposed novel hybrid adder is the combination of Carry Skip adder (CSkA) and Carry Increment adder (CIA) which is implemented in the Radix-4 booth multiplier to obtain a low power high speed booth multiplier.The implementation of multiplier is done by using Tanner EDA software.

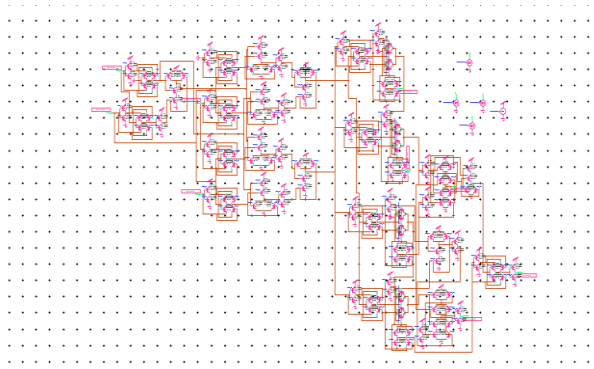

Fig 6 Schematic diagram for 2-bit radix-4 booth multiplier.

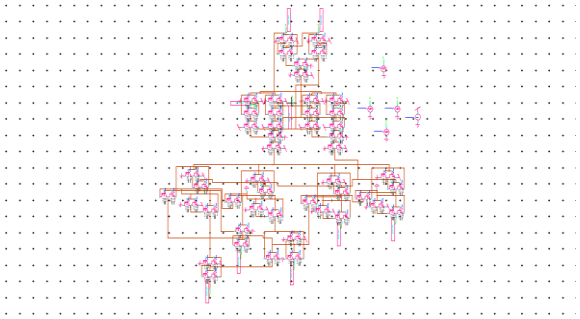

Fig 7 Schematic diagram for a 2-bit radix-4 booth multiplier using GDI Technique

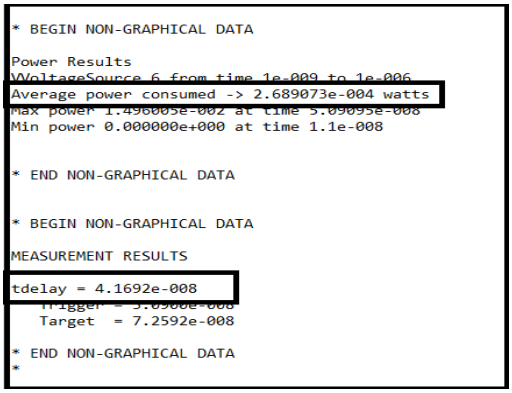

Fig 8 Power and Delay values for 2-bit radix-4 booth multiplier

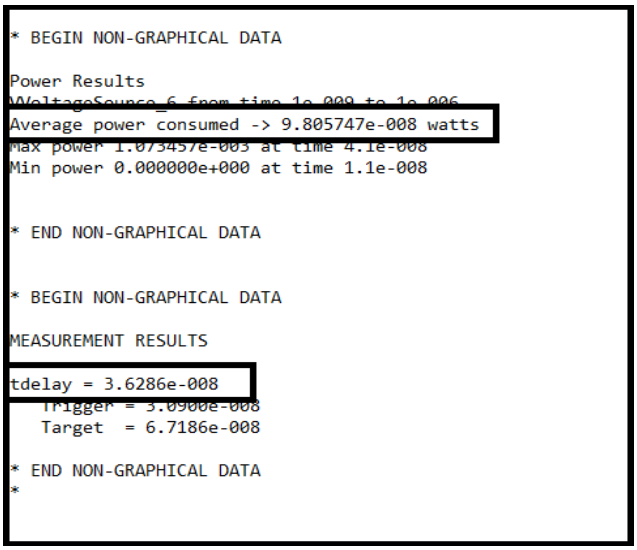

Fig 9 Power and Delay values for 2-bit radix-4 booth multiplier using GDI technique

Table 1 Performance Comparison of Hybrid Adder

Hybrid Adder	Without GDI Technique			With GDI Technique		
	Power (micro W)	Delay (ns)	PDP (pWs)	Power (micro W)	Delay (ns)	PDP (pWs)
4-bit	177.138	29.46	5.218	28.335	20.40	0.578
8-bit	212.012	40.06	8.493	102.837	20.39	2.096
16-bit	413.819	39.85	16.49	148.520	9.319	1.384

The above Table 1 shows the performance comparison of 4-bit hybrid adder using GDI technique which provides 84% of power savings and 30.75% of delay improvement when compared with hybrid adder without GDI technique. The performance comparison of 8-bit hybrid adder using GDI technique which provides 51.49% of power savings and 49.10% of delay improvement when compared with hybrid adder without GDI technique and the performance comparison of 16-bit hybrid adder using GDI technique which provides 49.10% of power savings and 43.48% of delay improvement when compared with hybrid adder without GDI technique.

Table 2 Performance Comparison of Radix-4 booth multiplier

Booth Multiplier	Without GDI Technique			With GDI Technique		
	Power (micro W)	Delay(ns)	PDP (pWs)	Power (micro W)	Delay (ns)	PDP (pWs)
2-bit	268.907	41.69	11.211	98.05	36.28	3.55

The above Table 2 shows the performance comparison of 2-bit Radix-4 booth multiplier using GDI technique which provides 63.5% of power savings and 12.9% of delay improvement when compared with Radix-4 booth multiplier without GDI technique.

V. CONCLUSION

In this project, a novel hybrid adder using Gate Diffusion Input (GDI) technique was designed and it was implemented in Radix-4 booth multiplier to obtain a new low power high speed Booth multiplier. In this project, 4-bit, 8-bit and 16-bit hybrid adders were designed using GDI technique. The 4-bit, 8-bit, and 16-bit hybrid adders design using GDI technique provides 84%, 51.49%, and 49.10% of power savings and 30.75%, 49.10% and 43.48% of delay improvement. This novel hybrid adder was implemented in 2-bit Radix-4 booth multiplier and it provides 63.5% of power saving and 12.9% of delay improvement.Thus, from the simulation results it was observed that the proposed Radix-4 booth multiplier have improved delay and power consumption performances.

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