Analytical Modeling and Simulation of FinFET for Semiconductor memories

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Abstract *— This paper presents a study of the structure and the characteristics of the emerging SOI-FinFET device. Close form models are developed to estimate the values of the surface potential using superposition principle. Using this surface potential model, an expression for Electric field of the SOI-FinFET is derived. These models have been used to investigate the behavior of SOI-FinFET in the sub threshold region like the I-V characteristics, transconductance, output conductance, subthreshold swing and threshold voltage. In addition to analyzing the impact of various geometric parameters on the behavior of the device, the developed models and the presented analysis would be of great importance for numerical TCAD tool development. It is observed that by optimizing these dimensional factors, a sub threshold swing (SS) value very close to 60 mV/decade and a threshold voltage of 0.35 V can be achieved for SOI-FinFET.*

Keywords *— FinFET, Surface Potential, drain current, TCAD.*

I. INTRODUCTION

In this demanding VLSI Industry semiconductor memory plays a major role and occupies a large chip area in many of the VLSI circuit design. As memory consumes a large portion of area in many future designs, scaling of the semiconductor memory density should continue to footstep the scaling trends of logic [1-3]. As semiconductor devices are scaled down to nanometer regime, increase in device threshold voltage, on and off currents thus increases the power dissipations in the semiconductor memories. Low supply voltages must be used, in order to limit the static power dissipations in larger memory devices [4, 5] and is affected by several short channel effects. To cater this FinFETs are already been replacing the conventional planar MOSFETs [6, 7] and due to high caliber to control over the channel, FinFETs obeys a fastest switching rate between 0 and 1. Thus reads a very low operating voltage, a better subthreshold swing (SS) and Drain induced barrier lowering (DIBL). In addition, gate induced drain leakage (GIDL) is constituted to be a limiting factor to achieve low OFF currents (I_{OFF}) [8, 9] and thus can be lowered by increasing the threshold voltage of the device[10-13]. Thus a longer gate length is used by extending over source-drain regions to mitigate short channel effects (SCE) and reduce the leakage currents in the device.

Analytical modeling of semiconductor devices contributes highly useful understanding into device physics. Analytical description of a device exhibits the behavior corresponds to all the internal device parameters and its operation. The modeling of semiconductor devices starts from the basic electrical parameters such as electron density, surface potential, electric field etc., across the channel of the semiconductor device. There are numerous ways to solve the surface potential of the device. Parabolic approximation methods and superposition principles are the most used analytical methods. We employed superposition principle to solve the analytical model of surface potential because of its high accuracy.

Using superposition principle, a two dimensional analytical model has been formulated for electrostatic potential and lateral electric field. In the calculation, it is considered that the mobile charge carriers influencing the electrostatic potential. This paper is formed as follows. In Section II, a 2 D analytical model for the electrostatic surface potential is formulated, followed by lateral electric field, *V-I* characteristics and transconductance. In section III, the proposed analytical modeled results are validated by TCAD device simulator.

II. Device Structure

The 3 dimensional view of Trigate FinFET is shown in Fig 1.a and 2 dimensional cross sectional view is shown in Fig 1.b where L_{Fin}, W_{Fin}, H_{Fin}, t_{ox} and t_{box} are the Length , Width and Height of the channel, oxide thickness and buried oxide thickness respectively. It is assumed that, mobile charge carriers are neglected and source-channel & drain-channel region jumps are abrupt in FinFETs when operating at sub threshold region. Table 1shows all the device parameters of Tri-gate FinFETs.

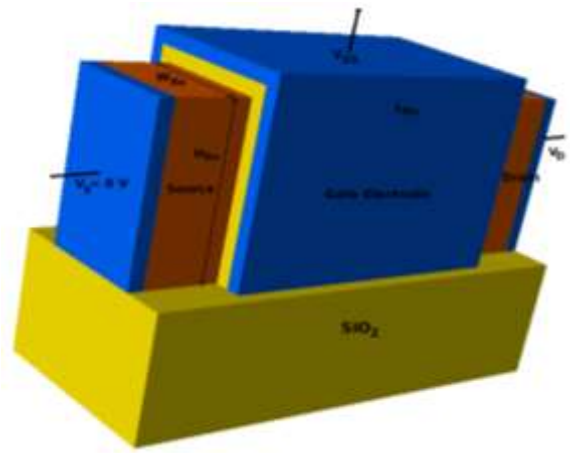

Fig 1.a 3 D view of Trigate FinFET

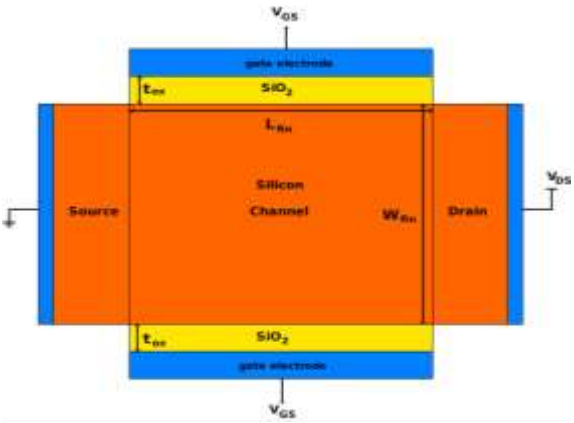

Figure 1.b. 2 Dimensional view of FinFET

Table 1. Device Parameters for FinFET

Sl.No	Parameter	Symbol	Value
1	Length of Fin	L_{Fin}	20 nm
2	Width of Fin	W_{Fin}	10 nm
3	Height of Fin	H_{Fin}	10 nm
4	Oxide Thickness	t_{ox}	1 nm
5	Buried Oxide Thickness	t_{box}	20 nm
6	Gate Workfunction	φ_G	4.7 eV
7	Source/Drain Workfunction	φ_{SD}	4.1 eV
8	Source/Drain Doping	$N_{S/D}$	10^{19} cm^3
9	Channel Doping	N_C	5×10^{17} cm^3

A. Surface Potential Model

In this section, an accurate analytical solution to the two dimensional Poisson's equation is modeled by influencing mobile charge carriers [12]. The cross sectional view of the FinFET in *x-y* plane is shown in Fig.1b. The 2D Poisson's equation can be given as,

$$\frac{d^2\varphi}{dx^2}+\frac{d^2\varphi}{dy^2}=\frac{q}{\varepsilon_{Si}}n_i e^{\frac{\varphi-V}{V_t}} \quad (1)$$

Where $\psi(x,y)$ is the electrostatic potential along the channel region, thermal voltage V_t = *0.0259 V*, n_i be the intrinsic carrier density and *V* be the quasi Fermi potential. By adopting super position principle, electrostatic potential [13] can be given as,

$$\varphi(x,y)=\varphi_x+u_L(x,y)+u_R(x,y) \quad (2)$$

Where ψ_x is solution to the 1D Poisson's equation,

$$\frac{d^2\varphi}{dx^2}=\frac{q}{\varepsilon_{Si}}n_i e^{\frac{\varphi_x-V}{V_t}} \quad (3)$$

ψ_x is obtained by twice integrating (3) and is obtained by

$$\varphi_x=V-2V_t\ln\left(\frac{t_{Si}}{2\beta}\sqrt{\frac{qn_i}{2\varepsilon_{Si}V_t}}\cos\left(\frac{2\beta}{t_{Si}}x\right)\right) \quad (4)$$

Where β is a function of V and varied from 0 to π/2 . For a given input bias V_{gs}, β can be obtained by solving non linear equation using bi section method,

$$\frac{V_{gs}-\Delta\phi-V}{2V_t}-\ln\left(\frac{2}{t_{Si}}\sqrt{\frac{2\varepsilon_{Si}V_t}{qn_i}}\right)=\ln\beta-\ln(\cos(\beta))-\frac{2\varepsilon_{Si}t_i}{\varepsilon_i t_{Si}}\beta\tan(\beta) \quad (5)$$

Where, $\Delta\phi$ is the work function difference between device gate electrode and the semiconducting channel. The electron quasi Fermi potential remains constant across the lateral direction of the channel and varies in transverse path of the channel because the movement of electrons from source region to drain region is observed in the channel region. It is assumed that the quasi Fermi potential remains constant until it reaches the drain to source junction. Accordingly in FinFETs, the quasi Fermi potential remains constant along the channel length barring at the source-channel junction. This causes ψ_x to read a constant value in they-direction barring the vicinity of source junction

$u_L(x, y) + u_R(x,y)$ is the solution to 2D Laplace equation,

$$\frac{d^2\varphi}{dx^2}+\frac{d^2\varphi}{dy^2}=0 \quad (6)$$

The solution to the 2 dimensional Laplace equation is obtained by the following expressions, where $u_L=\sum_{n=1}^{\infty} u_{Ln}(x,y)$ *and* $u_R=\sum_{n=1}^{\infty} u_{Rn}(x,y)$ and $u_{Ln}(x, y)+u_{Rn}(x,y)$ are specified as Eigen functions and are achieved as follows

$$u_{Ln}(x,y)=b_n\frac{\sinh(\pi(L-y)/\lambda_n)}{\sinh(\pi L/\lambda_n)}\sin\left(\frac{n\pi}{2}+\frac{\pi x}{\lambda_n}\right) \quad (7)$$

$$u_{Rn}(x,y) = c_n \frac{\sinh(\pi y/\lambda_n)}{\sinh(\pi L/\lambda_n)} \sin\left(\frac{n\pi}{2} + \frac{\pi x}{\lambda_n}\right) \quad (8)$$

Where λ_n Eigen values are achieved from,

$$\varepsilon_{Si} \tan\left(\frac{\pi t_i}{\lambda_n}\right) = \varepsilon_i \tan\left(\frac{n\pi}{2} - \frac{\pi t_{Si}}{2\lambda_n}\right) \quad (9)$$

The coefficients of first order are obtained by,[15]

$$b1 = \frac{2\lambda_1^2 \tan(\pi t_i/\lambda_1)\sin(\pi t_{Si}/2\lambda_1)}{\pi^2 t_i \left(\frac{t_{Si}}{2} + \frac{\sin(\pi t_{Si}/\lambda_1)}{\sin(2\pi t_i/\lambda_1)}\right) t_i} (\phi_{SC} - V_{gs} - \Delta\phi) \quad (10)$$

$$c_1 = \frac{\sin(\pi t_{Si}/2\lambda_1)}{\left(\frac{t_{Si}}{2} + \frac{\sin(\pi t_{Si}/\lambda_1)}{\sin(2\pi t_i/\lambda_1)}\right) t_i} \left(\frac{-4V_t\lambda_1}{\pi} \ln(\cos\beta_d) - \frac{2\lambda_1^2}{\pi^2} \frac{\varphi_s(t_{Si}/2) - \phi_{DC}}{t_i} \tan\left(\frac{\pi t_i}{\lambda_1}\right)\right) \quad (11)$$

Where φ_{SC} and φ_{DC} are built in potential for source and drain junctions respectively. β_d is determined from (5). The final interpretation for potential can be given as

$$\varphi(x,y) = \varphi_s + \cos(\pi x/\lambda_1)\left(\frac{b_1 \sinh(\pi(L-y)/\lambda_1) + c_1 \sinh(\pi y/\lambda_1)}{\sinh(\pi L/\lambda_1)}\right) \quad (12)$$

B. Lateral Electric Field

The lateral electric field is achieved by differentiating the surface potential, and is given by,

$$E_x(x,y) = \left(-\frac{\pi}{\lambda_1} b_1 \frac{\cos(\pi(L-y)/\lambda_1)}{\sinh(\pi L/\lambda_1)} + \frac{\pi}{\lambda_1} c_1 \frac{\cosh(\pi y/\lambda_1)}{\sinh(\pi L/\lambda_1)}\right)\cosh(\pi x/\lambda_1) \quad (13)$$

ψ_x will be uniform throughout in y direction, henceforth the differentiation of ψ_x will results to zero and thus lateral path turn into the effective tunneling path. Accordingly tunneling befalls exclusively in the channel region ahead the channel length. Consequently, in the modelling of electric field, it is considered to be in the lateral direction only.

C. Drain Current Model

The expression for the drain current is obtained by considering gradual channel approximation, which presumes that the change in the electric field across the channel is much insignificant than change in the electric field across the perpendicular direction to the gate channel length. By refereeing Pao and Sah's double integral Equation to drain current is calculated by,

$$I_{DS} = \mu_{eff} \frac{W}{L} \int_0^{V_{DS}} [-Q_i(V)] dV \quad (14)$$

D. Transconductance Model

Transconductance is the electrical property of the device. It is the change in the current at output port to change in voltage at input port. It shows the sensitivity of the device i.e. how fast the current will increase for a short duration of input voltage. Transconductance is denoted by g_m and is calculated by

$$g_m = (\partial I_{ds}/\partial V_{gs})\,|_{\text{Vds}} \quad (15)$$

Similarly, Output Conductance is calculated by,

$$G_d = (\partial I_{ds}/\partial V_{ds})\,|_{\text{Vgs}} \quad (16)$$

III. Results and Discussion

Based on the analytical modeling derived in section 3. The characteristics for Tri gate FinFET is validated with 2 dimensional numerical device simulation results that numerically solve poisons equation [14]. In the figures discussed lines are referred to simulated data and symbols referred to the modeled data.

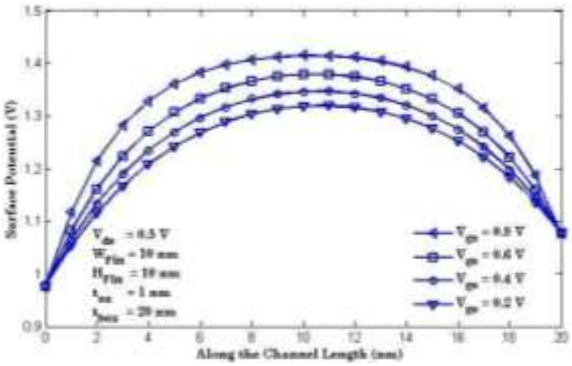

Figure 2.Surface Potential in variation with gate Voltage for V_{DS} = *0.1 V.*

Fig 2 shows the plot for surface potential for Tri-gate FinFET along the channel direction in variation with different input gate biases for a constant drain bias V_{DS}=0.1 V. based on the above figure it is clearly seen that in increase in input gate voltage surface potential also increases providing a thicker inversion charge layer for electrons to migrate from source to drain along the channel of the device.

Fig 3 shows the plot of lateral electric field along the channel length for different input gate voltage for a constant drain bias of *0.1 V.* the plot shows the change in electric field along the source-channel and channel-drain junction which increases along with the input gate to source voltage.

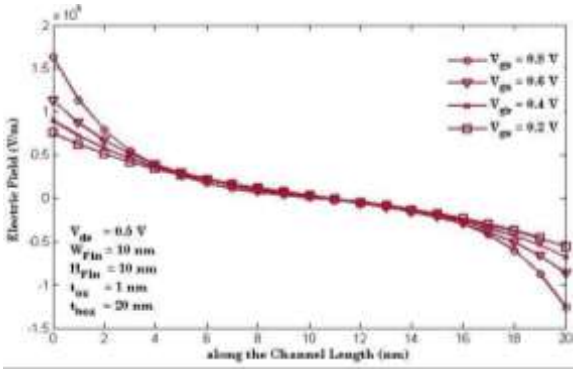

Figure.3. Lateral Electric Filed in variation with input gate bias for $V_{DS} = 0.1$ V

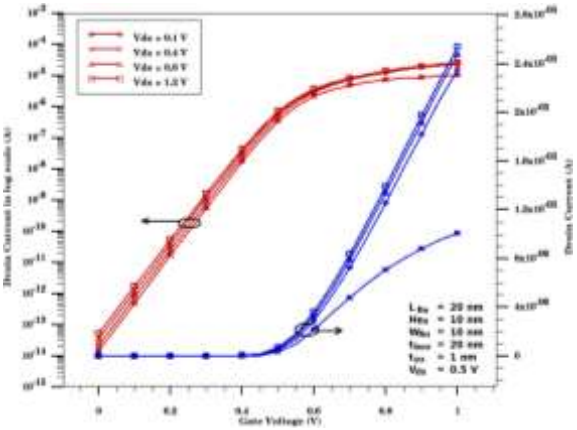

Figure 4. Transfer characteristics in both linear and logarithmic scale for different drain bias (V_{DS}).

Fig 4 shows the *V-I* characteristics in linear scale and logarithmic scale for distinct drain biases respectively, linear part of *V-I* characteristics shows the higher value of drain current for higher input drain bias, which also shows the on current variation along with the input biases. Logarithmic scale of *V-I* characteristics shows the off current (I_{OFF}) as well as on current (I_{ON}) of the device. The performance of the device is gauged by the higher I_{ON}/I_{OFF} ratio. Our model shows an OFF current of 10^{-14} *A* and ON current of 10^{-5} *A* with I_{ON}/I_{OFF} ratio of around 10^{9} for drain bias of *0.4 V*.

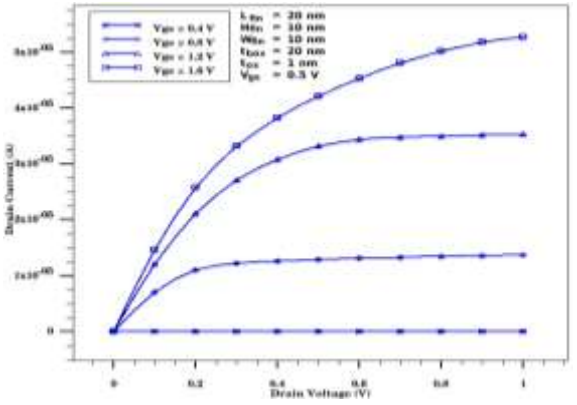

Figure 5.Output characteristics for different input biases.

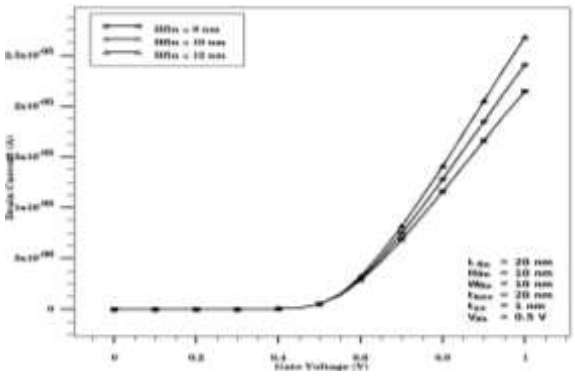

Figure 6.a. V-I Characteristics in variation with Silicon Fin Height (H_{Fin}).

Fig 5 shows the plot for output characteristics for Tri-gate FinFET for varied input gate bias. It shows no current for the input gate (0.4 V) to source voltage less than threshold voltage (0.42 V). it shows constant drain current for input voltage less than 1.2 V, after reaching the saturation point for drain saturation voltage V_{DSat}. For the input voltage above 1.2 V the channel undergo channel length modulation and with effect to this output current starts increasing linearly with respect to drain bias.

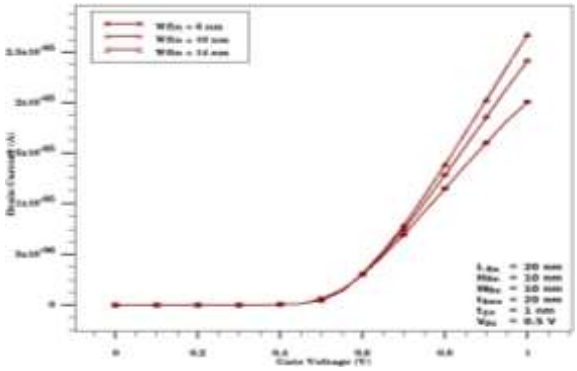

Figure 6.b. V-I Characteristics in variation with Silicon Fin Width (W_{Fin}).

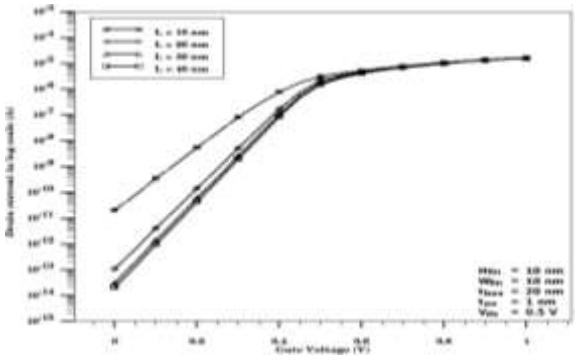

Figure 6.c. V-I Characteristics in logarithmic scale for different Fin Length (L_{Fin}).

Fig 6 shows the plot of *V-I* characteristics for variation in different device parameters. Fig 6a, 6b and 6c shows the transfer characteristics in variation with height, width and length of the fin respectively

showing better performance for the device parameters H_{Fin}=*12 nm*, W_{Fin}= *14 nm* and L_{Fin} = *30 nm*. Fig 6.d shows the *V-I* characteristics for constant width and height of Silicon fin and shows a superior performance for *12 nm*.

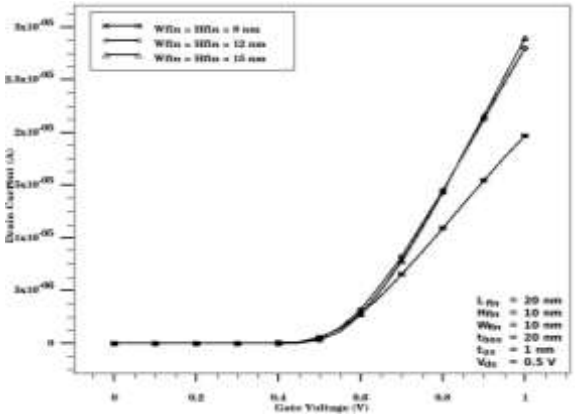

Figure 6.d. V-I characteristics for constant device parameters.

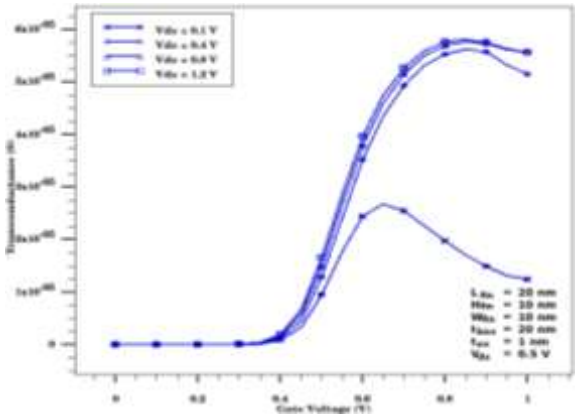

Figure 7.Transconductance plot for FinFET.

Fig 7 & 8 shows the AC parameters such as Transconductance and Output Conductance of the Tri-gate FinFET. Fig 7 represents the plot of transconductance for Tri gate FinFET. Fig 8 presents the plot of Output Conductance of the tri gate FinFET.

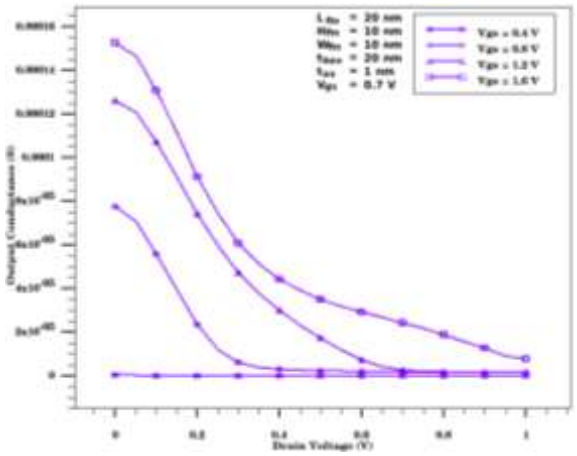

Figure 8.Output Conductance for varied gate bias.

Fig.7. presents the plot of transconductance in variation with input gate bias. Transconductance shows the sensitivity of the device. i.e., how the device will produce the output current for a step input voltage or how much strong the device is to convert a small amount of voltage into a desirable current. Fig 7 shows the rapid increase in the drain current for gate voltage *0.7 V*.

Table 2 shows the values of subthreshold swing (*SS*) and threshold voltage (V_t) for different device parameters. Based on the obtained data we 60 obtain a sub threshold swing of nearly mV/decade for device parameters H_{Fin}=W_{Fin}=*8 nm* and L_{Fin}=*40 nm* with threshold voltage of 0.36 V.

Table 2. Sub threshold swing (*SS*) and Threshold voltage (V_t) for different device parameters.

Fin Length (L_{Fin}) nm	**Fin Width (W_{Fin}) nm**	**Fin Height (H_{Fin}) nm**	**Sub threshold Swing (*SS*) mV/decade**	**Threshold Voltage (V_t) V**
20	15	15	72.8	0.351
20	10	10	65.9	0.324
20	12	08	64.3	0.318
20	08	08	63.8	0.300
30	10	08	61.29	0.351
30	08	08	61.21	0.343
40	08	08	60.48	0.368

Based on the work carried out, we can conclude that for device parameters with H_{Fin}=*12 nm*, W_{Fin}=*8 nm* and L_{Fin}=*30 nm* shows a better performance with *SS* nearly *61 mV/decade*, I_{ON}/I_{OFF} ratio of 10^9, threshold voltage of *0.35 V* which shows better device structure for VLSI circuits and semiconductor memories.

IV. Conclusion

The analytical model has been developed for emerging SOI-FinFET device. Close form models are developed to estimate the values of the surface potential using superposition principle. Using this surface potential model, an expression for Electric field of the SOI-FinFET is derived. These models have been used to investigate the behavior of SOI-FinFET and electrical characteristics like I-V characteristics, transconductance, output conductance, sub threshold swing and threshold voltage are modeled. In addition to analyzing the impact of various geometric parameters on the behavior of the device, the developed models are validated by numerical simulation results. It is observed that by optimizing these dimensional factors, a sub threshold swing (S) value close to 60 mV/decade and a threshold voltage of 0.35 V can be

achieved for SOI-FinFET which is well suited for VLSI circuits and semiconductor memories.

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